Control Panel Functionality Overview

Control Panel V2.0

Rev 0.0

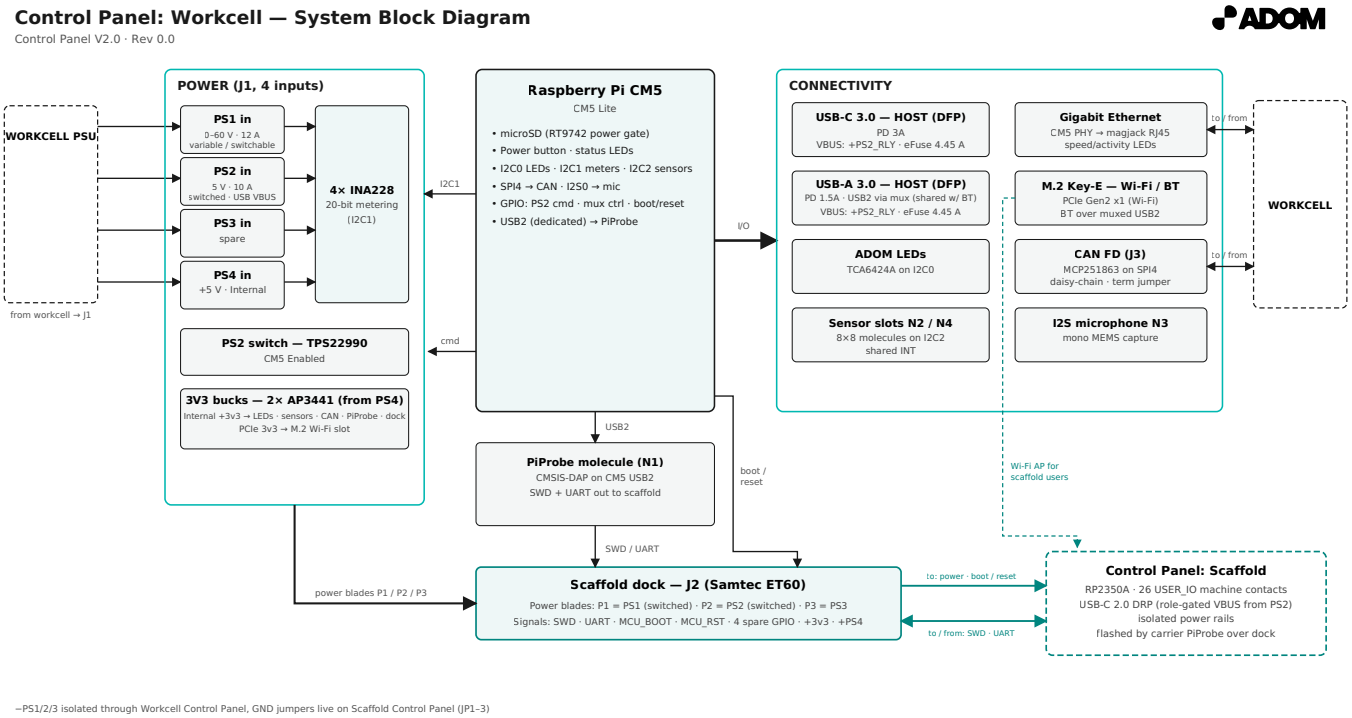
Companion: Control Panel Test Method Overview / Test Procedure

Caleb Taylor | 2026-07-11

FUNCTIONS

Power inputs (J1)	PS1 (0—60 V/12 A switched user rail) • PS2 (5 V/10 A switched user rail) • PS3 spare (user rail) • PS4 5 V (Internal, fused + TVS). Isolated −PS1/2/3 returns; GND↔EGND jumper bond at Scaffold.
Power metering	4× INA228 (20-bit) on I2C1 — per-rail current + bus voltage, Kelvin-sensed shunts.
PS2 switched rail	CM5-enabled TPS22990 10 A load switch through an NSi8210 isolator (return may float ±2.5 V); state readback.
Compute	CM5 Lite, microSD boot (power-gated socket), power button, status LEDs, 3.3 V logic + M.2 bucks enabled by CM5.
Networking	Gigabit Ethernet (CM5 PHY → magjack RJ45 with speed/activity LEDs).
USB	USB-C 3.0 (orientation mux, CC 3 A advertisement, eFuse-protected VBUS from PS2) • USB-A 3.0 (SuperSpeed direct; USB2 shared with Bluetooth via mux; eFuse-protected VBUS from PS2).
USB roles	**Host on every port:** USB-C is strapped DFP (host, 3 A source) and the CM5 USB_OTG strap is host; USB-A is host; the internal USB2 port is host to the PiProbe. The carrier never operates as a USB device.
Wireless	M.2 Key-E: Wi-Fi on PCIe Gen2 x1, Bluetooth on the muxed USB2 path (mutually exclusive with USB-A).
CAN FD	MCP251863 (controller + transceiver) on SPI4; chained with workcell; termination jumper.
Scaffold dock (J2)	3 power blades (PS1 (switched, variable) / PS2 (switched) / PS3 (Spare)) + SWD/UART debug, MCU boot/reset control, 4 spare GPIO, +3v3/+PS4.
Debug	On-board PiProbe (CMSIS-DAP, RP2040) on the CM5's dedicated USB2 — flashes/debugs User MCU (SWD/UART).
Molecule slots	(2) 8×8 sensor slots on I2C2 with shared interrupt • (1) I2S (MEMS microphone).
Indicators	Status LEDs: PWR (red) • ACT (green) • PCIE (green) • USB FAULT (red) • 18 ADOM LEDs via TCA6424A expander on I2C0 (feed indicator).

SYSTEM BLOCK DIAGRAM



–PS1/2/3 isolated through Workcell Control Panel, GND jumpers live on Scaffold Control Panel (JP1–3)

CM5 PIN TREE

Grouped by subsystem; pin = CM5 connector pin. Full 200-pin map: CM5_Pinout_Tree / interactive viewer.

Power — +PS4_SENS ×6, ×4, +3v3_CM5 ×2, GPIO_VREF ×1

System

16	FAN_TACHO
19	FAN_PWM
20	EEPROM_nWP EEPROM_nWP
24	GPIO26
35	ID_SC EXPD_NRST.IO1
89	WiFi_nDisable
91	BT_nDisable
92	PWR_BUT PWR_BUT
93	nRPIBOOT
94	CC1
95	LED_nPWR nPWR_LED
96	CC2

microSD (CM5 Lite)

57	SD_CLK SD_CLK
61	SD_DAT3 SD_DAT3
62	SD_CMD SD_CMD
63	SD_DAT0 SD_DAT0
64	SD_DAT5
67	SD_DAT1 SD_DAT1
68	SD_DAT4
69	SD_DAT2 SD_DAT2
70	SD_DAT7
72	SD_DAT6
73	SD_VDD_Override
75	SD_PWR_ON SD_PWR_ON

I2C buses

28	GPIO13 SENSOR_I2C-2.SCL
29	GPIO16 SENSOR_I2C-2.INT
31	GPIO12 SENSOR_I2C-2.SDA
56	GPIO3 PWR_I2C-1.SCL
58	GPIO2 PWR_I2C-1.SDA
80	SCL0 LED_I2C-0.SCL
82	SDA0 LED_I2C-0.SDA

Ethernet (GigE)

3	Ethernet_Pair3_P ETH.TRD3_P
4	Ethernet_Pair1_P ETH.TRD1_P
5	Ethernet_Pair3_N ETH.TRD3_N
6	Ethernet_Pair1_N ETH.TRD1_N
9	Ethernet_Pair2_N ETH.TRD2_N
10	Ethernet_Pair0_N ETH.TRD0_N
11	Ethernet_Pair2_P ETH.TRD2_P
12	Ethernet_Pair0_P ETH.TRD0_P
15	Ethernet_nLED3(3.3v) ETH_LEDG
17	Ethernet_nLED2(3.3v) ETH_LEDY
18	Ethernet_SYNC_OUT(3.3v)
21	LED_nACT LED_nACT

USB3-0 (USB-C J10)

128	USB3-0-RX_N USER_USB3-0.RX_N
130	USB3-0-RX_P USER_USB3-0.RX_P
134	USB3-0-D_P USER_USB3-0.D_P

136 USB3-0-D_N USER_USB3-0.D_N
140 USB3-0-TX_N USER_USB3-0.TX_N
142 USB3-0-TX_P USER_USB3-0.TX_P

USB3-1 (USB-A J9)

157 USB3-1-RX_N USER_USB3-1.RX_N
159 USB3-1-RX_P USER_USB3-1.RX_P
163 USB3-1-D_P MUX_USB3-1.D_P
165 USB3-1-D_N MUX_USB3-1.D_N
169 USB3-1-TX_N USER_USB3-1.TX_N
171 USB3-1-TX_P USER_USB3-1.TX_P

USB3-1 mux control

48 GPIO27 MUX_USB3-1_SEL
50 GPIO17 MUX_USB3-1_OEn

USB 2.0 OTG

101 USB_OTG_ID USB_OTG
103 USB2_N DEBUG_USB2_N
105 USB2_P DEBUG_USB2_P

PCIe Gen2 x1

102 PCIe_nCLKREQ PCIE.nCLKREQ
104 PCIE_nWAKE PCIE.nWAKE
106 PCIE_PWR_EN PCIE.PWR_EN
109 PCIe_nRST PCIE_nRST
110 PCIe_CLK_P WIFI_PCIE.CLK_P
111 VBUS_EN 3v3_PWR_EN
112 PCIe_CLK_N WIFI_PCIE.CLK_N
116 PCIe_RX_P WIFI_PCIE.RX_P
118 PCIe_RX_N WIFI_PCIE.RX_N
122 PCIe_TX_P WIFI_PCIE.TX_P
124 PCIe_TX_N WIFI_PCIE.TX_N

M.2 / PCIe control

41 GPIO25 PCIE.BT_REG_ON
45 GPIO24 PCIE.WL_REG_ON

CAN FD (SPI4)

30 GPIO6 CAN_SPI-4.nINT0
34 GPIO5 CAN_SPI-4.nINT
37 GPIO7 CAN_SPI-4.nINT1
38 GPIO11 CAN_SPI-4.SCK
39 GPIO8 CAN_SPI-4.nCS
40 GPIO9 CAN_SPI-4.SDO
44 GPIO10 CAN_SPI-4.SDI

I2S microphone

26 GPIO19 MIC_I2S-0.WS
27 GPIO20 MIC_I2S-0.SD
49 GPIO18 MIC_I2S-0.SCK

PiProbe debug

46 GPIO22 DEBUG_BOOT
47 GPIO23 DEBUG_RST

Scaffold dock (J2)

25 GPIO21 MCU_RST
36 ID_SD SPARE.IO0
51 GPIO15 SPARE.IO15
54 GPIO4 SPARE.IO4
55 GPIO14 SPARE.IO14
97 CAM_GPIO0 MCU_BOOT
100 CAM_GPIO1 +PS2_EN_IO35

Ground — 51 pins · Unused (HDMI, MIPI) — 44 pins n.c.