

Control Panel Test Method Overview

Control Panel V2.0

Rev 0.0

Use with Control Panel Test Procedure

1. INITIAL DEVICE SETUP & FIRST BOOT

- First power — PS4 input (scope) — §1.1

- SD & first boot — §1.2

- boot success

- boot loop ×10

- soak / power gate

- PWR_BTN — §1.3

- edge / debounce

- shutdown press

- wake from halt

- nPWR_LED — §1.4

- state truth table

- Ethernet link & SSH (90 m cable) — §1.5

- lights

- gigabit link + throughput

- flap loop ×50

- SSH

2. POWER

- 3V3 main ripple (scope) — §2.1

- @ startup

- @ power

- +PS2 relay (on—off) — §2.2

- turn-on / turn-off timing

- R_ON / drop @ 10 A

- power-meter cross-check

- isolation (–PS2 offset ± 2.5 V)

- off-state leakage / bleed

- thermal @ 9 A

- **Power meters 1—4** — §2.3

- I2C

- zero offset

- calibration

- bus voltage

- thermal validation

3. CM5 BUSES

- **I2C (0—2)** — §3.1

- edges

- recognition

4. ADOM LEDS

- **LED ring** — §4.1

- 0x22 ACK

- ring script 22/22

5. USB (SS)

- **USB-C 3.0 - PD-CNTRL** — §5.1

- ID-gate

- power delay

- advertised current

- loaded VBUS

- plug direction (CC1/CC2)

- **USB-C 3.0 - DATA** — §5.2

- SS speed

- throughput soak (both orientations)

- 2.0 speed

- **USB-A** — §5.3

- hot-plug ×10

- spin-up droop

- **USB power switch (eFuse)** — §5.4

- float / off state

- ILIM

- retry behavior

- fault LED

- UVLO / OVP

6. PCIE (WIFI / BT)

- **3V3_PCIE** — §6.1

- enable

- startup ramp

- ripple under TX

- **WiFi** — §6.2

- module detect (PCIe link)

- firmware / interface up

- scan / antenna check

- associate + throughput

- AER delta

- **BT** — §6.3

- mux to BT

- scan / pair

- stability

- exclusivity (USB-A)

- mux glitch

7. CAN

- **Controller communications (SPI)** — §7.1

- **Internal loopback** — §7.2

- **Bus levels / termination (JP6)** — §7.3

- **FD interop** — §7.4

- **Interrupts** — §7.5

8. NESTED

- **PiProbe** — §8.1

- connection check

- bootloader flash cycle

- **MIC** — §8.2

- clocks / edges

- noise floor

- tone capture

- EMI check

- **Sensor** — §8.3

- I2C presence

- chip IDs (BME690 / BMI270)

- interrupt

- environmental data

- IMU data

9. SCAFFOLD

- **Power** — §9.1

- 3V3 @ MCU (ramp / IO load)

- eFuse ILIM + fault LED

- +PS2 delivered @ 5 A

- **USB** — §9.2

- client role

- host role

- client speed

- **MCU (RP2350)** — §9.3

- SWD scan + margin

- flash + verify (SWD / UF2)

- UART echo (115200 / 1 M / 3 M)

- boot / reset control ×20

- USER_IO 26/26 + reserved pins

APPENDIX A — ENGINEERING-ONLY

- **USB VBUS crowbar** — §A.1 (sacrificial board only)

- **CAN transceiver fault tolerance** — §A.2 (sacrificial board only)

Section references (§) point into the Control Panel Test Procedure, Rev 0.0.