

CURRENT MODE PWM CONTROLLER

DESCRIPTION

The UC284x and UC384x are fixed frequency current mode PWM controller. They are specially designed for OFF Line and DC to DC converter applications with a minimal external components. Internally implemented circuits include a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET. Protection circuitry includes built under voltage lockout and current limiting.

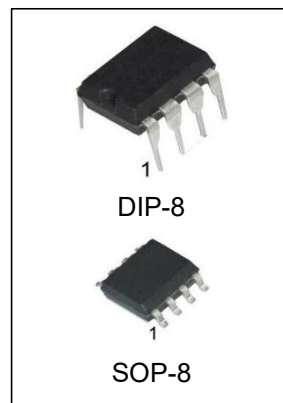
The UC2842/44, UC3842/44 have UVLO thresholds of 16 V (on) and 10 V (off). The corresponding thresholds for the UC2843/45, UC3843/45 are 8.4V (on) and 7.6V (off).

The UC2842/43, UC3842/43 can operate within 100% duty cycle.

The UC2844/45, UC3844/45 can operate within 50% duty cycle.

The UC2842/43/44/45 is characterized for operation from TA = -40°C to 85°C.

The UC3842/43/44/45 is characterized for operation from TA = 0°C to 70°C.



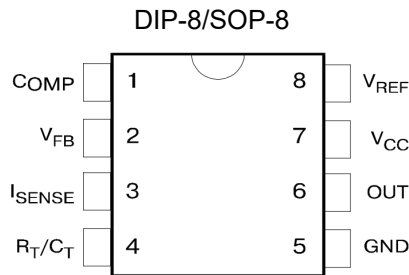
FEATURES

- Low Start-Up and Operating Current
- Under voltage Lockout With Hysteresis
- High Current Totem Pole Output
- Operating Frequency Up To 500KHz

ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
UC2842N	DIP-8	UC2842	TUBE	2000/box
UC2843N	DIP-8	UC2843	TUBE	2000/box
UC2844N	DIP-8	UC2844	TUBE	2000/box
UC2845N	DIP-8	UC2845	TUBE	2000/box
UC2842M/TR	SOP-8	UC2842	REEL	2500/reel
UC2843M/TR	SOP-8	UC2843	REEL	2500/reel
UC2844M/TR	SOP-8	UC2844	REEL	2500/reel
UC2845M/TR	SOP-8	UC2845	REEL	2500/reel
UC3842N	DIP-8	UC3842	TUBE	2000/box
UC3843N	DIP-8	UC3843	TUBE	2000/box
UC3844N	DIP-8	UC3844	TUBE	2000/box
UC3845N	DIP-8	UC3845	TUBE	2000/box
UC3842M/TR	SOP-8	UC3842	REEL	2500/reel
UC3843M/TR	SOP-8	UC3843	REEL	2500/reel
UC3844M/TR	SOP-8	UC3844	REEL	2500/reel
UC3845M/TR	SOP-8	UC3845	REEL	2500/reel

Pin CONNECTION

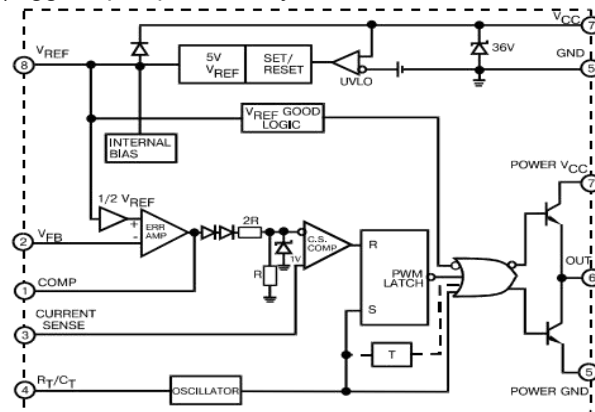


PIN FUNCTION

N	FUNCTION	DESCRIPTION
1	COMP	This pin is the Error Amplifier output and is made for loop compensation.
2	VFB	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	ISENSE	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	RT/CT	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sink by this pin.
7	VCC	This pin is the positive supply of the integrated circuit.
8	Vref	This is the reference output. It provides charging current for capacitor CT through resistor RT.

BLOCK DIAGRAM

(toggle flip flop used only in UC2844/45, UC3844/45)



Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply Voltage (low impedance source)	VCC	30	V
Output Current	Io	1	A
Input Voltage (Analog Inputs pins 2,3)	VI	0.3 to 5.5	V
Error Amp Output Sink Current	ISINK (E.A)	10	mA
Power Dissipation (TA=25°C)	PO	1	W
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temperature (Soldering, 10 seconds)	TL	260	°C

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

Electrical characteristics (*VCC=15V, RT=10k , CT=3.3nF, TA=0°C to +70°C, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Section						
Reference Output Voltage	VREF	T _J = 25°C, I _{REF} = 1 mA	4.9	5.0	5.1	V
Line Regulation	ΔVREF	12V ≤ V _{CC} ≤ 25 V		6.0	20	mV
Load Regulation	ΔVREF	1 mA ≤ I _{REF} ≤ 20mA		6.0	25	
Short Circuit Output Current	ISC	T _A = 25°C		-100	-180	mA
Oscillator Section						
Oscillation Frequency	f	T _J = 25°C	47	52	57	KHz
Frequency Change with Voltage	Δf/ΔV _{CC}	12V ≤ V _{CC} ≤ 25 V		0.05	1.0	%
Oscillator Amplitude	V(OSC)	(peak to peak)		1.6		V
Error Amplifier Section						
Input Bias Current	I _{BIAS}	V _{FB} =3V		-0.1	-2	μA
Input Voltage	V _I (E.A)	V _{pin1} = 2.5V	2.42	2.5	2.58	V
Open Loop Voltage Gain	A _{VOL}	2V ≤ V _O ≤ 4V	65	90		dB
Unity Gain Bandwidth	UGBW	T _J =25°C, Note 3	0.5	0.6		MHz
Power Supply Rejection Ratio	PSRR	12V ≤ V _{CC} ≤ 25 V	60	70		dB
Output Sink Current	I _{SINK}	V _{pin2} = 2.7V, V _{pin1} = 1.1V	2	7		mA
Output Source Current	I _{SOURCE}	V _{pin2} = 2.3V, V _{pin1} = 5V	-0.5	-1.0		mA
High Output Voltage	V _{OH}	V _{pin2} = 2.3V, R _L = 15KΩ to GND	5.0	6.0		V
Low Output Voltage	V _{OL}	V _{pin2} = 2.7V, R _L = 15KΩ to PIN 8		0.8	1.1	
Current Sense Section						
Gain	G _V	(Note 1 & 2)	2.85	3.0	3.15	V/V
Maximum Input Signal	V _I (MAX)	V _{pin1} = 5V (Note1)	0.9	1.0	1.1	V
Supply Voltage Rejection	SVR	12V ≤ V _{CC} ≤ 25 V (Note 1)		70		dB
Input Bias Current	I _{BIAS}	V _{pin3} = 3V		-3.0	-10	μA
Output Section						
Low Output Voltage	V _{OL}	I _{SINK} = 20 mA		0.08	0.4	V
		I _{SINK} = 200 mA		1.4	2.2	
High Output Voltage	V _{OH}	I _{SINK} = 20 mA	13	13.5		
		I _{SINK} = 200 mA	12	13.0		
Rise Time	t _R	T _J = 25°C, C _L = 1nF (Note 3)		45	150	nS
Fall Time	t _F	T _J = 25°C, C _L = 1nF (Note 3)		35	150	
Undervoltage Lockout Section						
Start Theshold	V _{TH} (ST)	UC2842/44,UC3842/44	14.5	16.0	17.5	V
		UC2843/45,UC3843/45	7.8	8.4	9.0	
Min. Operating Voltage (After Turn On)	V _{OPR} (min)	UC2842/44,UC3842/44	8.5	10	11.5	V
		UC2843/45,UC3843/45	7.0	7.6	8.2	
PWM Section						
Max. Duty Cycle	D(MAX)	UC2842/43,UC3842/43	95	97	100	%
		UC2844/45,UC3844/45	47	48	50	
Min. Duty Cycle	D(MAX)				0	
Total Standby Current						
Start Up Current	I _{ST}	UC3842/43/44/45		0.17	0.3	mA
Operating Supply Current	I _{CC} (OPR)	V _{pin3} = V _{pin2} = 0V		13	17	
Zener Voltage	V _Z	I _{CC} =25 mA	30	38		V

* Adjust VCC above the start threshold before setting it to 15V.

Note 1: Parameter measured at trip point of latch with V_{pin2}=0.

Note 2: Gain defined as A=ΔV_{pin1}/ΔV_{pin3} ; 0 ≤ V_{pin3} ≤ 0.8V.

Note 3: These parameters, although guaranteed, are not 100% tested in production.

APPLICATION INFORMATION

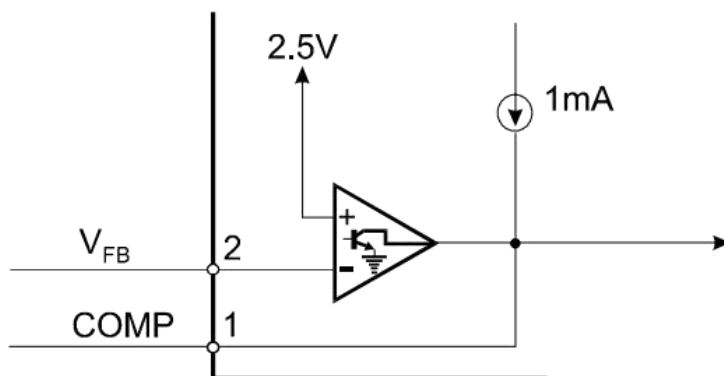


Figure 1. Error Amp Configuration

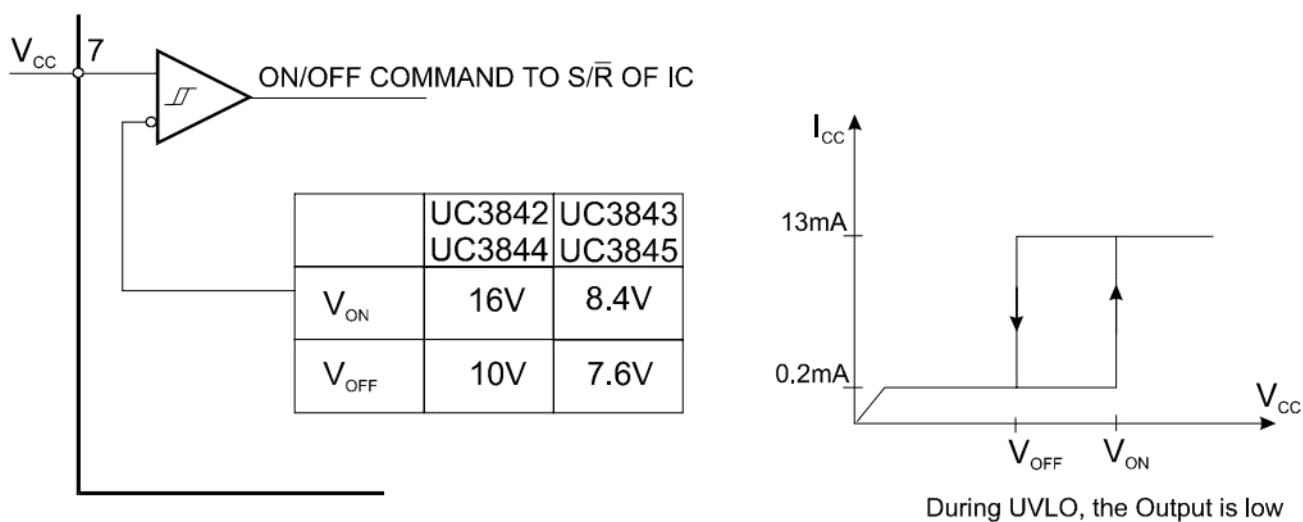
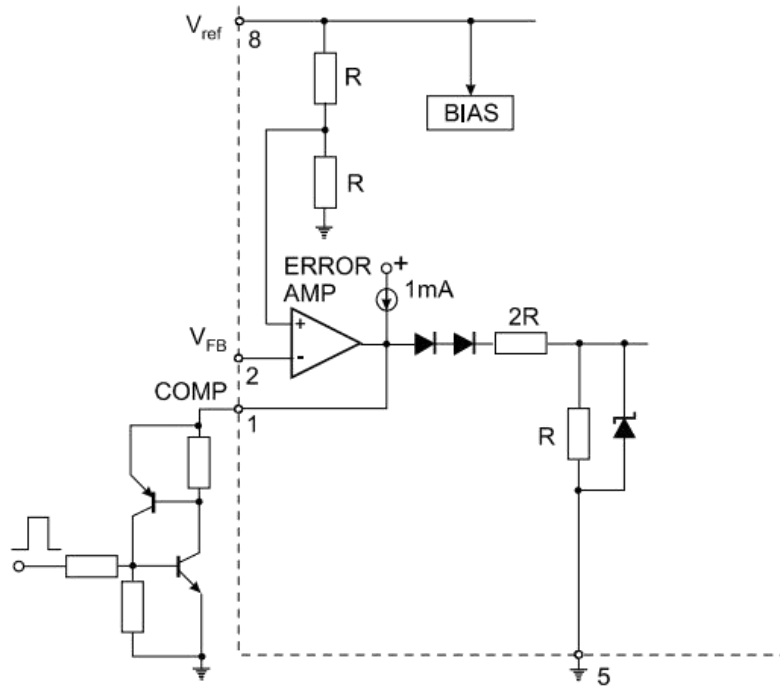


Figure 2. Under voltage Lockout



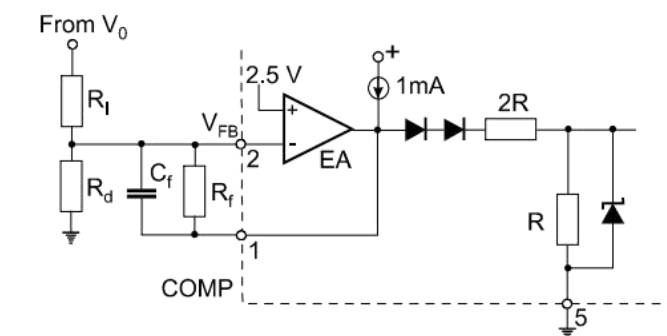
Figure 3. Current Sense Circuit



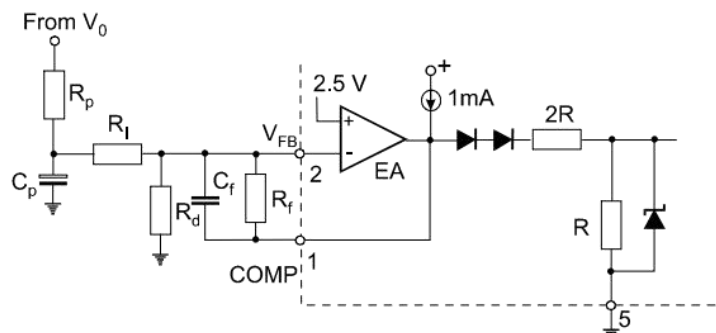


SCR must be selected for a holding current of less than 0.5mA.
The simple two transistor circuit can be used in place of the SCR as shown.

Figure 5. Latched Shutdown



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 6. Error Amplifier Compensation

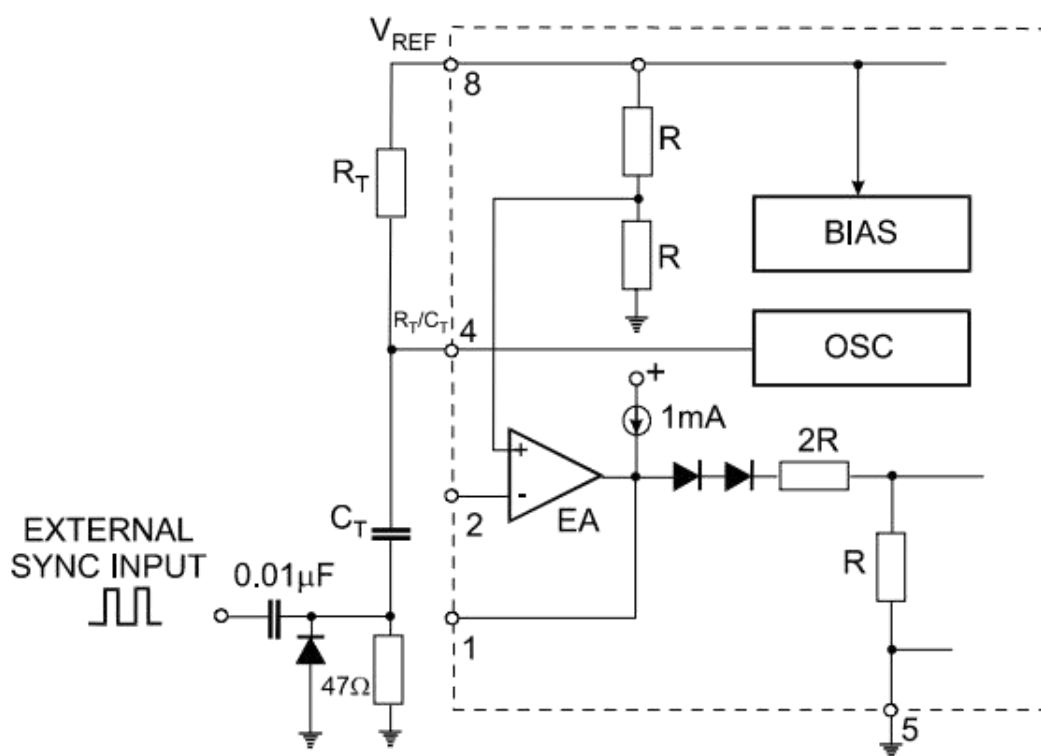


Figure 7. External Clock Synchronization

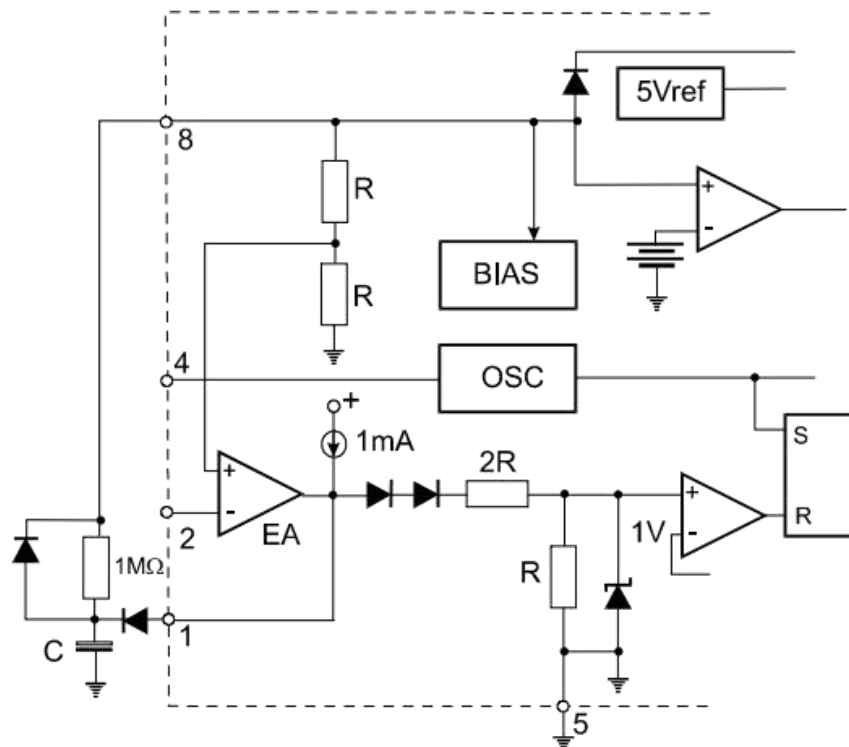


Figure 8. Soft-Start Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

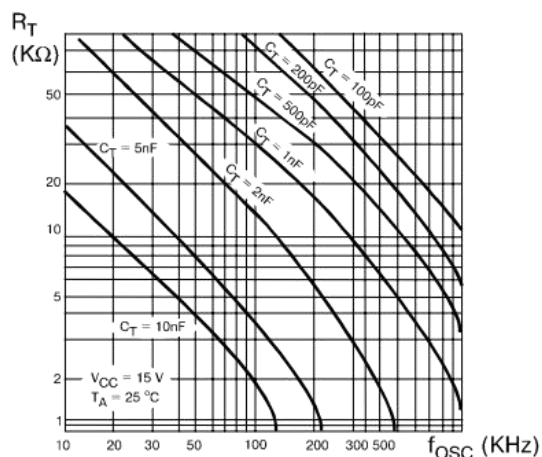


Figure 1. Timing Resistor vs. Oscillator Frequency

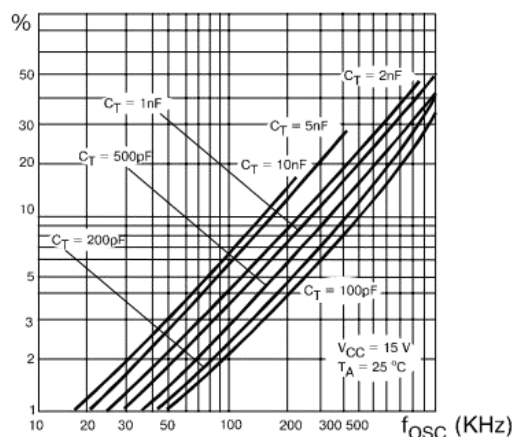


Figure 2. Output Dead-Time vs. Oscillator Frequency

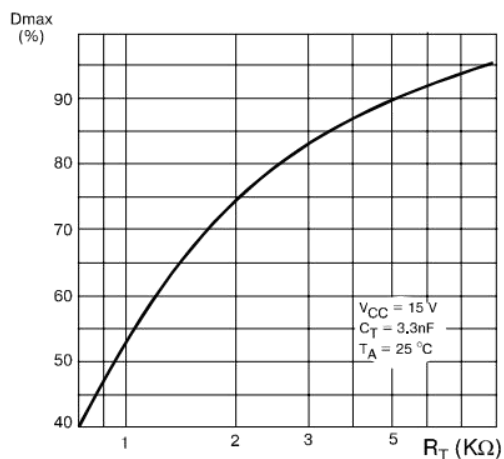


Figure 3. Maximum Output Duty Cycle vs. Timing Resistor (UC3842/43)

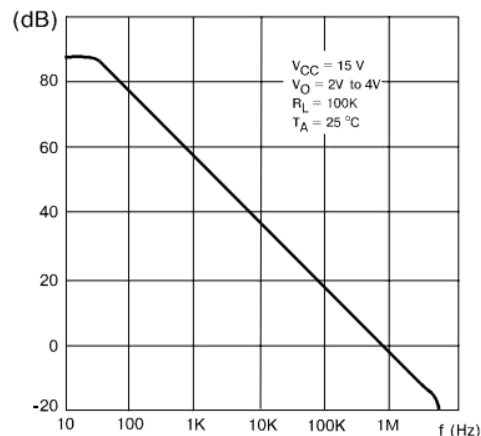


Figure 4. Error Amp Open-Loop Gain vs. Frequency

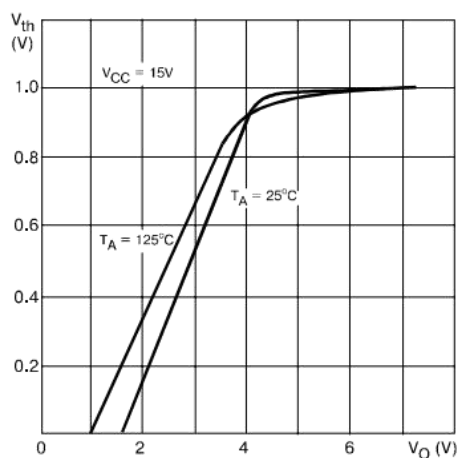


Figure 5. Current Sense Input Threshold vs. Error Amp Output Voltage

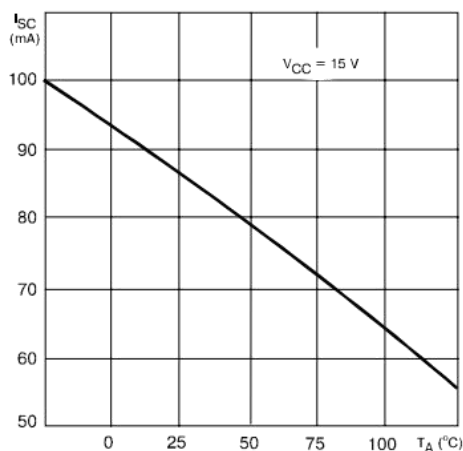


Figure 6. Reference Short Circuit Current vs. Temperature

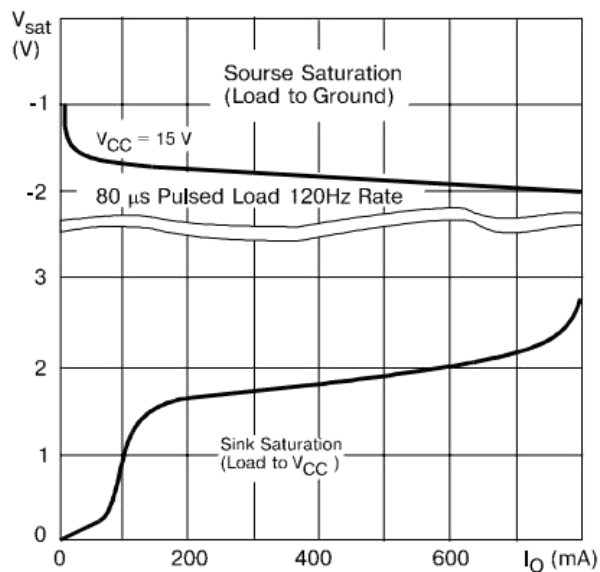


Figure 7. Output Saturation Voltage vs. Load Current
 $T_A = 25^\circ\text{C}$

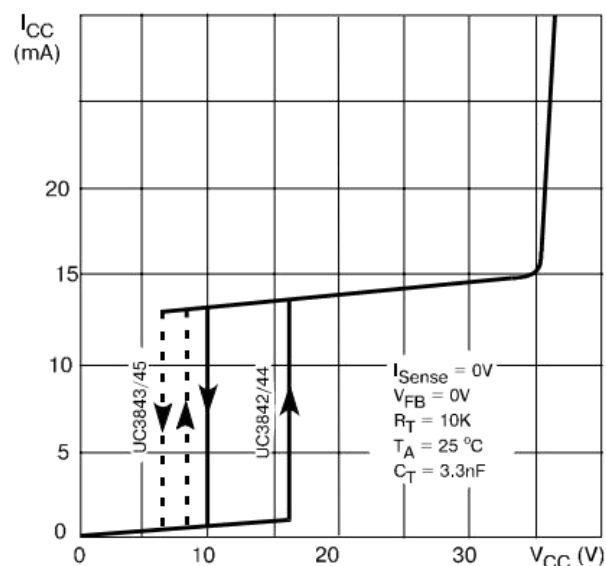


Figure 8. Supply Current vs. Supply Voltage

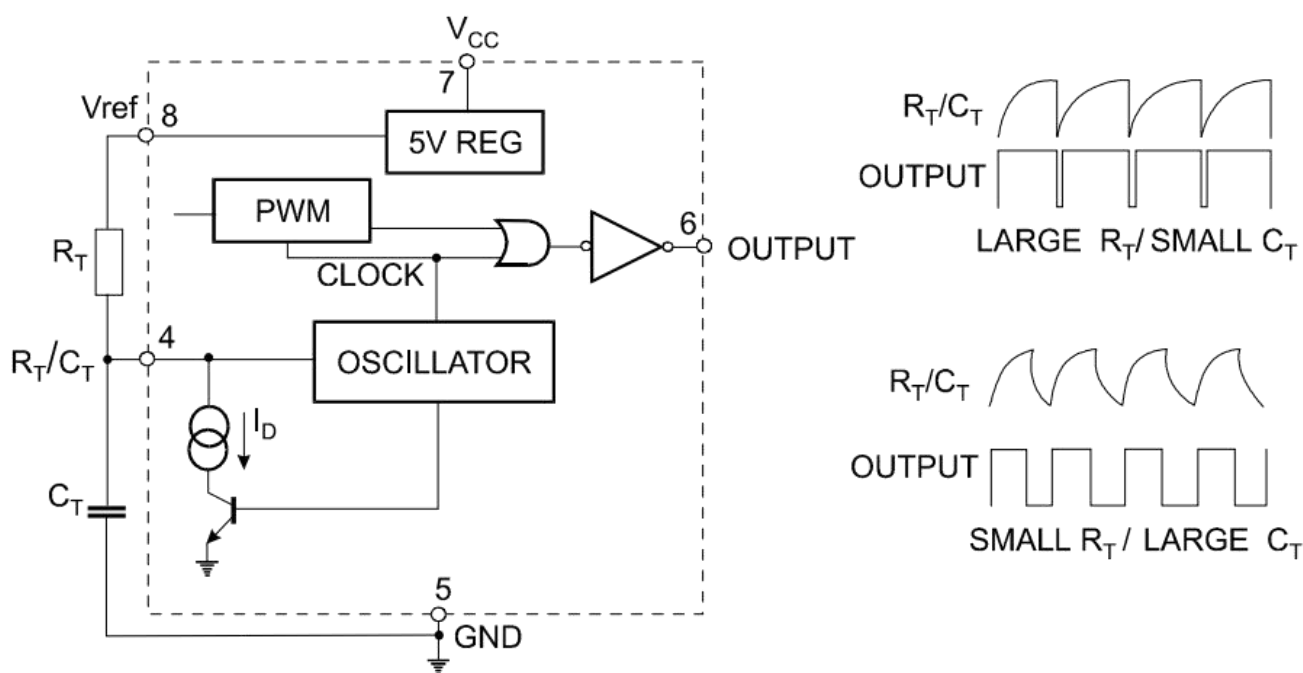
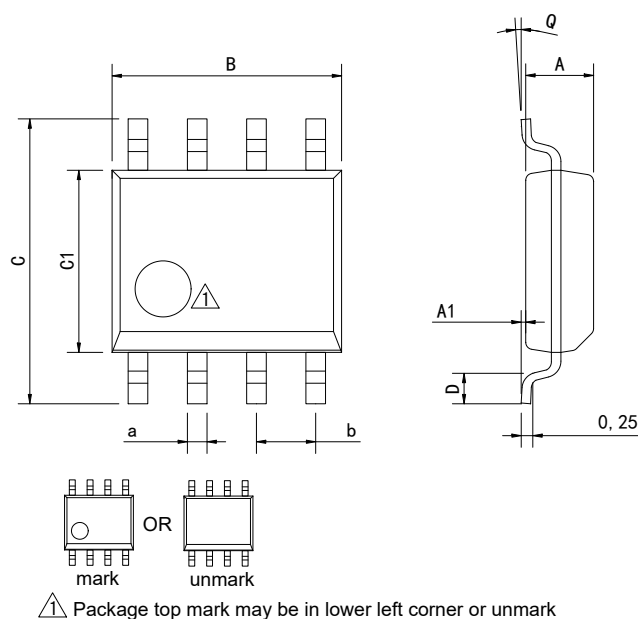


Figure 9. Oscillator and Output Waveforms

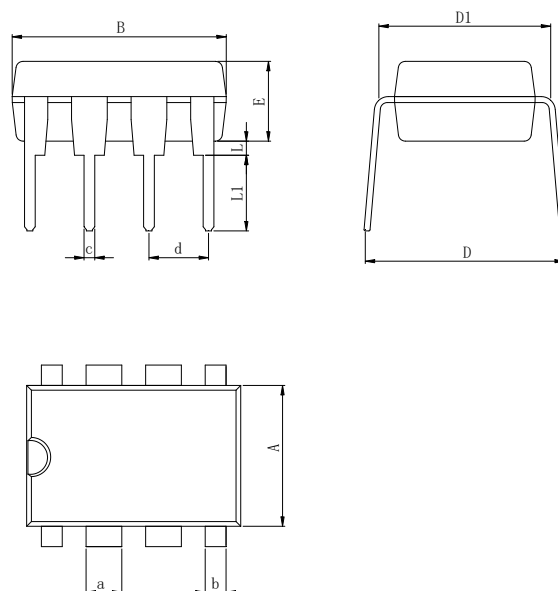
Physical Dimensions

SOP-8



Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2015-9	New	1-12
V1.1	2019-10	Update encapsulation type、Updated DIP-8 dimension、Update Description.	1、 10
V1.2	2024-11	Update Lead Temperature	2
V1.3	2025-12	Update important statements、 Update SOP-8 Dimension drawing	10、 12

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