

TRSF3221E 采用小型封装、具有 $\pm 15\text{kV}$ IEC ESD 保护的 3V 至 5.5V 单通道 RS-232 1Mbit 线路驱动器和接收器

1 特性

- 为 RS-232 引脚提供 ESD 保护
 - $\pm 15\text{kV}$ 人体放电模型 (HBM)
 - $\pm 8\text{kV}$ IEC 61000-4-2 接触放电
 - $\pm 15\text{kV}$ IEC 61000-4-2 空气间隙放电
- 由 3V 至 5.5V V_{CC} 电源供电
- 速率高达 1Mbit/s
 - 低速引脚兼容器件 (250kbit/s) - TRSF3221E
- 采用近似于芯片级封装的 16 引脚 VQFN (RGT, 比 TSSOP 封装小 82%)
- 低待机电流: $1\mu\text{A}$ (典型值)
- 外部电容器: $4 \times 0.1\mu\text{F}$
- 支持 5V 逻辑输入 (3.3V 电源时)
- 自动断电功能可自动禁用驱动器以节省能耗

2 应用

- 工业 PC
- 有线网络
- 数据中心和企业级计算
- 电池供电型系统
- PDA
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

3 说明

TRSF3221E 包含一个线路驱动器、一个线路接收器和一个具有引脚对引脚 (串行端口连接引脚, 包括 GND) $\pm 15\text{kV}$ IEC ESD 保护功能的双电荷泵电路。TRSF3221E 可在异步通信控制器和串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由单个 3V 至 5.5V 电源供电。TRSF3221E 以高达 1Mbit/s 的数据信号传输速率运行, 驱动器输出压摆率为 $24\text{V}/\mu\text{s}$ 至 $150\text{V}/\mu\text{s}$ 。

串行端口处于非活动状态时, 可提供灵活的电源管理控制选项。当 **FORCEON** 为低电平且 **FORCEOFF** 为高电平时, 自动断电功能启用。在这种运行模式下, 如果 TRSF3221E 在接收器输入端未感应到有效的 RS-232 信号, 则会禁用驱动器输出。如果 **FORCEOFF** 设定为低电平且使能 (**EN**) 输入为高电平, 则驱动器和接收器均关闭, 且电源电流降低至 $1\mu\text{A}$ 。断开串行端口的连接或关闭外围驱动器会导致发生自动断电情况。当 **FORCEON** 和 **FORCEOFF** 均为高电平时可禁用自动断电。启用自动断电的情况下, 向接收器输入施加有效信号时, 器件会自动激活。**INVALID** 输出会通知用户接收器输入端是否存在 RS-232 信号。如果接收器输入电压大于 2.7V 或小于 -2.7V , 或者介于 -0.3V 至 0.3V 之间的时间少于 $30\mu\text{s}$, 则 **INVALID** 为高电平 (有效数据)。如果接收器输入电压在 -0.3V 至 0.3V 之间的时间超过 $30\mu\text{s}$, 则 **INVALID** 为低电平 (无效数据)。

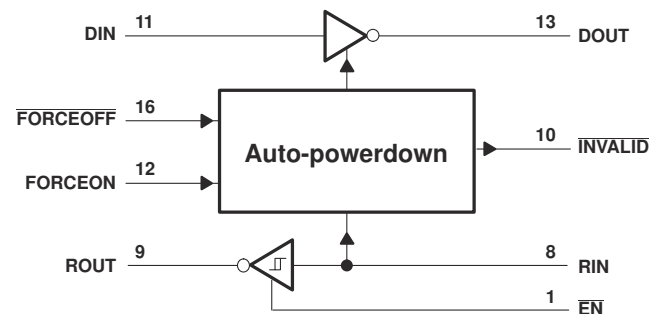
有关接收器输入电平的信息, 请参阅图 6-5。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
TRSF3221E	DB (SSOP)	6.2mm x 5.3mm
	PW (TSSOP)	5mm x 4.4mm
	RGT (VQFN)	3mm x 3mm
	SOT-23-THN (DYY, 16)	4.2mm x 2mm

(1) 有关更多信息, 请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。



逻辑图 (正逻辑)



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4 Pin Configuration and Functions

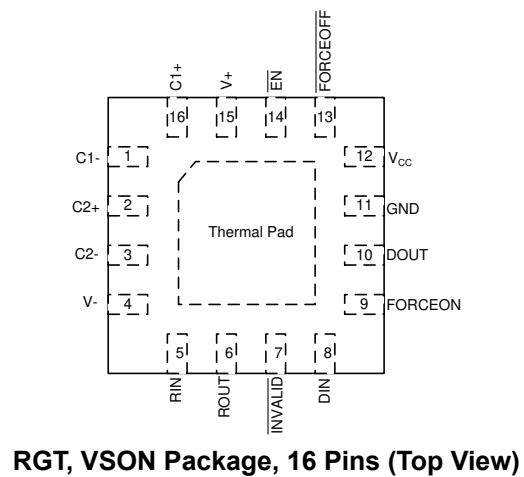
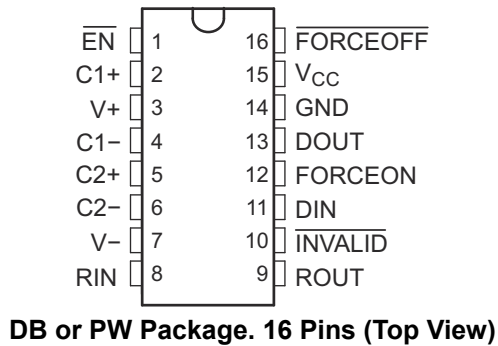


表 4-1. Pin Functions

PIN			TYPE ⁽¹⁾	DESCRIPTION
NAME	DB or PW	RGT		
EN	1	14	--	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
C1+	2	16	-	Positive lead of C1 capacitor
V+	3	15	O	Positive charge pump output for storage capacitor only
C1-	4	1	-	Negative lead of C1 capacitor
C2+	5	2	-	Positive lead of C2 capacitor
C2-	6	3	-	Negative lead of C2 capacitor
V-	7	4	O	Negative charge pump output for storage capacitor only
RIN	8	5	I	RS232 line data input (from remote RS232 system)
ROUT	9	6	O	Logic data output (to UART)
INVALID	10	7		Invalid output pin. Output low when RIN input is unpowered.
DIN	11	8	I	Logic data input (from UART)
FORCEON	12	9		Automatic power-down control input
DOUT	13	10	O	RS232 line data output (to remote RS232 system)
GRD	14	11	-	Ground
V _{CC}	15	12	-	Supply Voltage, Connect to external 3V to 5.5V power supply
FORCEOFF	16	13		Automatic power-down control input
Thermal Pad	-	Yes	-	Exposed thermal pad. Can be connected to GND or left floating.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

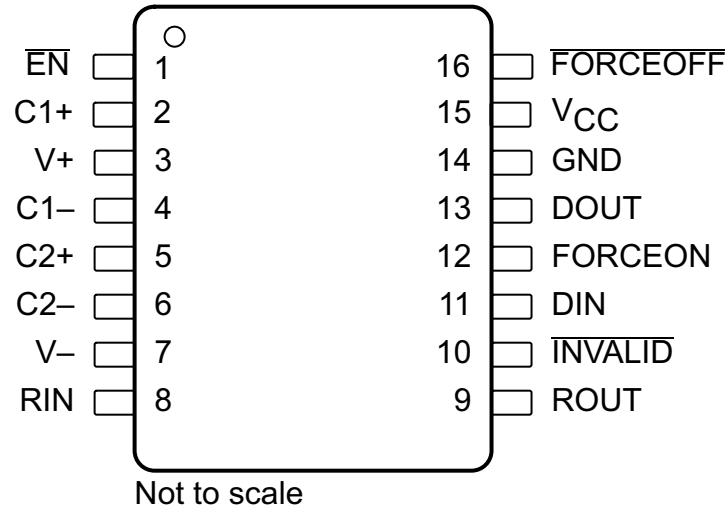


图 4-1. DYY Package
16-Pin SOT-23-THN
(Top View)

表 4-2. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
C1+	2	—	Positive terminals of the voltage-doubler charge pump capacitors
V+	3	O	5.5V supply generated by the charge pump
C1 -	4	—	Negative terminals of the voltage-doubler charge pump capacitors
C2+	5		Positive terminals of the voltage-doubler charge pump capacitors
C2 -	6		Negative terminals of the voltage-doubler charge pump capacitors
V -	7	O	- 5.5V supply generated by the charge pump
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
INVALID	10	O	Invalid output pin. Output low when RIN input is unpowered.
DIN	11	I	Driver input
FORCEON	12	I	Automatic power-down control input
DOUT	13	O	RS-232 driver output
GND	14	—	Ground
V _{CC}	15	—	3V to 5.5V supply voltage
FORCEOFF	16	I	Automatic power-down control input

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) See ⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾		− 0.3	6	V
V+	Positive output supply voltage range ⁽²⁾		− 0.3	7	V
V −	Negative output supply voltage range ⁽²⁾		0.3	− 7	V
V+ − V −	Supply voltage difference ⁽²⁾			13	V
V _I	Input voltage range	Driver (FORCEOFF, FORCEON, EN)	− 0.3	6	V
		Receiver	− 25	25	
V _O	Output voltage range	Driver	− 13.2	13.2	V
		Receiver (INVALID)	− 0.3	V _{CC} + 0.3	
T _J	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		− 65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings, IEC Specifications

PIN NAME	TEST CONDITIONS	VALUE	UNIT
RIN, DOUT ⁽²⁾	HBM	±15,000	V
	IEC 61000-4-2 Contact Discharge ^{(1) (2)}	±8,000	
	IEC 61000-4-2 Air-Gap Discharge ^{(1) (2)}	±15,000	

- (1) For the RGT and PW package only, a minimum of 1μF capacitor is required between VCC and GND to meet the specified IEC-ESD level.
- (2) For optimized IEC ESD performance for DYY package, the recommendation is to have series resistor ($\geq 50\Omega$), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

5.4 Recommended Operating Conditions

See 图 8-1 and (1)

				MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3\text{ V}$		3	3.3	3.6	V
		$V_{CC} = 5\text{ V}$		4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON, EN	$V_{CC} = 3.3\text{ V}$		2		V
			$V_{CC} = 5\text{ V}$		2.4		
V_{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON, EN				0.8	V
V_I	Driver and control input voltage	DIN, FORCEOFF, FORCEON	0			5.5	V
V_I	Receiver input voltage		– 25			25	V
T_A	Operating free-air temperature	TRSF3221EI	– 40			85	°C
		TRSF3221EC	0			70	

(1) Test conditions are $C1 - C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2 - C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

5.5 Thermal Resistance Characteristics

THERMAL METRIC ⁽¹⁾		TRSF3221E				UNIT
		DB (SSOP)	PW (TSSOP)	RGT (VQFN)	DYY (SOT-23-THN)	
		16 Pins	16 Pins	16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82	110.9	58.8	119.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	41.7	55.8	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	57.2	23.8	51.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.0	4.2	1.7	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.8	56.6	23.7	51.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see 图 8-1)

PARAMETER			TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
I_I	Input leakage current	FORCEOFF, FORCEON, EN		± 0.01	± 1		μA
I_{CC}	Supply current ($T_A = 25^\circ\text{C}$)	Auto-powerdown disabled	No load, FORCEOFF and FORCEON at V_{CC}		0.3	1	μA
		Powered off	No load, FORCEOFF at GND		1	10	
		Auto-powerdown enabled	No load, FORCEOFF at V_{CC} , FORCEON at GND, All RIN are open or grounded		1	10	

(1) Test conditions are $C1 - C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2 - C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

5.7 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [图 8-1](#))

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH} High-level output voltage	DOOUT at R _L = 3 kΩ to GND, DIN = GND	5	5.4		V
V _{OL} Low-level output voltage	DOOUT at R _L = 3 kΩ to GND, DIN = V _{CC}	- 5	- 5.4		V
I _{IH} High-level input current	V _I = V _{CC}		±0.01	±1	μ A
I _{IL} Low-level input current	V _I at GND		±0.01	±1	μ A
I _{OS} Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V, V _O = 0 V		±35	±60	mA
	V _{CC} = 5.5 V, V _O = 0 V		±35	±90	
r _o Output resistance	V _{CC} , V ₊ , and V ₋ = 0 V, V _O = ±2 V	300	10M		Ω
I _{off} Output leakage current	FORCEOFF = GND	V _O = ±12 V, V _{CC} = 3 V to 3.6 V		±25	μ A
		V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V		±25	

- (1) Test conditions are C1 - C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2 - C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations must be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output can be shorted at a time.

5.8 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [图 8-1](#))

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
Maximum data rate (see 图 6-1)	R _L = 3 kΩ	C _L = 1000 pF	250		kbit/s
		C _L = 250 pF, V _{CC} = 3 V to 4.5 V	1000		
		C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V	1000		
t _{sk(p)} Pulse skew ⁽³⁾	C _L = 250 pF	R _L = 3 kΩ 图 6-2	RGT Package	25	ns
	C _L = 150 pF to 2500 pF,	R _L = 3 kΩ to 7 kΩ, See 图 6-2	DB or PW package	100	
SR(tr) Slew rate, transition region (see 图 6-1)	V _{CC} = 3.3 V,	R _L = 3 kΩ to 7 kΩ, C _L = 150 pF to 1000 pF	18	150	V/ μ s

- (1) Test conditions are C1 - C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2 - C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

5.9 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see 图 8-1)

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6 V	V _{CC} - 0.1 V		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		V
I _{off}	Output leakage current	FORCEOFF = 0 V		±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

5.10 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see 图 8-1)

PARAMETER		TEST CONDITIONS ⁽¹⁾		TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See 图 6-3	RGT package	100	ns
			DB or PW package	150	
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See 图 6-3	RGT package	125	ns
			DB or PW package	150	
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See 图 6-4		200	ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 kΩ, See 图 6-4		200	ns
t _{sk(p)}	Pulse skew ⁽³⁾	See 图 6-3	RGT package	25	ns
			DB or PW package	50	

(1) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

5.11 Electrical Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see 图 6-5)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+}(\text{valid})$ Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}		2.7	V
$V_{T-}(\text{valid})$ Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}	- 2.7		V
$V_{T}(\text{invalid})$ Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}	- 0.3	0.3	V
V_{OH} INVALID high-level output voltage	$I_{OH} = -1\text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}	$V_{CC} - 0.6$		V
V_{OL} INVALID low-level output voltage	$I_{OL} = 1.6\text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}		0.4	V

5.12 Switching Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see 图 6-5)

PARAMETER	TYP ⁽¹⁾	UNIT
t_{valid} Propagation delay time, low- to high-level output	1	$\mu\text{ s}$
t_{invalid} Propagation delay time, high- to low-level output	30	$\mu\text{ s}$
t_{en} Supply enable time	100	$\mu\text{ s}$

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

5.13 Typical Characteristics

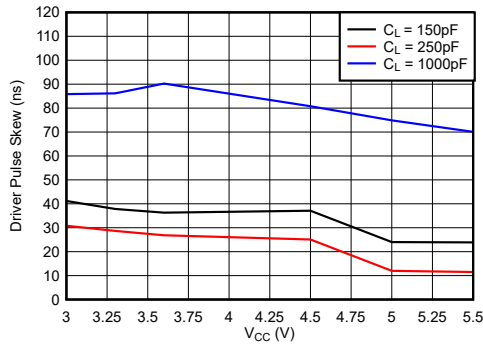


图 5-1. Driver Pulse Skew vs Load Capacitance and Supply Voltage at $T_A = 25^\circ\text{C}$ (RGT Package)

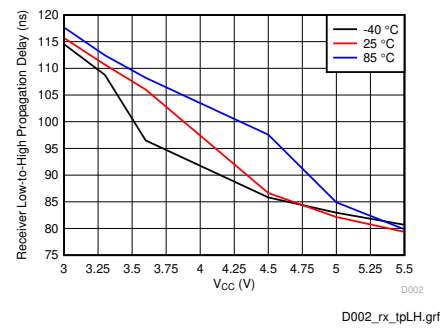


图 5-2. Receiver Path Low-to-High Propagation Delay vs T_A and Supply Voltage (RGT Package)

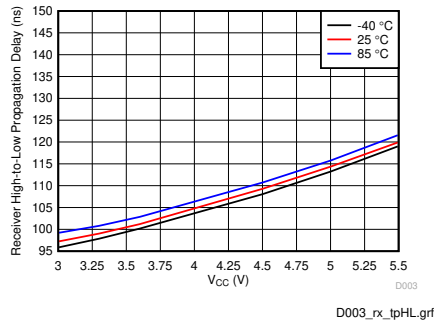


图 5-3. Receiver Path High-to-Low Propagation Delay vs T_A and Supply Voltage (RGT Package)

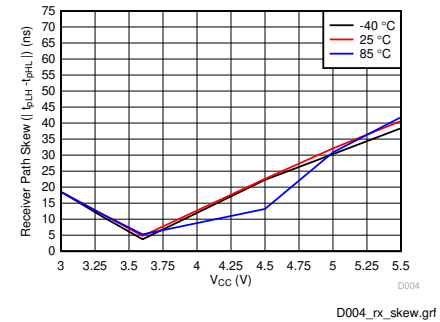
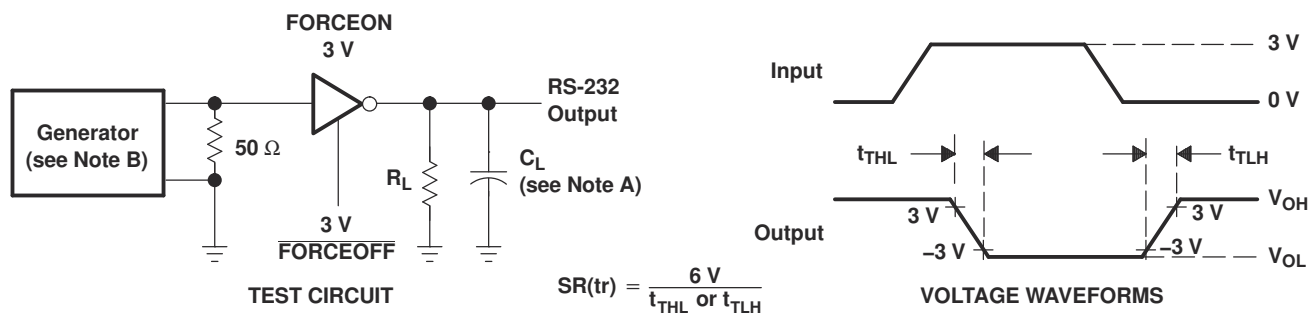


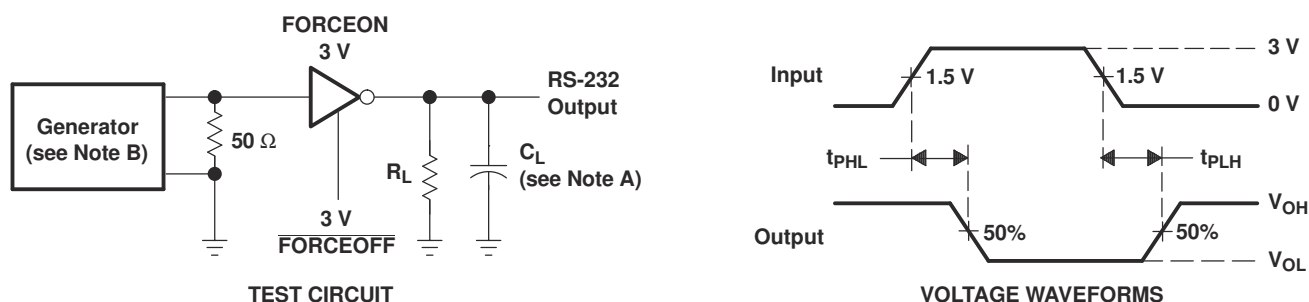
图 5-4. Receiver Pulse Skew ($t_{pLH} - t_{pHL}$) vs T_A and Supply Voltage (RGT Package)

6 Parameter Measurement Information



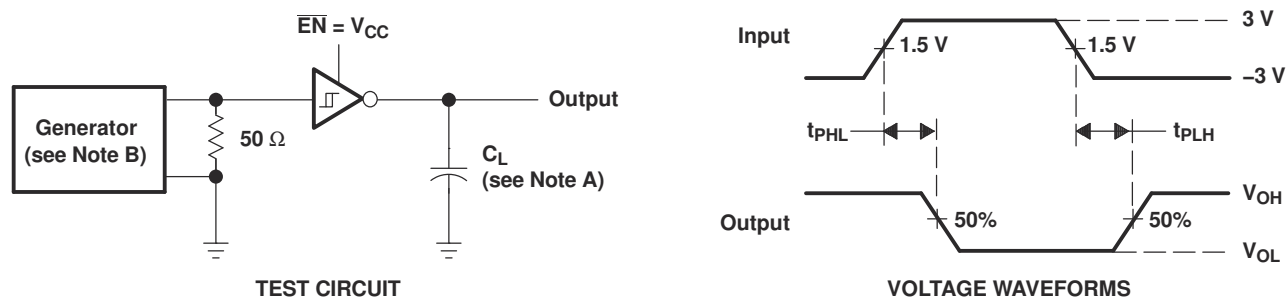
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 6-1. Driver Slew Rate



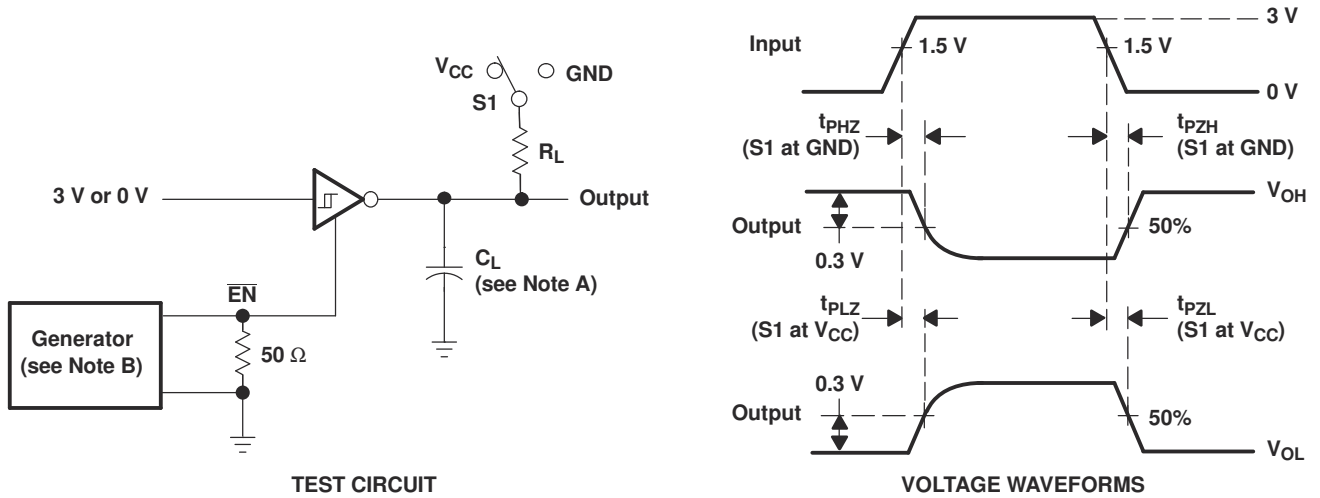
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 6-2. Driver Pulse Skew



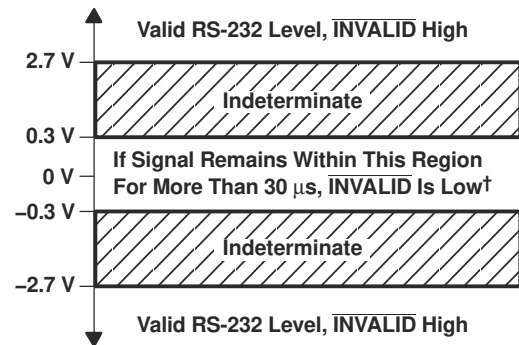
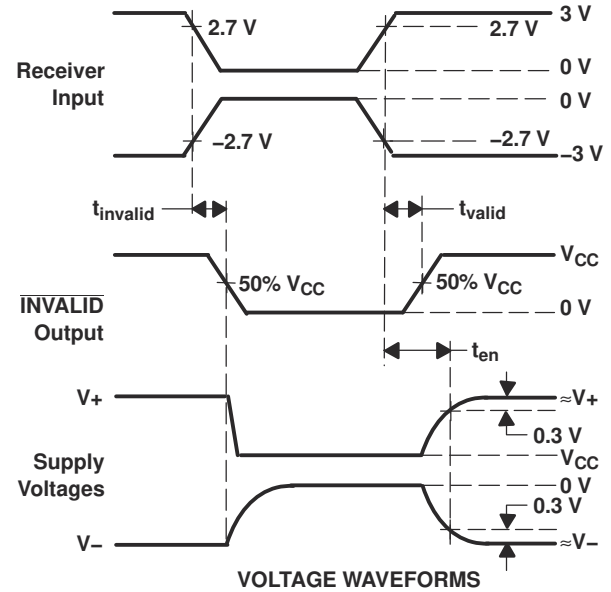
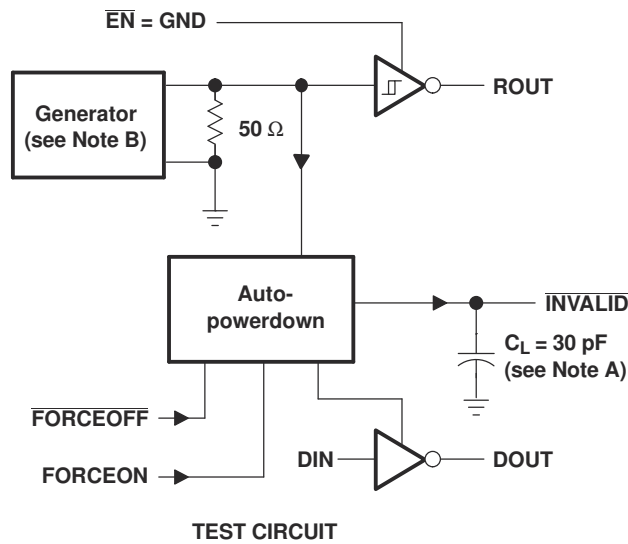
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 6-3. Receiver Propagation Delay Times



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.
 - C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - D. t_{PZL} and t_{PZH} are the same as t_{en} .

图 6-4. Receiver Enable and Disable Times



† Auto-powerdown disables drivers and reduces supply current to 1 μA .

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

图 6-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Driver Enabling Time

7 Detailed Description

7.1 Overview

The TRSF3221E consists of one line driver, one line receiver, and a dual charge-pump circuit with $\pm 15\text{kV}$ IEC ESD protection pin to pin (serial-port connection pins, including GND). The TRSF3221E provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. The TRSF3221E operates at data signaling rates up to 1Mbit/s and a driver output slew rate of $24\text{V}/\mu\text{s}$ to $150\text{V}/\mu\text{s}$.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when $\overline{\text{FORCEON}}$ is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the TRSF3221E does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If $\overline{\text{FORCEOFF}}$ is set low and the enable ($\overline{\text{EN}}$) input is high, both the driver and receiver are shut off, and the supply current is reduced to $1\mu\text{A}$. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to the receiver input. The $\overline{\text{INVALID}}$ output notifies the user if an RS-232 signal is present at the receiver input. $\overline{\text{INVALID}}$ is high (valid data) if the receiver input voltage is greater than 2.7V or less than -2.7V , or has been between -0.3V and 0.3V for less than $30\mu\text{s}$. $\overline{\text{INVALID}}$ is low (invalid data) if the receiver input voltage is between -0.3V and 0.3V for more than $30\mu\text{s}$. Outputs are protected against shorts to ground.

7.2 Functional Block Diagram

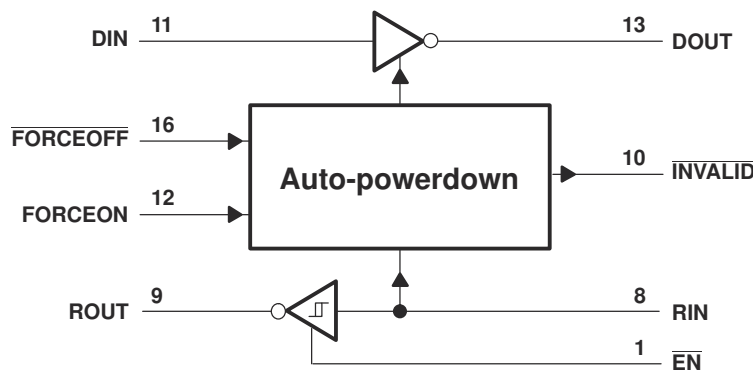


图 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

The power block increases, inverts, and regulates voltage at V^+ and V^- pins using a charge pump that requires four external capacitors. Auto-power-down feature for driver is controlled by $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ inputs. Receiver is controlled by $\overline{\text{EN}}$ input. When MAX3221E is unpowered, it can be safely connected to an active remote RS-232 device.

The driver interfaces the standard logic level to RS232 voltage levels. The DIN input must be valid high or low.

The receiver interfaces RS-232 levels to standard logic levels. An open input results in a high output on ROUT. RIN input includes an internal standard RS-232 load. A logic high input on the $\overline{\text{EN}}$ pin shuts down the receiver output.

7.4 Device Functional Modes

Functional Tables, Each Driver

INPUTS ⁽¹⁾				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver

INPUTS ⁽¹⁾			OUTPUT ROUT
RIN	EN	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

8 Application and Implementation

备注

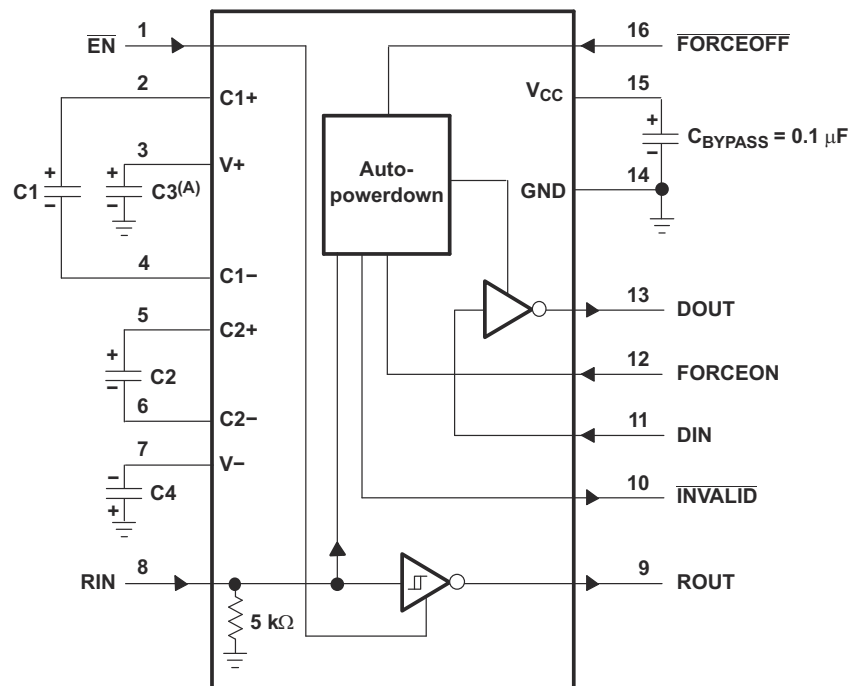
以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TRSF3221E line driver and receiver is a specialized device for 3V to 5.5V RS-232 communication applications. This application is a generic implementation of this device with all required external components. For proper operation, add capacitors as shown in 表 8-1.

8.1.1 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and FORCEOFF may be connected to general purpose logic lines or tied to ground or VCC. INVALID may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS-232 connector or cable. DIN, FORCEON, and FORCEOFF inputs must not be left unconnected.



- A. C3 can be connected to V_{CC} or GND.
- B. Resistor values shown are nominal.
- C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.

图 8-1. Typical Operating Circuit and Capacitor Values

表 8-1. V_{CC} vs Capacitor Values

V _{CC}	C1	C2, C3, C4
3.3V ± 0.3V	0.1μF	0.1μF
5V ± 0.5V	0.047μF	0.33μF
3V to 5.5V	0.1μF	0.47μF

8.1.1.1 Design Requirements

- Recommended VCC is 3.3V or 5V - 3V to 5.5V is also possible
- Maximum recommended bit rate is 1Mbps
- Use capacitors as shown in 图 8-1 and 表 8-1

8.1.1.2 Detailed Design Procedure

For proper operation:

- DIN, FORCEOFF and FORCEON inputs must be connected to valid low or high logic levels
- Select capacitor values based on VCC level for best performance

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and FORCEOFF may be connected general purpose logic lines or tied to ground or VCC. INVALID may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS232 connector or cable. DIN, FORCEON, and FORCEOFF inputs must not be left unconnected.

8.1.2 Application Performance Plot

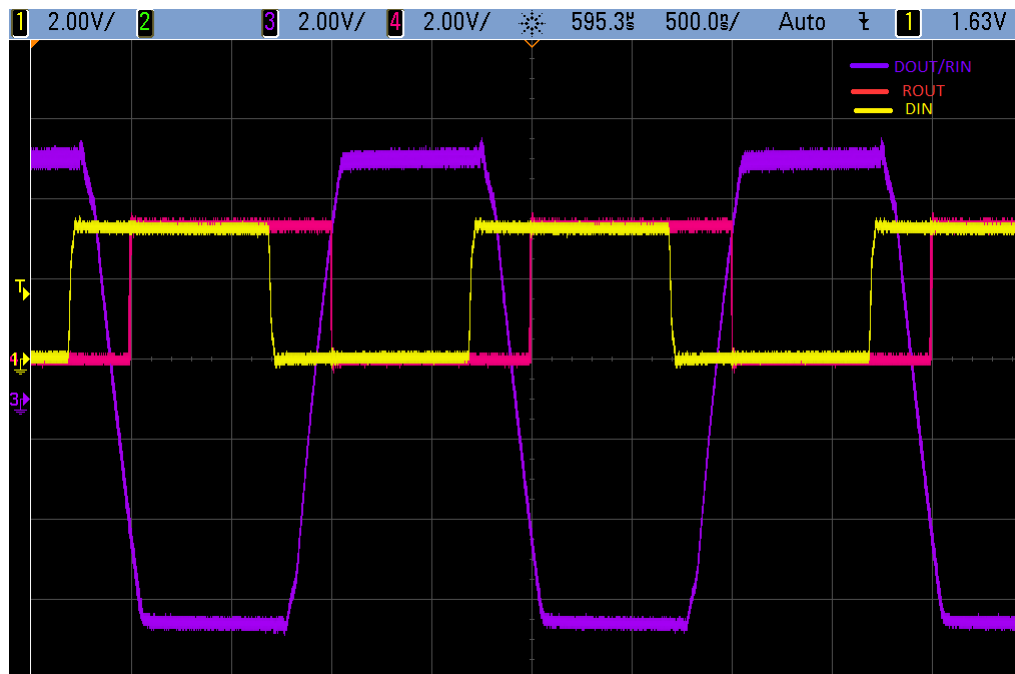


图 8-2. 1 Mbps Driver to Receiver Loopback Timing Waveform, VCC = 3.3 V

8.2 Power Supply Recommendations

VCC must be between 3V and 5.5V. Charge pump capacitors must be chosen using [VCC vs Capacitor Values](#).

8.3 Layout

8.3.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes, which have the fastest rise and fall times.

8.3.2 Layout Example

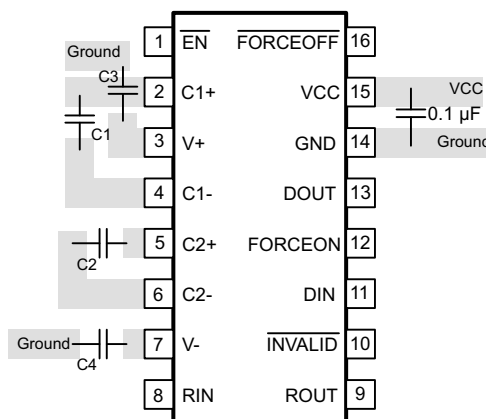


图 8-3. Layout Diagram

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.3 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (July 2021) to Revision C (December 2024)	Page
• 将 <i>器件信息</i> 表更改为 <i>封装信息</i> 表.....	1
• 向数据表中添加了 SOT-23-THN (DYY) 封装.....	1
• Added Note 2 to the <i>ESD Ratings, IEC Specifications</i>	5

Changes from Revision A (May 2021) to Revision B (July 2021)	Page
• 更改了 <i>应用</i> 列表.....	1
• Changed the table note for the <i>ESD Ratings, IEC Specifications</i> table to make it also applicable to PW package.....	5
• Changed the thermal information for PW package.....	6

Changes from Revision * (August 2007) to Revision A (May 2021)	Page
• 添加了“器件信息”表、“ESD 等级”表、“特性说明”部分、“器件功能模式”、“应用和实施”部分、“电源相关建议”部分、“布局”部分、“器件和文档支持”部分以及“机械、封装和可订购信息”部分.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRSF3221ECDB	Obsolete	Production	SSOP (DB) 16	-	-	Call TI	Call TI	0 to 70	RT21EC
TRSF3221ECDBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC
TRSF3221ECDBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC
TRSF3221ECPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	RT21EC
TRSF3221ECPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC
TRSF3221EIDBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI
TRSF3221EIDBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI
TRSF3221EIDYYR	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI
TRSF3221EIDYYR.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI
TRSF3221EIPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	RT21EI
TRSF3221EIPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI
TRSF3221EIRGTR	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	F3221
TRSF3221EIRGTR.A	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	F3221

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

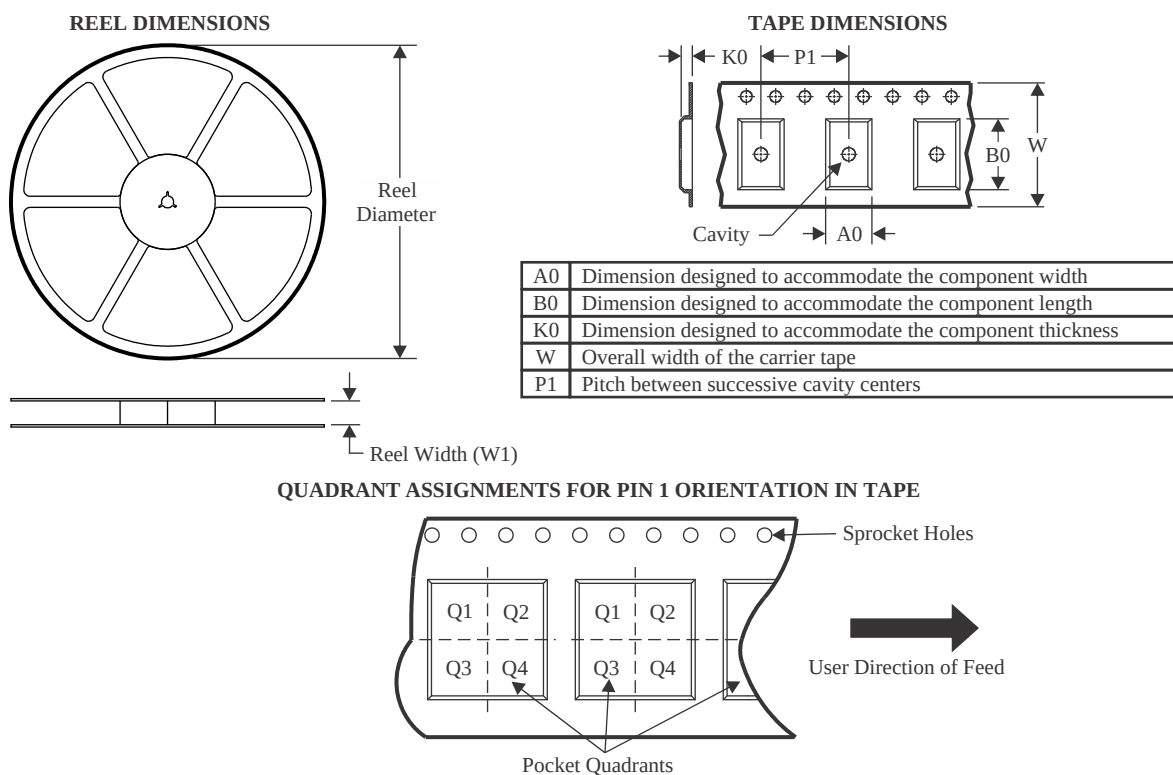
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

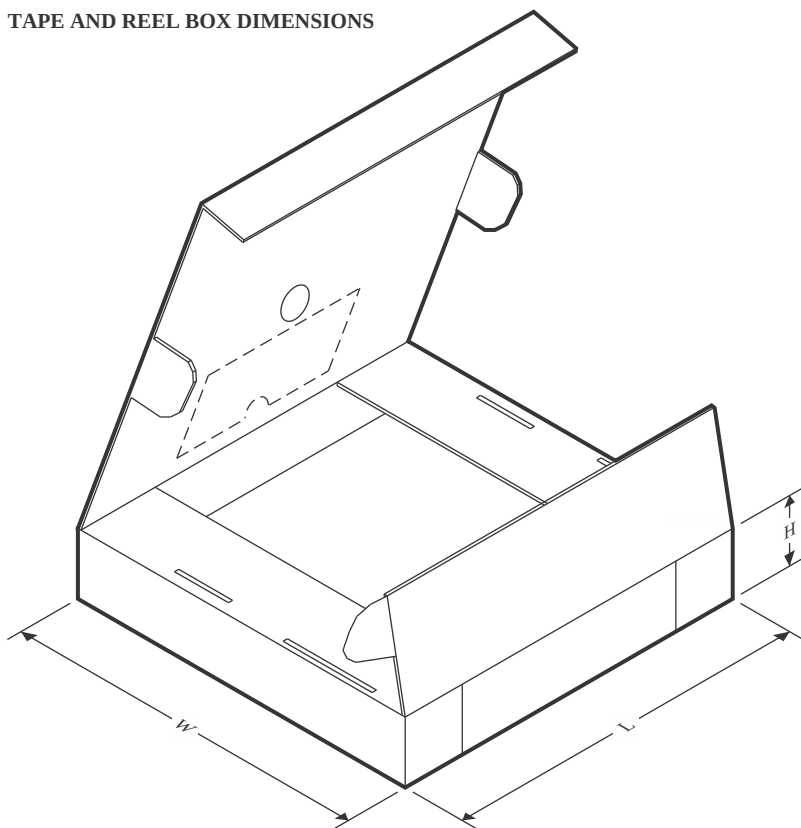
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3221ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRSF3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRSF3221EIDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TRSF3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

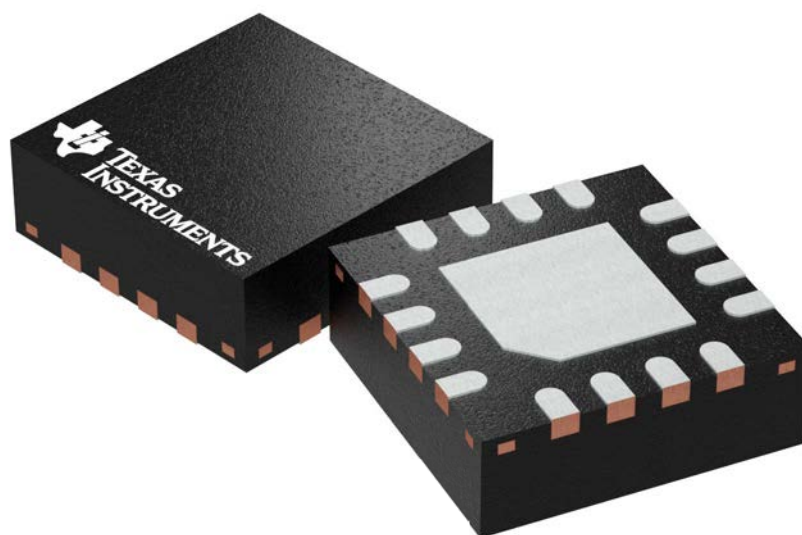
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3221ECDBR	SSOP	DB	16	2000	353.0	353.0	32.0
TRSF3221ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3221EIDBR	SSOP	DB	16	2000	353.0	353.0	32.0
TRSF3221EIDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TRSF3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3221EIRGTR	VQFN	RGT	16	3000	360.0	360.0	36.0

RGT 16

GENERIC PACKAGE VIEW

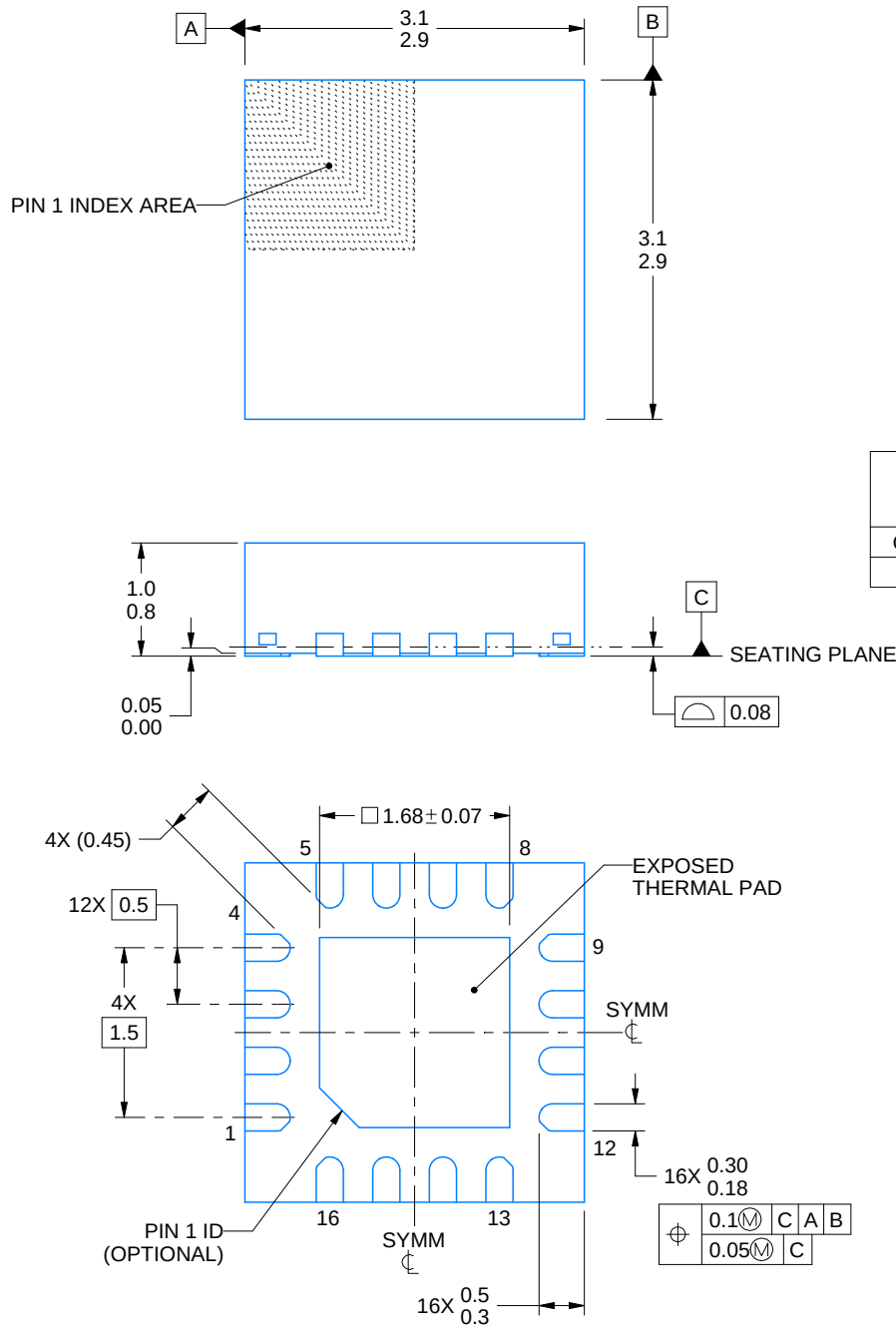
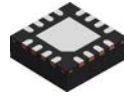
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



4222419/E 07/2025

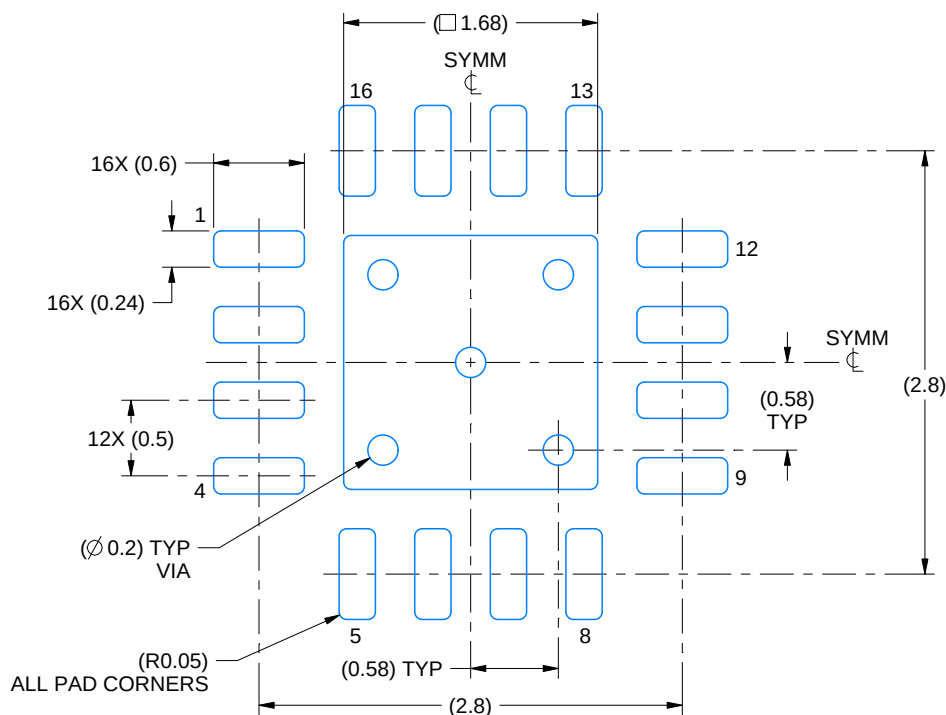
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

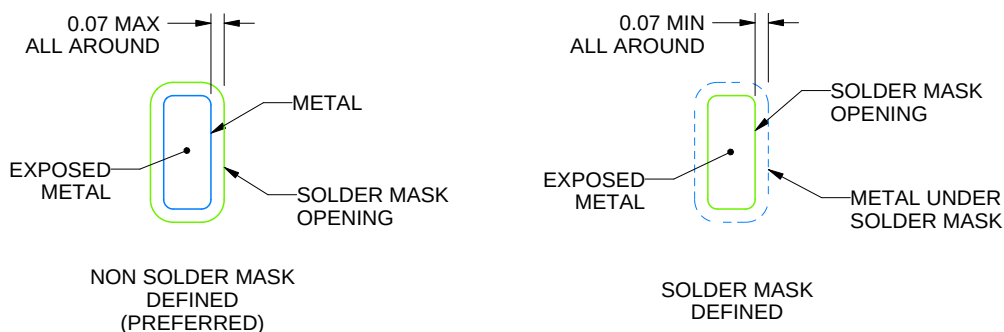
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222419/E 07/2025

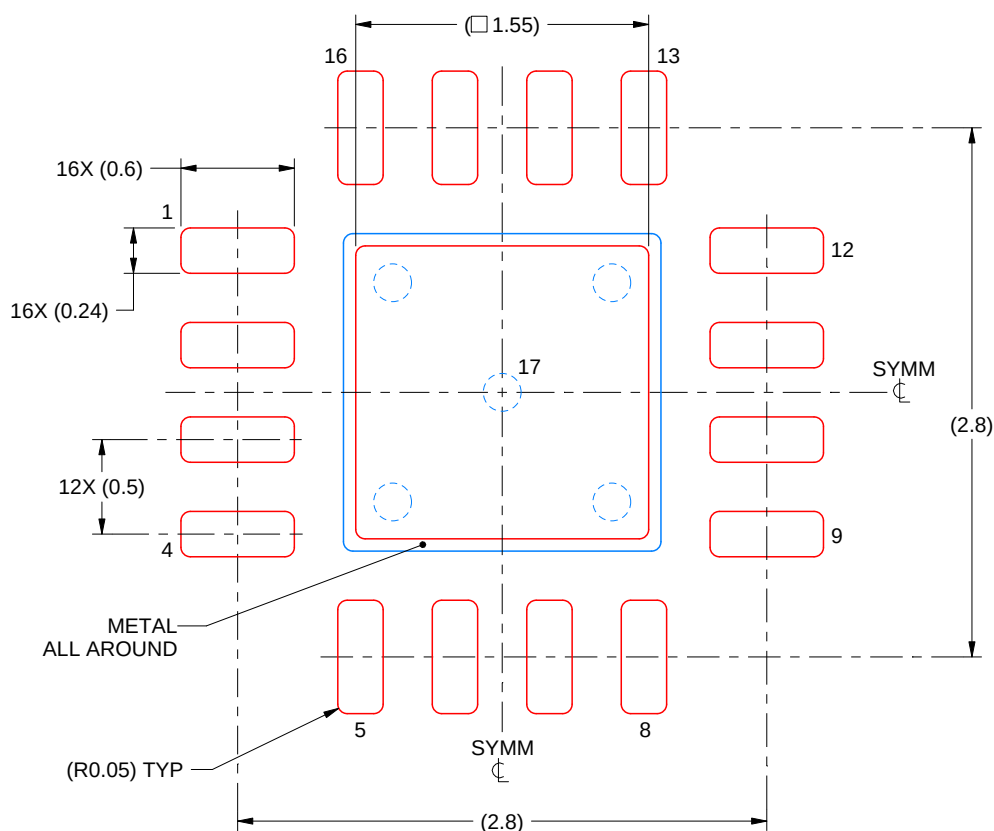
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

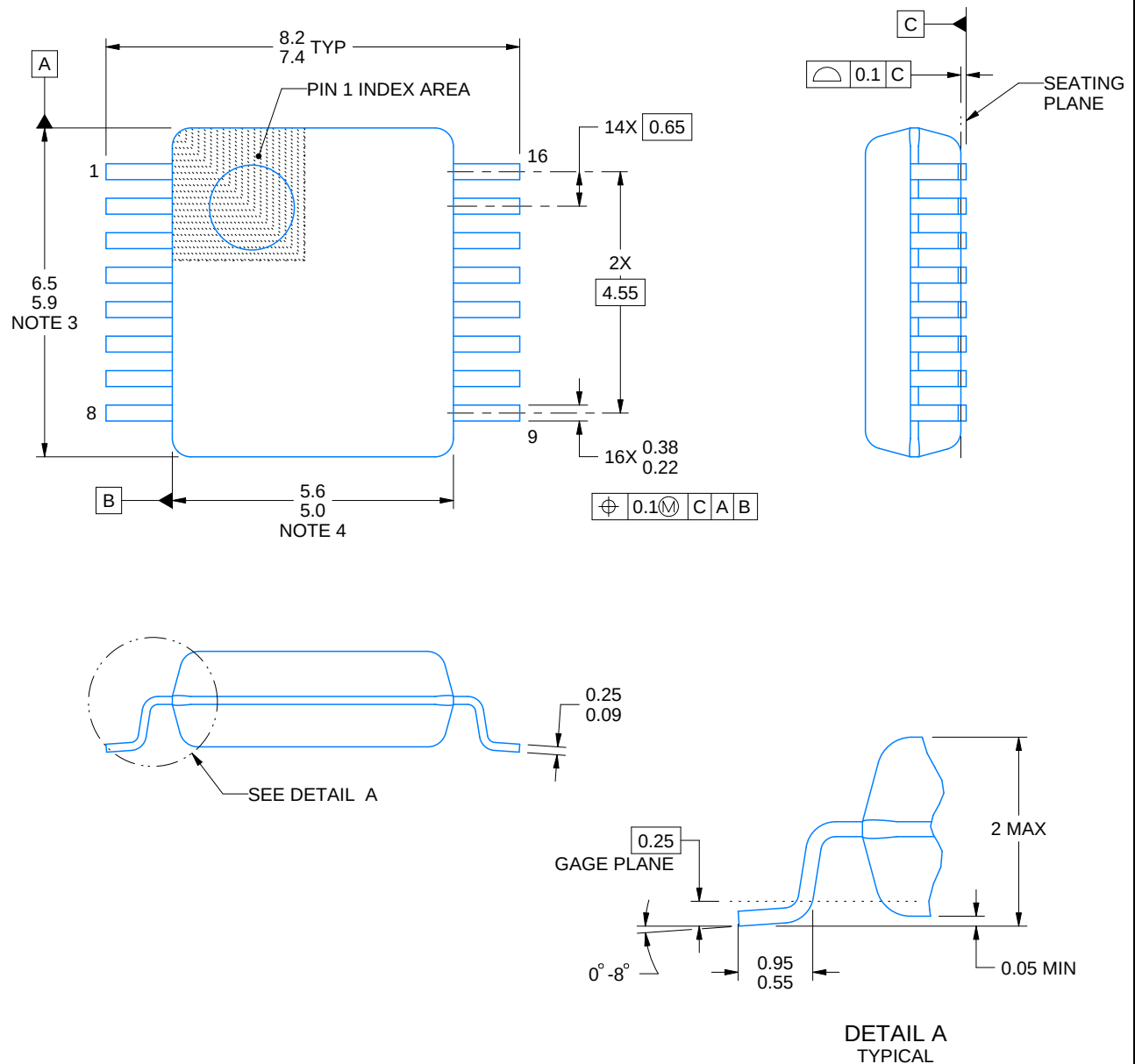
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DB0016A

PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

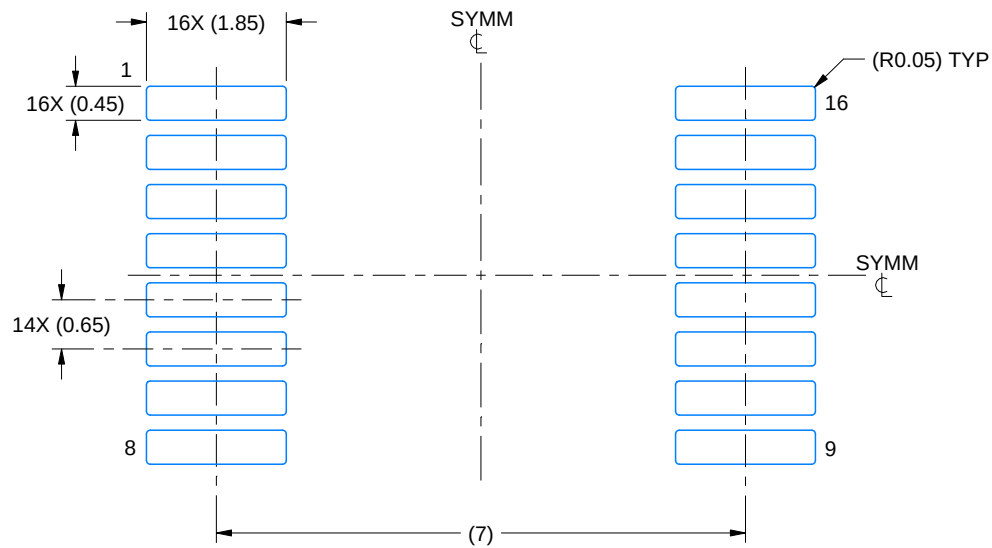
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

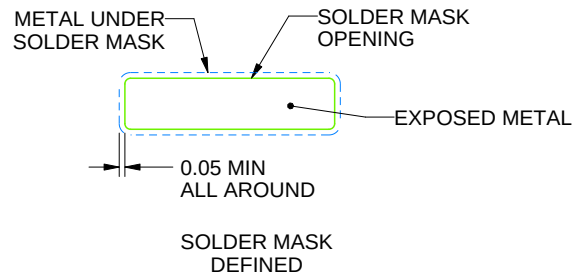
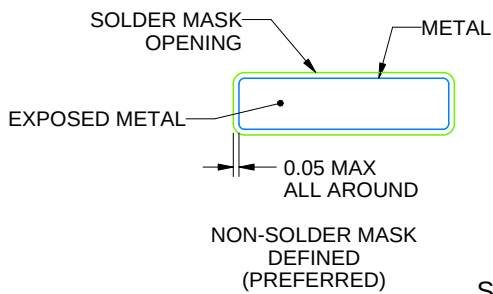
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

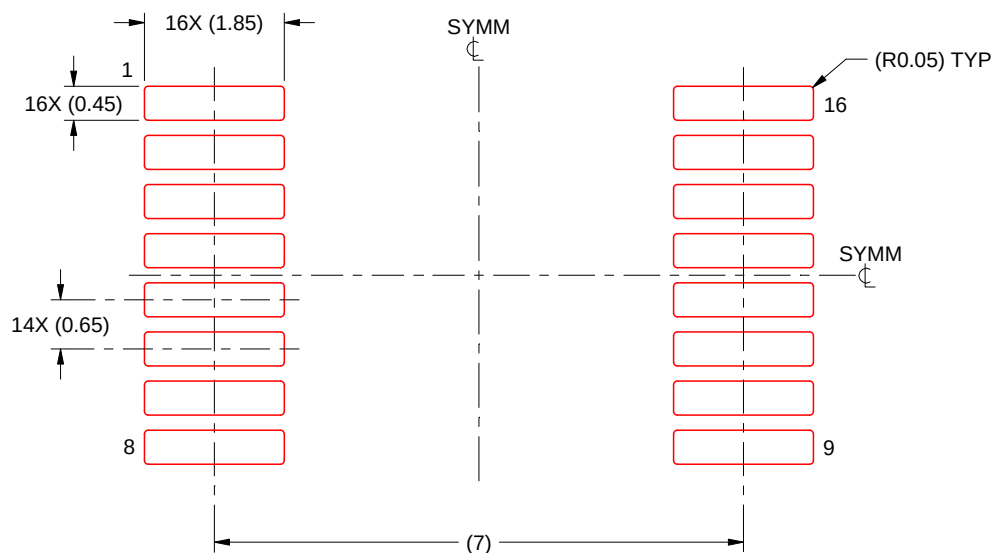
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

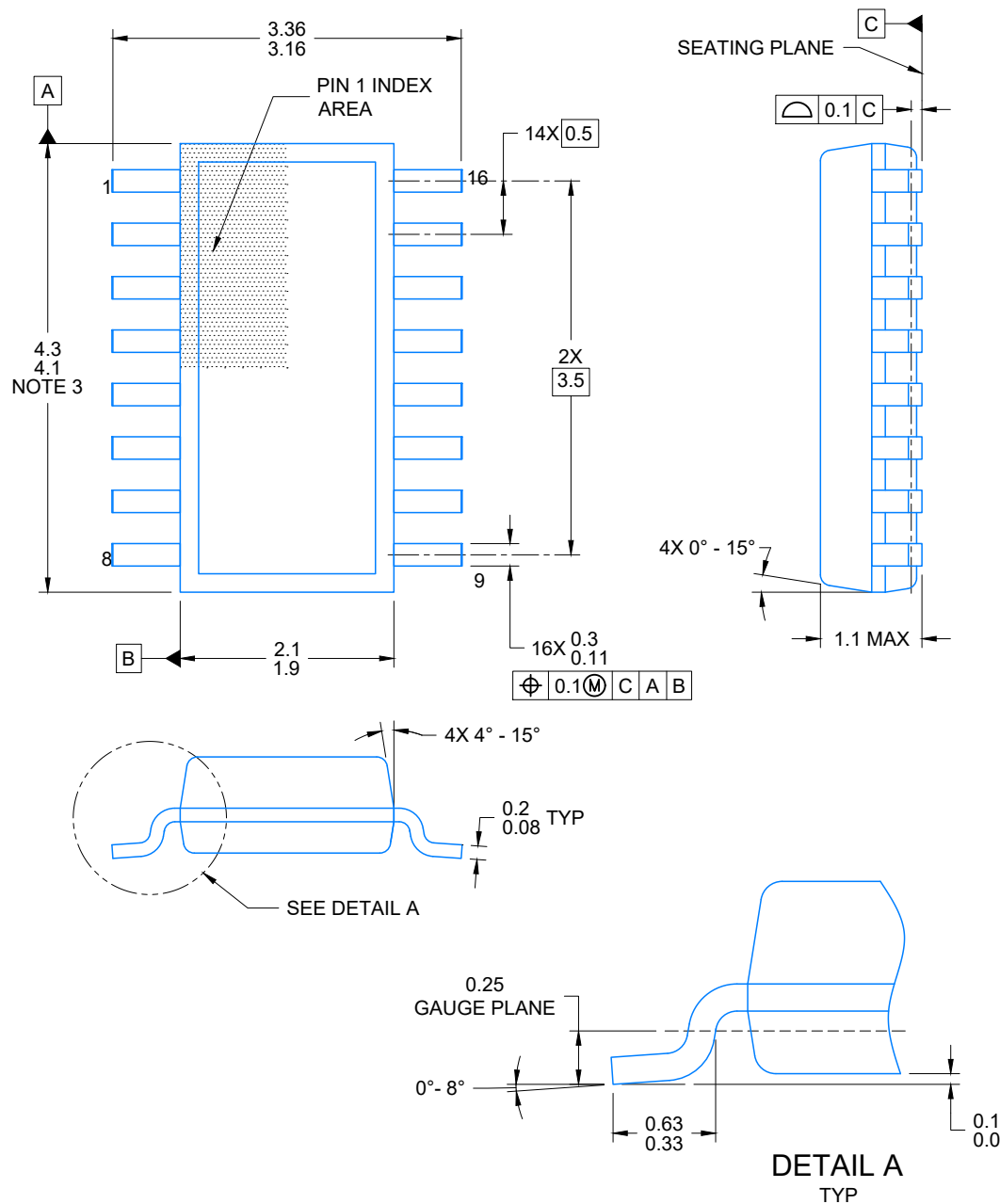


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

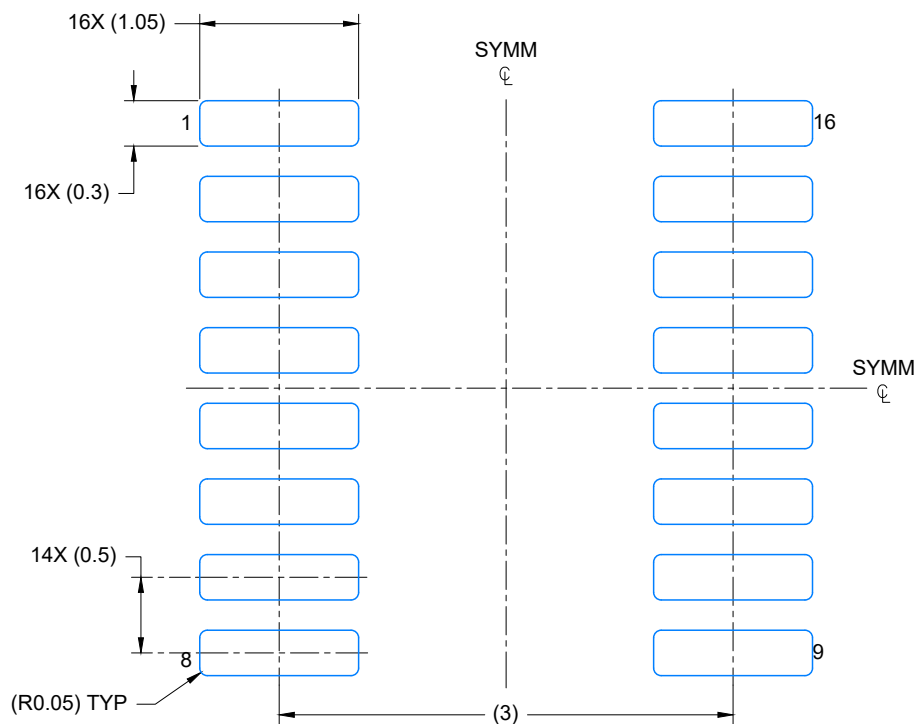
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



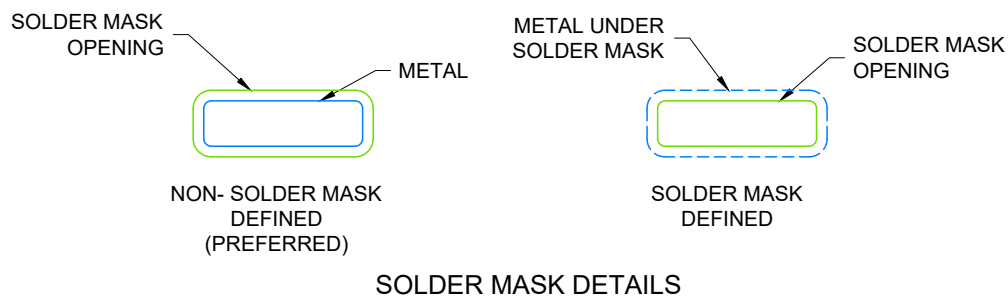
4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



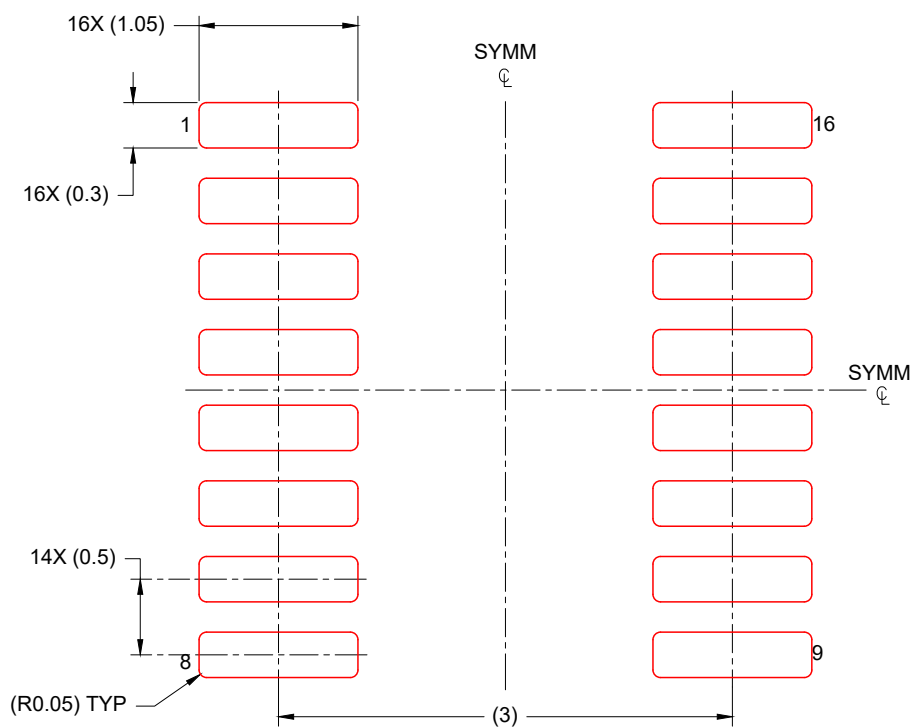
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224642/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

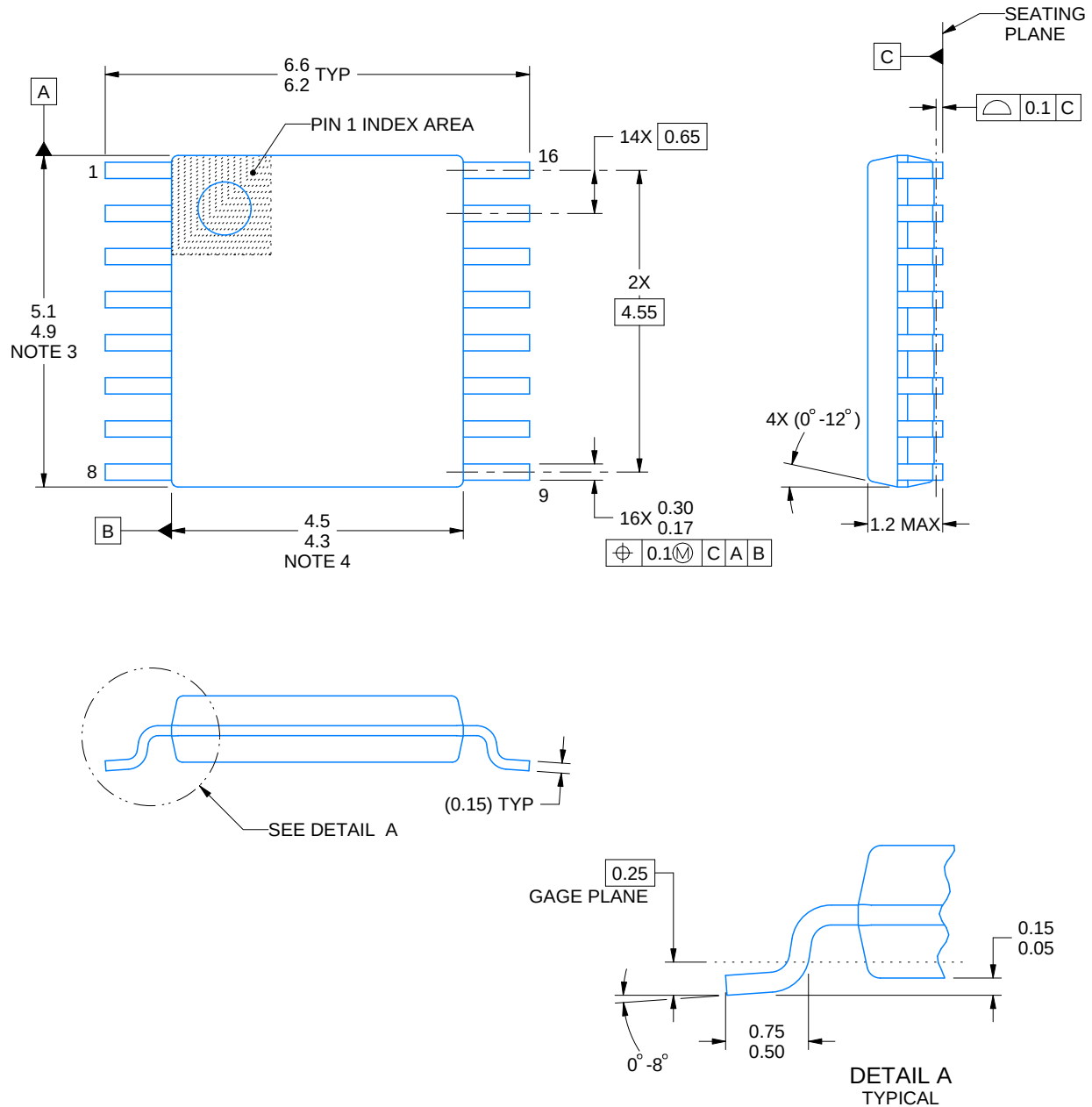
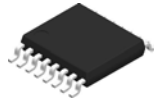


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220204/B 12/2023

NOTES:

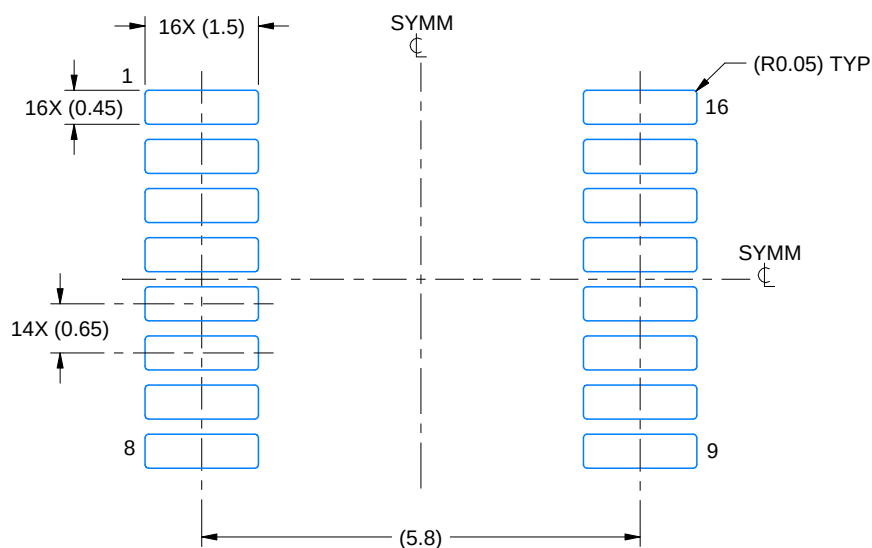
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

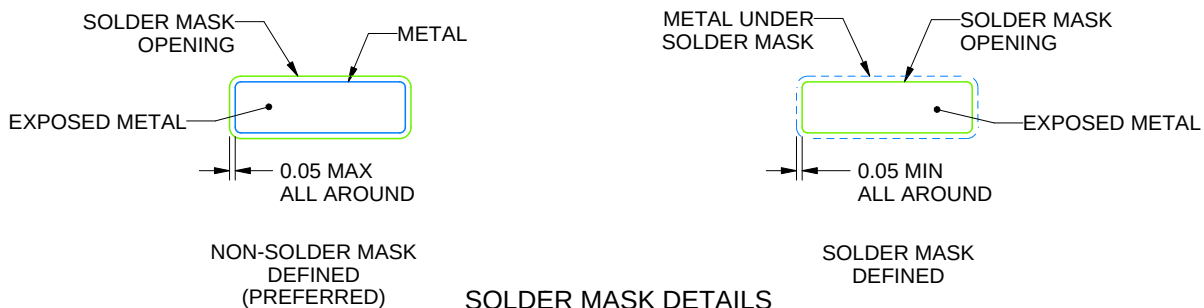
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

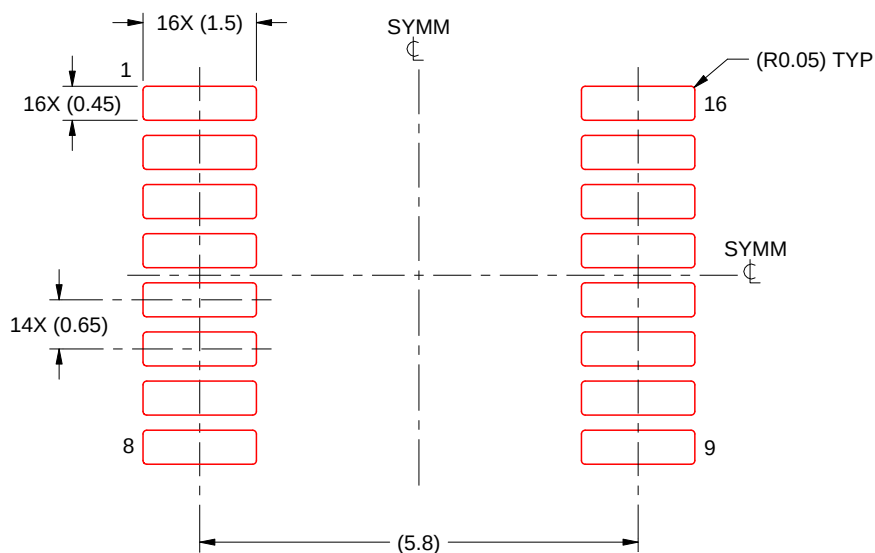
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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