

# TRF7962A 全集成 13.56MHz RFID 读/写器 IC (符合 ISO/IEC 15693 和 ISO/IEC 18000-3 标准)

## 1 器件概述

### 1.1 特性

- 完全集成了 ISO/IEC 15693 和 ISO/IEC 18000-3 的协议处理
- 输入电压范围: 2.7VDC 至 5.5VDC
- 可编程输出功率:  
+20 dBm (100 mW) 或者 +23 dBm (200 mW)
- 可编程 I/O 电压电平:  
1.8 VDC 至 5.5 VDC
- 可编程系统时钟频率输出 (RF, RF/2, RF/4)
- 可编程调制深度
- 具有针对“读取漏洞”消除和邻近读取器系统或者周围环境频带内噪声检测的具有接收信号强度指示器 (RSSI) 的双接收器架构
- 适用于超低功耗系统设计的可编程功耗模式 (关断时  $< 0.5\mu\text{A}$ )
- 并行或者串行外设接口 (SPI) 接口
- 用于微控制器电源的集成型电压稳压器
- 温度范围:  $-25^{\circ}\text{C}$  至  $85^{\circ}\text{C}$
- 32 引脚 QFN 封装 (5mm × 5mm) (RHB)

### 1.2 应用

- 产品认证
- 存取控制
- 数字门锁
- 图书馆管理
- 医疗系统
- 远程传感器 应用

### 1.3 说明

TRF7962A 器件是集成式模拟前端 (AFE) 和数据成帧器件, 适用于 13.56MHz RFID 读/写器系统, 支持 ISO/IEC 15693。该器件具有内置的编程选项, 因此适合于广泛的接近和附近识别系统应用。

通过在控制寄存器内选择所需的协议可对此读取器进行配置。到所有控制寄存器的直接存取可根据需要对不同的读取器参数进行微调。

TRF7962A 器件针对所有符合板载 ISO 协议的成帧和同步任务, 支持 6kbps 和 26kbps 的数据速率。此器件还支持 NFC 论坛标签类型 5 的读/写器模式。为了支持 NFC 论坛标签类型 5, 该器件允许在直接模式 2 下使用内置协议解码器。NFC 论坛标签类型 1 要求使用直接模式 0。其它标准和自定义协议也可通过使用直接模式 0 来实现。直接模式 0 可让用户完全控制 AFE, 并且还可以访问原始子载波数据或者未成帧但已经是 ISO 格式的数据和相关 (提取的) 时钟信号。

接收器系统具有双输入接收器架构, 可最大程度实现通信稳定。这些接收器还包括多种自动和手动增益控制选项。在 RSSI 寄存器中可获取从应答器、周围信号源或者内部电平接收到的信号强度。

可使用 SPI 或并行接口进行 MCU 和 TRF7962A 读取器间的通信。当使用内置的硬件编码器和解码器的时候, 发射和接收功能使用一个 12 字节 FIFO 寄存器。对于直接发射或者接收功能, 由于编码器或者解码器可被旁路绕开, 所以 MCU 可实时的处理数据。

TRF7962A 器件支持 2.7V 至 5.5V 的宽电源电压范围以及 MCU I/O 接口的 1.8V 至 5.5V 数据通信电平。

当使用 5V 电源时, 发送器对于 50Ω 负载具有 100mW (+20dBm) 或 200mW (+23dBm) 等效值的可选输出功率电平, 并支持可选调制深度的 OOK 和 ASK 调制。

内置的可编程辅助稳压器为 MCU 和读取器系统内的其他外部电路提供高达 20mA 的电源。

使用 TRF7962A 收发器 IC 超集器件的 [TRF7960AEVM](#) 或 [TRF7960ATB](#) 即可开始评估该器件。

[文档](#), [工具](#)、[参考设计和软件](#), [样片](#)



| 器件信息 <sup>(1)</sup> |           |           |
|---------------------|-----------|-----------|
| 器件型号                | 封装        | 封装尺寸      |
| TRF7962ARHB         | VQFN (32) | 5mm x 5mm |

(1) 有关更多信息，请参阅节 9“机械、封装和可订购信息”。

1.4 应用框图

图 1-1 显示了典型应用框图。

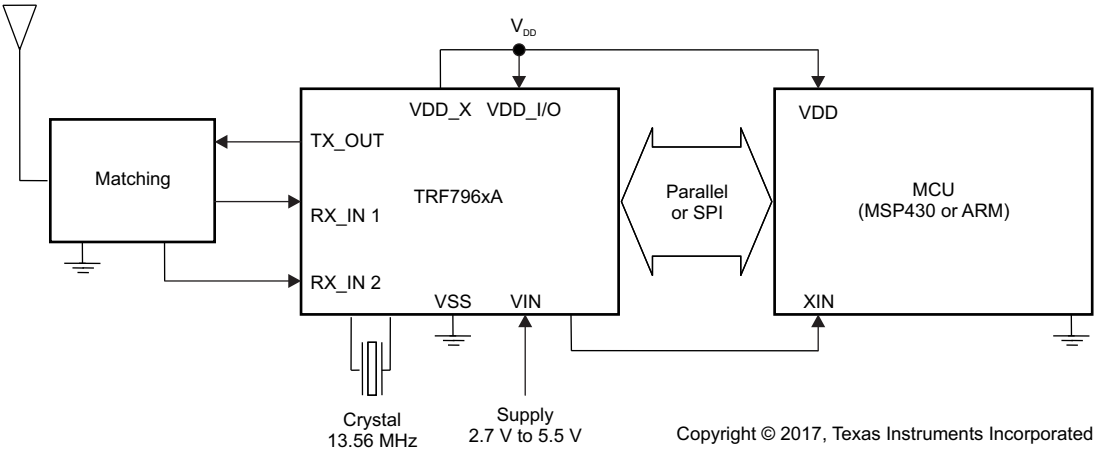


图 1-1. 应用框图

## 内容

|          |                                             |                           |          |                                                               |                           |
|----------|---------------------------------------------|---------------------------|----------|---------------------------------------------------------------|---------------------------|
| <b>1</b> | <b>器件概述</b>                                 | <b><a href="#">1</a></b>  | 6.6      | Receiver – Analog Section                                     | <a href="#">17</a>        |
| 1.1      | 特性                                          | <a href="#">1</a>         | 6.7      | Receiver – Digital Section                                    | <a href="#">18</a>        |
| 1.2      | 应用                                          | <a href="#">1</a>         | 6.8      | Oscillator Section                                            | <a href="#">21</a>        |
| 1.3      | 说明                                          | <a href="#">1</a>         | 6.9      | Transmitter - Analog Section                                  | <a href="#">22</a>        |
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| 4.1      | Pin Diagrams                                | <a href="#">6</a>         | <b>7</b> | <b>Applications, Implementation, and Layout</b>               | <b><a href="#">58</a></b> |
| 4.2      | Signal Descriptions                         | <a href="#">6</a>         | 7.1      | TRF7962A Reader System Using SPI With SS Mode                 | <a href="#">58</a>        |
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| 6.5      | Power Modes                                 | <a href="#">14</a>        |          |                                                               |                           |

## 2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| Changes from January 7, 2015 to May 17, 2017                                                                                                                                                                         | Page      |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| • 更新了节 1.3“说明”的内容 .....                                                                                                                                                                                              | <u>1</u>  |
| • 将图 1-1“应用框图”移到节 1.4，并删除了功能框图（请参阅Section 6.1中的框图） .....                                                                                                                                                             | <u>2</u>  |
| • Added Section 3, <i>Device Characteristics</i> , and moved Table 3-1 to it .....                                                                                                                                   | <u>5</u>  |
| • Added Section 3.1, <i>Related Products</i> .....                                                                                                                                                                   | <u>5</u>  |
| • Changed the TYP value of the $f_{D\_CLKmax}$ parameter from 8 MHz to 4 MHz in Section 5.4, <i>Electrical Characteristics</i> ...                                                                                   | <u>9</u>  |
| • Removed the sentence "This mechanism must be used to avoid reading holes" in the paragraph that starts "The default MUX setting is RX_IN1 connected..." in Section 6.6.1, <i>Main and Auxiliary Receiver</i> ..... | <u>17</u> |
| • Removed paragraphs starting with "The main receiver also has a second receiver gain..." and "By default, the AGC is frozen..." in Section 6.6.2, <i>Receiver Gain and Filter Stages</i> .....                      | <u>17</u> |
| • Changed B1 and B0 to Reserved in Table 6-4, <i>RX Special Setting Register (0x0A)</i> .....                                                                                                                        | <u>18</u> |
| • Updated the first four paragraphs of Section 6.7, <i>Receiver - Digital Section</i> .....                                                                                                                          | <u>18</u> |
| • Updated the first three steps in the procedure that follows "To check the internal or external RSSI value..." in Section 6.7.1.2, <i>External RSSI</i> .....                                                       | <u>21</u> |
| • Changed the title of Table 6-5 from <i>Minimum Crystal Requirements</i> to <i>Minimum Crystal Recommendations</i> and removed the ESR row .....                                                                    | <u>22</u> |
| • Updated the list that follows "There are two ways to start the transmit operation" in Section 6.10, <i>Transmitter - Digital Section</i> .....                                                                     | <u>23</u> |
| • Updated the description in Section 6.11, <i>Transmitter – External Power Amplifier or Subcarrier Detector</i> .....                                                                                                | <u>23</u> |
| • Updated the paragraph that starts "If the received packet is longer than 8 bytes..." in Section 6.12.4, <i>Reception of Air Interface Data</i> .....                                                               | <u>29</u> |
| • Updated the paragraph that starts "TI recommends resetting the FIFO after..." in Section 6.12.6.2, <i>Serial Interface Mode With Slave Select (SS)</i> .....                                                       | <u>36</u> |
| • Corrected the Reset FIFO command name (added "FIFO") in 表 6-11, <i>Command Codes</i> .....                                                                                                                         | <u>40</u> |
| • Corrected Reset FIFO command name in the title of 节 6.13.2, <i>Reset FIFO (0x0F)</i> .....                                                                                                                         | <u>40</u> |
| • Removed former Section 6.13.12, <i>Receiver Gain Adjust (0x1A)</i> .....                                                                                                                                           | <u>42</u> |
| • Moved 节 6.14, <i>Register Description</i> .....                                                                                                                                                                    | <u>43</u> |
| • Removed "AGC" from the description of the register in 节 6.14.1.1.1, <i>Chip Status Control Register (0x00)</i> .....                                                                                               | <u>44</u> |
| • Changed B2 to Reserved in 表 6-16, <i>Chip Status Control Register (0x00)</i> .....                                                                                                                                 | <u>44</u> |
| • Changed B1 and B0 to Reserved in 表 6-23, <i>RX Special Setting Register (0x0A)</i> .....                                                                                                                           | <u>49</u> |
| • Removed the description of AGC in 节 6.14.1.2.5, <i>RX Special Setting Register (0x0A)</i> .....                                                                                                                    | <u>49</u> |
| • Changed "High nibble" to "Middle nibble" in description of B3:B0 in 表 6-36, <i>TX Length Byte1 Register (0x1D)</i> .....                                                                                           | <u>56</u> |
| • Changed "High nibble" to "Low nibble" in description of B7:B4 in 表 6-37, <i>TX Length Byte2 Register (0x1E)</i> .....                                                                                              | <u>57</u> |
| • Moved and changed title of 节 7, <i>Applications, Implementation, and Layout</i> .....                                                                                                                              | <u>58</u> |
| • Deleted former section <i>Reader System Using Parallel Microcontroller Interface</i> in 节 7, <i>Applications, Implementation, and Layout</i> .....                                                                 | <u>58</u> |
| • Updated 图 7-1, <i>Application Schematic, SPI With SS Mode MCU Interface</i> .....                                                                                                                                  | <u>58</u> |
| • Updated the paragraph that starts "Minimum MCU requirements depend on application requirements..." in 节 7.1.2, <i>Schematic</i> .....                                                                              | <u>58</u> |
| • Moved 节 7.2, <i>System Design</i> .....                                                                                                                                                                            | <u>59</u> |
| • 添加了节 8.1“入门和后续步骤” .....                                                                                                                                                                                            | <u>61</u> |
| • 添加了节 8.2“器件命名规则” .....                                                                                                                                                                                             | <u>61</u> |
| • 添加了节 8.3“工具和软件” .....                                                                                                                                                                                              | <u>62</u> |
| • 更新了节 8.4“文档支持” .....                                                                                                                                                                                               | <u>62</u> |

## 3 Device Characteristics

Table 3-1 lists the supported protocols.

**Table 3-1. Supported Protocols**

| DEVICE   | ISO/IEC 15693 | ISO/IEC 18000-3<br>MODE 1 |
|----------|---------------|---------------------------|
| TRF7962A | ✓             | ✓                         |

### 3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

**Products for TI Wireless Connectivity** Connect more with the industry's broadest wireless connectivity portfolio.

**Products for NFC / RFID** TI provides one of the industry's most differentiated NFC and RFID product portfolios and is your solution to meet a broad range of NFC connectivity and RFID identification needs.

**Companion Products for TRF7962A** Review products that are frequently purchased or used with this product.

**Reference Designs for TRF7962A** The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at [ti.com/tidesigns](http://ti.com/tidesigns).

## 4 Terminal Configuration and Functions

### 4.1 Pin Diagrams

Figure 4-1 shows the pinout for the 32-pin RHB package.

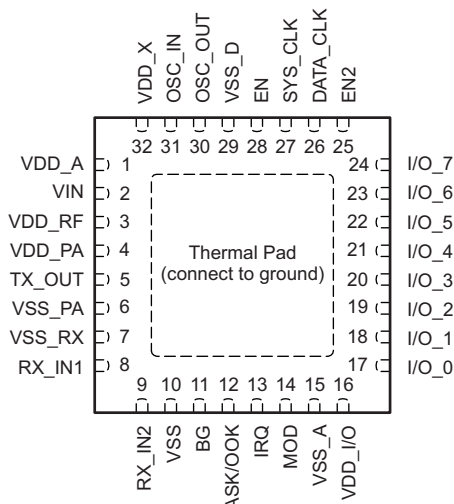


Figure 4-1. 32-Pin RHB Package (Top View)

### 4.2 Signal Descriptions

Table 4-1 describes the signals.

Table 4-1. Signal Descriptions

| TERMINAL |          | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                          |
|----------|----------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NO.      | NAME     |                     |                                                                                                                                                                      |
| 1        | VDD_A    | OUT                 | Internal regulated supply (2.7 V to 3.4 V) for analog circuitry                                                                                                      |
| 2        | VIN      | SUP                 | External supply input to chip (2.7 V to 5.5 V)                                                                                                                       |
| 3        | VDD_RF   | OUT                 | Internal regulated supply (2.7 V to 5 V); normally connected to VDD_PA (pin 4)                                                                                       |
| 4        | VDD_PA   | INP                 | Supply for PA; normally connected externally to VDD_RF (pin 3)                                                                                                       |
| 5        | TX_OUT   | OUT                 | RF output (selectable output power: 100 mW or 200 mW, with $V_{DD} = 5$ V)                                                                                           |
| 6        | VSS_PA   | SUP                 | Negative supply for PA; normally connected to circuit ground                                                                                                         |
| 7        | VSS_RX   | SUP                 | Negative supply for receive inputs; normally connected to circuit ground                                                                                             |
| 8        | RX_IN1   | INP                 | Main receive input                                                                                                                                                   |
| 9        | RX_IN2   | INP                 | Auxiliary receive input                                                                                                                                              |
| 10       | VSS      | SUP                 | Chip substrate ground                                                                                                                                                |
| 11       | BAND_GAP | OUT                 | Bandgap voltage ( $V_{BG} = 1.6$ V); internal analog voltage reference                                                                                               |
| 12       | ASK/OOK  | BID                 | Selection between ASK and OOK modulation (0 = ASK, 1 = OOK) for direct mode 0 and 1. It can be configured as an output to provide the received analog signal output. |
| 13       | IRQ      | OUT                 | Interrupt request                                                                                                                                                    |
| 14       | MOD      | INP                 | External data modulation input for direct mode 0 or 1                                                                                                                |
|          |          | OUT                 | Subcarrier digital data output (see register 0x1A and 0x1B definitions)                                                                                              |
| 15       | VSS_A    | SUP                 | Negative supply for internal analog circuits. Connected to GND.                                                                                                      |
| 16       | VDD_I/O  | INP                 | Supply for I/O communications (1.8 V to VIN) level shifter. VIN should be never exceeded.                                                                            |
| 17       | I/O_0    | BID                 | I/O pin for parallel communication                                                                                                                                   |
| 18       | I/O_1    | BID                 | I/O pin for parallel communication                                                                                                                                   |
| 19       | I/O_2    | BID                 | I/O pin for parallel communication                                                                                                                                   |

(1) SUP = Supply, INP = Input, BID = Bidirectional, OUT = Output

**Table 4-1. Signal Descriptions (continued)**

| TERMINAL |          | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                      |
|----------|----------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NO.      | NAME     |                     |                                                                                                                                                                                                  |
| 20       | I/O_3    | BID                 | I/O pin for parallel communication                                                                                                                                                               |
| 21       | I/O_4    | BID                 | I/O pin for parallel communication<br>Slave select signal in SPI mode                                                                                                                            |
| 22       | I/O_5    | BID                 | I/O pin for parallel communication<br>Data clock output in direct mode 1                                                                                                                         |
| 23       | I/O_6    | BID                 | I/O pin for parallel communication<br>MISO for serial communication (SPI)<br>Serial bit data output in direct mode 1 or subcarrier signal in direct mode 0                                       |
| 24       | I/O_7    | BID                 | I/O pin for parallel communication.<br>MOSI for serial communication (SPI)                                                                                                                       |
| 25       | EN2      | INP                 | Selection of power down mode. If EN2 is connected to VIN, then VDD_X is active during power down mode 2 (for example, to supply the MCU).                                                        |
| 26       | DATA_CLK | INP                 | Data clock input for MCU communication (parallel and serial)                                                                                                                                     |
| 27       | SYS_CLK  | OUT                 | If EN = 1 (EN2 = don't care) the system clock for the MCU is configured with register 0x09 (off, 3.39 MHz, 6.78 MHz, or 13.56 MHz).<br>If EN = 0 and EN2 = 1, the system clock is set to 60 kHz. |
| 28       | EN       | INP                 | Chip enable input (if EN = 0, then the chip is in sleep or power-down mode)                                                                                                                      |
| 29       | VSS_D    | SUP                 | Negative supply for internal digital circuits                                                                                                                                                    |
| 30       | OSC_OUT  | OUT                 | Crystal or oscillator output                                                                                                                                                                     |
| 31       | OSC_IN   | INP                 | Crystal or oscillator input                                                                                                                                                                      |
| 32       | VDD_X    | OUT                 | Internally regulated supply (2.7 V to 3.4 V) for digital circuit and external devices (for example, an MCU)                                                                                      |
| PAD      | PAD      | SUP                 | Chip substrate ground                                                                                                                                                                            |

## 5 Specifications

### 5.1 Absolute Maximum Ratings <sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted) <sup>(2)</sup>

|                                                                      |                                             | MIN  | MAX | UNIT |
|----------------------------------------------------------------------|---------------------------------------------|------|-----|------|
| Input voltage range, $V_{IN}$                                        |                                             | –0.3 | 6   | V    |
| Maximum current, $I_{IN}$                                            |                                             |      | 150 | mA   |
| Maximum operating virtual junction temperature, $T_J$ <sup>(3)</sup> | Any condition                               |      | 140 | °C   |
|                                                                      | Continuous operation, long-term reliability |      | 125 |      |
| Storage temperature, $T_{STG}$                                       |                                             | –55  | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to substrate ground terminal VSS.
- (3) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability or lifetime of the device.

### 5.2 ESD Ratings

|                                     |                                                                                | VALUE | UNIT |
|-------------------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |
|                                     | Machine model (MM)                                                             | ±200  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|          |                                        | MIN | NOM | MAX | UNIT |
|----------|----------------------------------------|-----|-----|-----|------|
| $V_{IN}$ | Operating input voltage                | 2.7 | 5   | 5.5 | V    |
| $T_A$    | Operating ambient temperature          | –25 | 25  | 85  | °C   |
| $T_J$    | Operating virtual junction temperature | –25 | 25  | 125 | °C   |

## 5.4 Electrical Characteristics

TYP operating conditions are  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{ V}$ , full-power mode (unless otherwise noted)

MIN and MAX operating conditions are over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                       | TEST CONDITIONS                                                                                                                           | MIN | TYP   | MAX                      | UNIT          |
|-------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|--------------------------|---------------|
| $I_{PD1}$ Supply current in power down mode 1                                                   | All building blocks disabled, including supply-voltage regulators; measured after 500-ms settling time ( $EN = 0$ , $EN2 = 0$ )           |     | <0.5  | 5                        | $\mu\text{A}$ |
| $I_{PD2}$ Supply current in power down mode 2 (sleep mode)                                      | The SYS_CLK generator and VDD_X remain active to support external circuitry, measured after 100-ms settling time ( $EN = 0$ , $EN2 = 1$ ) |     | 120   | 200                      | $\mu\text{A}$ |
| $I_{STBY}$ Supply current in standby mode                                                       | Oscillator running, supply-voltage regulators in low-consumption mode ( $EN = 1$ , $EN2 = x$ )                                            |     | 1.9   | 3.5                      | mA            |
| $I_{ON1}$ Supply current without antenna driver current                                         | Oscillator, regulators, RX, and AGC are active, TX is off                                                                                 |     | 10.5  | 14                       | mA            |
| $I_{ON2}$ Supply current in TX (half power)                                                     | Oscillator, regulators, RX, AGC, and TX active, $P_{OUT} = 100\text{ mW}$                                                                 |     | 70    | 78                       | mA            |
| $I_{ON3}$ Supply current in TX (full power)                                                     | Oscillator, regulators, RX, AGC, and TX active, $P_{OUT} = 200\text{ mW}$                                                                 |     | 130   | 170                      | mA            |
| $V_{POR}$ Power-on reset voltage                                                                | Input voltage at $V_{IN}$                                                                                                                 | 1.4 | 2     | 2.6                      | V             |
| $V_{BG}$ Bandgap voltage (pin 11)                                                               | Internal analog reference voltage                                                                                                         | 1.5 | 1.6   | 1.7                      | V             |
| $V_{DD\_A}$ Regulated output voltage for analog circuitry (pin 1)                               | $V_{IN} = 5\text{ V}$                                                                                                                     | 3.1 | 3.5   | 3.8                      | V             |
| $V_{DD\_X}$ Regulated supply for external circuitry                                             | Output voltage pin 32, $V_{IN} = 5\text{ V}$                                                                                              | 3.1 | 3.4   | 3.8                      | V             |
| $I_{VDD\_Xmax}$ Maximum output current of VDD_X                                                 | Output current pin 32, $V_{IN} = 5\text{ V}$                                                                                              |     |       | 20                       | mA            |
| $R_{RFOUT}$ Antenna driver output resistance <sup>(1)</sup>                                     | Half-power mode, $V_{IN} = 2.7\text{ V}$ to $5.5\text{ V}$                                                                                |     | 8     | 12                       | $\Omega$      |
|                                                                                                 | Full-power mode, $V_{IN} = 2.7\text{ V}$ to $5.5\text{ V}$                                                                                |     | 4     | 6                        |               |
| $R_{RFIN}$ RX_IN1 and RX_IN2 input resistance                                                   |                                                                                                                                           | 4   | 10    | 20                       | k $\Omega$    |
| $V_{RF\_INmax}$ Maximum RF input voltage at RX_IN1 or RX_IN2                                    | $V_{RF\_INmax}$ should not exceed $V_{IN}$                                                                                                |     | 3.5   |                          | $V_{pp}$      |
| $V_{RF\_INmin}$ Minimum RF input voltage at RX_IN1 or RX_IN2 (input sensitivity) <sup>(2)</sup> | $f_{SUBCARRIER} = 424\text{ kHz}$                                                                                                         |     | 1.4   | 2.5                      | mV $_{pp}$    |
|                                                                                                 | $f_{SUBCARRIER} = 848\text{ kHz}$                                                                                                         |     | 2.1   | 3                        |               |
| $f_{SYS\_CLK}$ SYS_CLK frequency                                                                | In power mode 2, $EN = 0$ , $EN2 = 1$                                                                                                     | 25  | 60    | 120                      | kHz           |
| $f_C$ Carrier frequency                                                                         | Defined by external crystal                                                                                                               |     | 13.56 |                          | MHz           |
| $t_{CRYSTAL}$ Crystal run-in time                                                               | Time until oscillator stable bit is set (register 0x0F) <sup>(3)</sup>                                                                    |     | 5     |                          | ms            |
| $f_{D\_CLKmax}$ Maximum DATA_CLK frequency <sup>(4)</sup>                                       | Depends on capacitive load on the I/O lines, recommendation is 2 MHz <sup>(4)</sup>                                                       | 2   | 4     | 10                       | MHz           |
| $V_{IL}$ Input voltage, logic low                                                               | I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2                                                                                                |     |       | $0.2 \times V_{DD\_I/O}$ | V             |
| $V_{IH}$ Input voltage threshold, logic high                                                    | I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2                                                                                                |     |       | $0.8 \times V_{DD\_I/O}$ | V             |
| $R_{OUT}$ Output resistance, I/O_0 to I/O_7                                                     |                                                                                                                                           |     | 500   | 800                      | $\Omega$      |
| $R_{SYS\_CLK}$ Output resistance $R_{SYS\_CLK}$                                                 |                                                                                                                                           |     | 200   | 400                      | $\Omega$      |

(1) Antenna driver output resistance

(2) Measured with subcarrier signal at RX\_IN1 or RX\_IN2 and measured the digital output at MOD pin with register 0x1A bit 6 = 1

(3) Depending on the crystal parameters and components

(4) Recommended DATA\_CLK speed is 2 MHz; higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. MISO driver has a typical output resistance of 400  $\Omega$  (12-ns time constant when 30-pF load is used).

## 5.5 Thermal Resistance Characteristics

| PACKAGE  | $R_{\theta JC}$ | $R_{\theta JA}^{(1)}$ | POWER RATING <sup>(2)</sup> |                             |
|----------|-----------------|-----------------------|-----------------------------|-----------------------------|
|          |                 |                       | $T_A \leq 25^\circ\text{C}$ | $T_A \leq 85^\circ\text{C}$ |
| RHB (32) | 31°C/W          | 36.4°C/W              | 2.7 W                       | 1.1 W                       |

- (1) This data was taken using the JEDEC standard high-K test PCB.
- (2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to increase substantially. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

## 5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

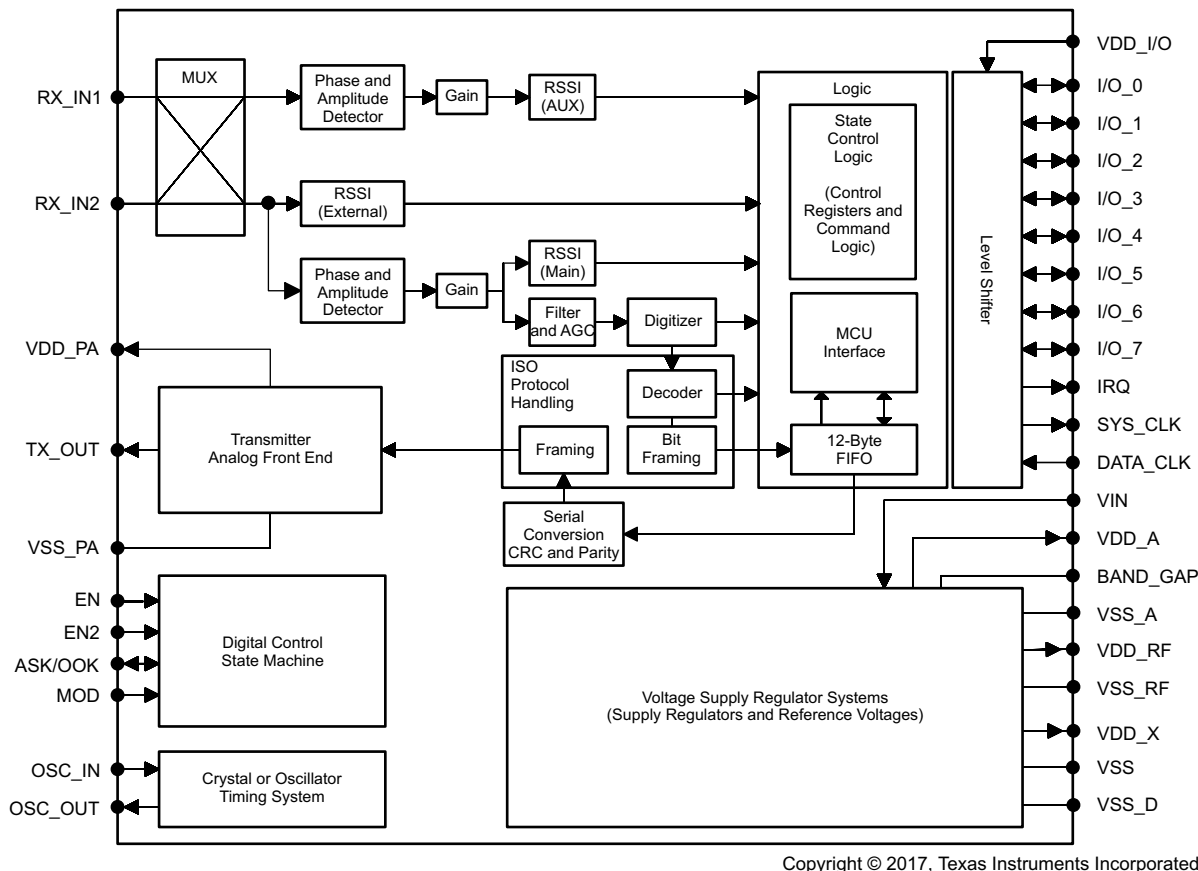
| PARAMETER      |                                                                     | TEST CONDITIONS                                            | MIN | TYP  | MAX | UNIT |
|----------------|---------------------------------------------------------------------|------------------------------------------------------------|-----|------|-----|------|
| $t_{LO/HI}$    | DATA_CLK time, high or low (one half of DATA_CLK at 50% duty cycle) | Depends on capacitive load on the I/O lines <sup>(1)</sup> | 50  | 62.5 | 250 | ns   |
| $t_{STE,LEAD}$ | Slave select lead time, slave select low to clock                   |                                                            |     | 200  |     | ns   |
| $t_{STE,LAG}$  | Slave select lag time, last clock to slave select high              |                                                            |     | 200  |     | ns   |
| $t_{SU,SI}$    | MOSI input data setup time                                          |                                                            | 15  |      |     | ns   |
| $t_{HD,SI}$    | MOSI input data hold time                                           |                                                            | 15  |      |     | ns   |
| $t_{SU,SO}$    | MISO input data setup time                                          |                                                            | 15  |      |     | ns   |
| $t_{HD,SO}$    | MISO input data hold time                                           |                                                            | 15  |      |     | ns   |
| $t_{VALID,SO}$ | MISO output data valid time                                         | DATA_CLK edge to MISO valid, $C_L = <30$ pF                | 30  | 50   | 75  | ns   |

- (1) Recommended DATA\_CLK speed is 2 MHz; higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. MISO driver has a typical output resistance of 400  $\Omega$  (12-ns time constant when 30-pF load is used).

## 6 Detailed Description

### 6.1 Functional Block Diagram

Figure 6-1 shows the functional block diagram.



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Figure 6-1. Functional Block Diagram

### 6.2 Power Supplies

The TRF7962A positive supply input VIN (pin 2) sources three internal regulators with output voltages VDD\_RF, VDD\_A, and VDD\_X. All regulators require external bypass capacitors for supply noise filtering and must be connected as indicated in reference schematics. These regulators provide a high power supply reject ratio (PSRR) as required for RFID reader systems. All regulators are supplied by VIN (pin 2).

The regulators are not independent and have common control bits in register 0x0B for output voltage setting. The regulators can be configured to operate in either automatic or manual mode (register 0x0B, bit 7). The automatic regulator setting mode ensures an optimal compromise between PSRR and the highest possible supply voltage for RF output (to ensure maximum RF power output). The manual mode lets the user manually configure the regulator settings.

## 6.3 Supply Arrangements

### Regulator Supply Input: VIN

The positive supply at VIN (pin 2) has an input voltage range of 2.7 V to 5.5 V. VIN provides the supply input sources for three internal regulators with the output voltages VDD\_RF, VDD\_A, and VDD\_X. External bypass capacitors for supply noise filtering must be used (per reference schematics).

---

#### NOTE

VIN must be the highest voltage supplied to the TRF7962A.

---

### RF Power Amplifier Regulator: VDD\_RF

The VDD\_RF (pin 3) regulator is supplying the RF power amplifier. The voltage regulator can be set for either 5-V or 3-V operation. External bypass capacitors for supply noise filtering must be used (per reference schematics). When configured for 5-V manual operation, the VDD\_RF output voltage can be set from 4.3 V to 5 V in 100-mV steps. In 3-V manual operation, the output can be programmed from 2.7 V to 3.4 V in 100-mV steps (see [Table 6-2](#)). The maximum output current capability for 5-V operation is 150 mA and for 3-V operation is 100 mA.

### Analog Supply Regulator: VDD\_A

Regulator VDD\_A (pin 1) supplies the analog circuits of the device. The output voltage setting depends on the input voltage and can be set for 5-V and 3-V operation. When configured for 5-V manual operation, the output voltage is fixed at 3.4 V. External bypass capacitors for supply noise filtering must be used (per reference schematics). When configured for 3-V manual operation, the VDD\_A output can be set from 2.7 V to 3.4 V in 100-mV steps (see [Table 6-2](#)).

---

#### NOTE

The configuration of VDD\_A and VDD\_X regulators are not independent from each other. The VDD\_A output current should not exceed 20 mA.

---

### Digital Supply Regulator: VDD\_X

The digital supply regulator VDD\_X (pin 32) provides the power for the internal digital building blocks and can also be used to supply external electronics within the reader system. When configured for 3-V operation, the output voltage can be set from 2.7 to 3.4 V in 100-mV steps. External bypass capacitors for supply noise filtering must be used (refer to the reference schematics).

---

#### NOTE

The configuration of the VDD\_A and VDD\_X regulators are not independent from each other. The VDD\_X output current should not exceed 20 mA.

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The RF power amplifier regulator (VDD\_RF), analog supply regulator (VDD\_A), and digital supply regulator (VDD\_X) can be configured to operate in either automatic or manual mode described in [Table 6-1](#). The automatic regulator setting mode ensures an optimal compromise between PSRR and the highest possible supply voltage to ensure maximum RF power output.

By default, the regulators are set in automatic regulator setting mode. In this mode, the regulators are automatically set every time the system is activated by setting EN input High or each time the automatic regulator setting bit, B7 in register 0x0B is set to a 1. The action is started on the 0 to 1 transition. This means that, if the user wants to rerun the automatic setting from a state in which the automatic setting bit is already high, the automatic setting bit (B7 in register 0x0B) should be changed: 1-0-1.

By default, the regulator setting algorithm sets the regulator outputs to a "Delta Voltage" of 250 mV below VIN, but not higher than 5 V for VDD\_RF and 3.4 V for VDD\_A and VDD\_X. The "Delta Voltage" in automatic regulator mode can be increased up to 400 mV (for more details, see bits B0 to B2 in register 0x0B).

#### Power Amplifier Supply: VDD\_PA

The power amplifier of the TRF7962A is supplied through VDD\_PA (pin 4). The positive supply pin for the RF power amplifier is externally connected to the regulator output VDD\_RF (pin 3).

#### I/O Level Shifter Supply: VDD\_I/O

The TRF7962A has a separate supply input VDD\_I/O (pin 16) for the build in I/O level shifter. The supported input voltage ranges from 1.8 V to VIN, however not exceeding 5.5 V. Pin 16 is used to supply the I/O interface pins (I/O\_0 to I/O\_7), IRQ, SYS\_CLK, and DATA\_CLK pins of the reader. In typical applications, VDD\_I/O is directly connected to VDD\_X while VDD\_X also supplies the MCU. This ensures that the I/O signal levels of the MCU match with the logic levels of the TRF7962A.

#### Negative Supply Connections: VSS, VSS\_RX, VSS\_A, VSS\_PA

The negative supply connections VSS\_X of each functional block are all externally connected to GND.

The substrate connection is VSS (pin 10), the analog negative supply is VSS\_A (pin 15), the logic negative supply is VSS\_D (pin 29), the RF output stage negative supply is VSS\_PA (pin 6), and the negative supply for the RF receiver VSS\_RX (pin 7).

## 6.4 Supply Regulator Settings

The input supply voltage mode of the reader must be selected. This is done in the Chip Status Control register (0x00). Bit 0 in register 0x00 selects either 5-V or 3-V input supply voltage. The default configuration is 5 V, which reflects an operating supply voltage range of 4.3 V to 5.5 V. If the supply voltage is below 4.3 V, the 3-V configuration should be used.

The various regulators can be configured to operate in automatic or manual mode. This is done in the Regulator and I/O Control register (0x0B) (see [Table 6-1](#) and [Table 6-2](#)).

**Table 6-1. Supply Regulator Setting: 5-V System**

| REGISTER ADDRESS         | OPTION BITS SETTING IN REGULATOR CONTROL REGISTER <sup>(1)</sup> |    |    |    |    |    |    |    | COMMENTS                                           |
|--------------------------|------------------------------------------------------------------|----|----|----|----|----|----|----|----------------------------------------------------|
|                          | B7                                                               | B6 | B5 | B4 | B3 | B2 | B1 | B0 |                                                    |
| Automatic Mode (default) |                                                                  |    |    |    |    |    |    |    |                                                    |
| 0B                       | 1                                                                | x  | x  | x  | x  | x  | 1  | 1  | Automatic regulator setting with 250-mV difference |
| 0B                       | 1                                                                | x  | x  | x  | x  | x  | 1  | 0  | Automatic regulator setting with 350-mV difference |
| 0B                       | 1                                                                | x  | x  | x  | x  | x  | 0  | 0  | Automatic regulator setting with 400-mV difference |
| Manual Mode              |                                                                  |    |    |    |    |    |    |    |                                                    |
| 0B                       | 0                                                                | x  | x  | x  | x  | 1  | 1  | 1  | VDD_RF = 5 V, VDD_A = 3.4 V, VDD_X = 3.4 V         |
| 0B                       | 0                                                                | x  | x  | x  | x  | 1  | 1  | 0  | VDD_RF = 4.9 V, VDD_A = 3.4 V, VDD_X = 3.4 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 1  | 0  | 1  | VDD_RF = 4.8 V, VDD_A = 3.4 V, VDD_X = 3.4 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 1  | 0  | 0  | VDD_RF = 4.7 V, VDD_A = 3.4 V, VDD_X = 3.4 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 0  | 1  | 1  | VDD_RF = 4.6 V, VDD_A = 3.4 V, VDD_X = 3.4 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 0  | 1  | 0  | VDD_RF = 4.5 V, VDD_A = 3.4 V, VDD_X = 3.4 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 0  | 0  | 1  | VDD_RF = 4.4 V, VDD_A = 3.4 V, VDD_X = 3.4 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 0  | 0  | 0  | VDD_RF = 4.3 V, VDD_A = 3.4 V, VDD_X = 3.4 V       |

(1) x = don't care

**Table 6-2. Supply Regulator Setting: 3-V System**

| REGISTER ADDRESS         | OPTION BITS SETTING IN REGULATOR CONTROL REGISTER <sup>(1)</sup> |    |    |    |    |    |    |    | COMMENTS                                           |
|--------------------------|------------------------------------------------------------------|----|----|----|----|----|----|----|----------------------------------------------------|
|                          | B7                                                               | B6 | B5 | B4 | B3 | B2 | B1 | B0 |                                                    |
| Automatic Mode (default) |                                                                  |    |    |    |    |    |    |    |                                                    |
| 0B                       | 1                                                                | x  | x  | x  | x  | x  | 1  | 1  | Automatic regulator setting with 250-mV difference |
| 0B                       | 1                                                                | x  | x  | x  | x  | x  | 1  | 0  | Automatic regulator setting with 350-mV difference |
| 0B                       | 1                                                                | x  | x  | x  | x  | x  | 0  | 0  | Automatic regulator setting with 400-mV difference |
| Manual Mode              |                                                                  |    |    |    |    |    |    |    |                                                    |
| 0B                       | 0                                                                | x  | x  | x  | x  | 1  | 1  | 1  | VDD_RF = 3.4 V, VDD_A = 3.4 V, VDD_X = 3.4 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 1  | 1  | 0  | VDD_RF = 3.3 V, VDD_A = 3.3 V, VDD_X = 3.3 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 1  | 0  | 1  | VDD_RF = 3.2 V, VDD_A = 3.2 V, VDD_X = 3.2 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 1  | 0  | 0  | VDD_RF = 3.1 V, VDD_A = 3.1 V, VDD_X = 3.1 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 0  | 1  | 1  | VDD_RF = 3.0 V, VDD_A = 3.0 V, VDD_X = 3.0 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 0  | 1  | 0  | VDD_RF = 2.9 V, VDD_A = 2.9 V, VDD_X = 2.9 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 0  | 0  | 1  | VDD_RF = 2.8 V, VDD_A = 2.8 V, VDD_X = 2.8 V       |
| 0B                       | 0                                                                | x  | x  | x  | x  | 0  | 0  | 0  | VDD_RF = 2.7 V, VDD_A = 2.7 V, VDD_X = 2.7 V       |

(1) x = don't care

The regulator configuration function adjusts the regulator outputs by default to 250 mV below VIN level, but not higher than 5 V for VDD\_RF, 3.4 V for VDD\_A and VDD\_X. This ensures the highest possible supply voltage for the RF output stage while maintaining an adequate PSRR (power supply rejection ratio).

To further improve the PSRR, it is possible to increase the target voltage difference across VDD\_X and VDD\_A from its default to 350 mV or even 400 mV (for details, see Regulator and I/O Control register 0x0B definition and [Table 6-2](#).)

## 6.5 Power Modes

The chip has several power states, which are controlled by two input pins (EN and EN2) and several bits in the Chip Status Control register (0x00).

[Table 6-3](#) lists the configuration for the different power modes when using a 5-V or 3-V system supply. The main reader enable signal is pin EN. When EN is set high, all of the reader regulators are enabled, the 13.56-MHz oscillator is running, and the SYS\_CLK (output clock for external microcontroller) is also available.

The Regulator Control register settings shown are for optimized power out. The automatic setting (normally 0x87) is optimized for best PSRR and noise reduction.

Table 6-3. Power Modes<sup>(1)</sup>

| MODE                              | EN2 | EN | CHIP STATUS<br>CONTROL<br>REGISTER<br>(0X00) | REGULATOR<br>CONTROL<br>REGISTER<br>(0X0B) | TRANS-<br>MITTER | RECEIVER | SYS_CLK<br>(13.56 MHz) | SYS_CLK<br>(60 kHz) | VDD_X | TYPICAL<br>CURRENT<br>(mA) | TYPICAL<br>POWER<br>OUT (dBm) | TIME<br>(FROM<br>PREVIOUS<br>STATE) |
|-----------------------------------|-----|----|----------------------------------------------|--------------------------------------------|------------------|----------|------------------------|---------------------|-------|----------------------------|-------------------------------|-------------------------------------|
| Mode 4<br>(full power)<br>5 VDC   | x   | 1  | 21                                           | 07                                         | On               | On       | On                     | x                   | On    | 130                        | 23                            | 20 to 25 $\mu$ s                    |
| Mode 4<br>(full power)<br>3.3 VDC | x   | 1  | 20                                           | 07                                         | On               | On       | On                     | x                   | On    | 67                         | 18                            |                                     |
| Mode 3<br>(half power)<br>5 VDC   | x   | 1  | 31                                           | 07                                         | On               | On       | On                     | x                   | On    | 70                         | 20                            | 20 to 25 $\mu$ s                    |
| Mode 3<br>(half power)<br>3.3 VDC | x   | 1  | 30                                           | 07                                         | On               | On       | On                     | x                   | On    | 53                         | 15                            |                                     |
| Mode 2<br>5 VDC                   | x   | 1  | 03                                           | 07                                         | Off              | On       | On                     | x                   | On    | 10.5                       | —                             | 20 to 25 $\mu$ s                    |
| Mode 2<br>3.3 VDC                 | x   | 1  | 02                                           | 00                                         | Off              | On       | On                     | x                   | On    | 9                          | —                             |                                     |
| Mode 1<br>5 VDC                   | x   | 1  | 01                                           | 07                                         | Off              | Off      | On                     | x                   | On    | 5                          | —                             | 20 to 25 $\mu$ s                    |
| Mode 1<br>3.3 VDC                 | x   | 1  | 00                                           | 00                                         | Off              | Off      | On                     | x                   | On    | 3                          |                               |                                     |
| Standby mode<br>5 VDC             | x   | 1  | 81                                           | 07                                         | Off              | Off      | On                     | x                   | On    | 3                          | —                             | 4.8 ms                              |
| Standby mode<br>3.3 VDC           | x   | 1  | 80                                           | 00                                         | Off              | Off      | On                     | x                   | On    | 2                          | —                             |                                     |
| Sleep mode                        | 1   | 0  | x                                            | x                                          | Off              | Off      | Off                    | On                  | On    | 0.120                      | —                             | 1.5 ms                              |
| Power down                        | 0   | 0  | x                                            | x                                          | Off              | Off      | Off                    | Off                 | Off   | <0.001                     | —                             | Start                               |

(1) x = don't care

The input pin EN2 has two functions:

- A direct connection from EN2 to VIN to ensure the availability of the regulated supply VDD\_X and an auxiliary clock signal (60 kHz, SYS\_CLK) for an external MCU. This mode (EN = 0, EN2 = 1) is intended for systems in which the MCU is also being supplied by the reader supply regulator (VDD\_X) and the MCU clock is supplied by the SYS\_CLK output of the reader. This lets the MCU supply and clock be available during sleep mode.
- EN2 enables the start-up of the reader system from complete power down (EN = 0, EN2 = 0). In this case, the EN input is being controlled by the MCU (or other system device) that is without supply voltage during complete power down (thus unable to control the EN input). A rising edge applied to the EN2 input (which has an approximately 1-V threshold level) starts the reader supply system and 13.56-MHz oscillator (identical to condition EN = 1).

When the user MCU controls EN and EN2, use a delay of 5 ms between EN and EN2. When the MCU controls only EN, TI recommends connecting EN2 to either VIN or GND, depending on the application MCU requirements for VDD\_X and SYS\_CLK.

#### NOTE

Using EN = 1 and EN2 = 1 in parallel at start-up should not be done as it may cause incorrect operation.

This start-up mode lasts until all of the regulators have settled and the 13.56-MHz oscillator has stabilized. If the EN input is set high (EN = 1) by the MCU (or other system device), the reader stays active. If the EN input is not set high (EN = 0) within 100  $\mu$ s after the SYS\_CLK output is switched from auxiliary clock (60 kHz) to high-frequency clock (derived from the crystal oscillator), the reader system returns to complete Power-Down Mode 1. This option can be used to wake the reader system from complete power down (PD Mode 1) by using a push-button switch or by sending a single pulse.

After the reader EN line is high, the other power modes are selected by control bits within the Chip Status Control register (0x00). The power mode options and states are listed in [Table 6-3](#).

When EN is set high (or on rising edge of EN2 and then confirmed by EN = 1) the supply regulators are activated and the 13.56-MHz oscillator started. When the supplies are settled and the oscillator frequency is stable, the SYS\_CLK output is switched from the auxiliary frequency of 60 kHz to the 13.56-MHz frequency derived from the crystal oscillator. At this time, the reader is ready to communicate and perform the required tasks. The MCU can then program the Chip Status Control register 0x00 and select the operation mode by programming the additional registers.

- Standby mode (bit 7 = 1 of register 0x00), the reader is capable of recovering to full operation in 100  $\mu$ s.
- Mode 1 (active mode with RF output disabled, bit 5 = 0 and bit 1 = 0 of register 0x00) is a low-power mode that lets the reader recover to full operation within 25  $\mu$ s.
- Mode 2 (active mode with only the RF receiver active, bit 1 = 1 of register 0x00) can be used to measure the external RF field (as described in RSSI measurements paragraph) if reader-to-reader anticollision is implemented.
- Mode 3 and Mode 4 (active modes with the entire RF section active, bit 5 = 1 of register 0x00) are the modes used for typical transmit and receive operations.

## 6.6 Receiver – Analog Section

### 6.6.1 Main and Auxiliary Receiver

The TRF7962A has two receiver inputs: RX\_IN1 (pin 8) and RX\_IN2 (pin 9). Each of the inputs is connected to an external capacitive voltage divider to ensure that the modulated signal from the tag is available on at least one of the two inputs. This architecture eliminates any possible communication holes that may occur from the tag to the reader.

The two RX inputs (RX\_IN1 and RX\_IN2) are multiplexed into two receivers—the main receiver and the auxiliary receiver. Only the main receiver is used for reception; the auxiliary receiver is used for signal quality monitoring. Receiver input multiplexing is controlled by bit B3 in the Chip Status Control register (address 0x00).

After start-up, RX\_IN1 is multiplexed to the main receiver which is composed of an RF envelope detection, first gain and band-pass filtering stage, second gain and filtering stage with AGC. Only the main receiver is connected to the digitizing stage which output is connected to the digital processing block. The main receiver also has an RSSI measuring stage, which measures the strength of the demodulated signal (subcarrier signal).

The primary function of the auxiliary receiver is to monitor the RX signal quality by measuring the RSSI of the demodulated subcarrier signal (internal RSSI). After start-up, RX\_IN2 is multiplexed to the auxiliary receiver. The auxiliary receiver has an RF envelope detection stage, first gain and filtering with AGC stage and finally the auxiliary RSSI block.

The default MUX setting is RX\_IN1 connected to the main receiver and RX\_IN2 connected to the auxiliary receiver. To determine the signal quality, the response from the tag is detected by the "main" (pin RX\_IN1) and "auxiliary" (pin RX\_IN2) RSSI. Both values measured and stored in the RSSI level register (address 0x0F). The MCU can read the RSSI values from the TRF7962A RSSI register and decide if swapping the input signals is preferable or not. Setting B3 in the Chip Status Control register (address 0x00) to 1 connects RX\_IN1 (pin 8) to the auxiliary receiver and RX\_IN2 (pin 9) to the main receiver.

The main and auxiliary receiver input stages are RF envelope detectors. The RF amplitude at RX\_IN1 and RX\_IN2 should be approximately 3 V<sub>PP</sub> for a VIN supply level greater than 3.3 V. If the VIN level is lower, the RF input peak-to-peak voltage level should not exceed the VIN level.

### 6.6.2 Receiver Gain and Filter Stages

The first gain and filtering stage has a nominal gain of 15 dB with an adjustable band-pass filter. The band-pass filter has programmable 3-dB corner frequencies from 110 kHz to 450 kHz for the high-pass filter and from 570 kHz to 1500 kHz for the low-pass filter. After the band-pass filter, there is another gain-and-filtering stage with a nominal gain of 8 dB and with frequency characteristics identical to the first band-pass stage.

The internal filters are configured automatically depending on the selected ISO communication standard in the ISO Control register (address 0x01). If required, additional fine tuning can be done by writing directly to the RX special setting registers (address 0x0A).

[Table 6-4](#) shows the various settings for the receiver analog section.

**Table 6-4. RX Special Setting Register (0x0A)**

| BIT | FUNCTION                                                       | COMMENTS                                                                               |
|-----|----------------------------------------------------------------|----------------------------------------------------------------------------------------|
| B7  | Band-pass filter from 110 kHz to 570 kHz                       |                                                                                        |
| B6  | Band-pass filter from 200 kHz to 900 kHz                       | Appropriate for 424-kHz subcarrier systems used in ISO/IEC 15693                       |
| B5  | Band-pass filter from 450 kHz to 1.5 MHz                       |                                                                                        |
| B4  | Band-pass filter from 100 kHz to 1.5 MHz                       |                                                                                        |
| B3  | 00 = No gain reduction<br>01 = Gain reduction for 5 dB         | Sets the RX digital gain reduction (changing the window of the digitizing comparator). |
| B2  | 10 = Gain reduction for 10 dB<br>11 = Gain reduction for 15 dB |                                                                                        |
| B1  | Reserved                                                       |                                                                                        |
| B0  | Reserved                                                       |                                                                                        |

## 6.7 Receiver – Digital Section

The output of the TRF7962A analog receiver block is a digitized subcarrier signal and is the input to the digital receiver block, which consists of two sections that partly overlap. The digitized subcarrier signal is a digital representation of the modulation signal on the RF envelope. The two sections of the digital receiver block are the protocol bit decoder section and the framing logic section.

The protocol bit decoder section converts the subcarrier coded signal into a serial bit stream and a data clock. The decoder logic is designed for maximum error tolerance. This tolerance lets the decoder section successfully decode even partly corrupted subcarrier signals that would otherwise be lost due to noise or interference.

The framing logic section formats the serial bit stream data from the protocol bit decoder stage into data bytes. During the formatting process, special signals such as the start of frame (SOF), end of frame (EOF), start of communication, and end of communication are automatically removed. The parity bits and CRC bytes are also checked and removed. The end result is "clean" or "raw" data that is then sent to the 12-byte FIFO register where it can be read by the external microcontroller system. Providing the data this way, in conjunction with the timing register settings of the TRF7962A, means the firmware developer must know about much less of the finer details of the ISO protocols to create a very robust application, especially in low-cost platforms where code space is at a premium and high performance is still required.

The start of the receive operation (successfully received SOF) sets the IRQ flags in the IRQ Status register (0x0C). The end of the receive operation is signaled to the external system MCU by setting pin 13 (IRQ) to high. When data is received in the FIFO, an interrupt is sent to the MCU to signal that there is data to be read from the FIFO. The FIFO Status register (0x1C) should be used to provide the number of bytes that should be clocked out during the actual FIFO read. Additionally, an interrupt is sent to the MCU when the received data occupies 75% of the FIFO capacity to signal that the data should be removed from the FIFO. That interrupt is triggered when the received data packet is longer than 9 bytes.

Any error in the data format, parity, or CRC is detected and notified to the external system by an interrupt request pulse. The source condition of the interrupt request pulse is available in the IRQ Status register (0x0C). The main register controlling the digital part of the receiver is the ISO Control register (0x01). By writing to this register, the user selects the protocol to be used. With each new write in this register, the default presets are reloaded in all related registers, so no further adjustments in other registers are needed for proper operation.

### NOTE

If additional register setting changes are needed to fine-tune the system, set the ISO Control register (0x01) before making the additional changes.

The receive section also includes two timers. The RX wait time timer is controlled by the value in the RX Wait Time register (0x08). This timer defines the time interval after the end of the transmit operation in which the receive decoders are not active (held in reset state). This prevents false detections resulting from transients following the transmit operation. The value of the RX Wait Time register (0x08) defines the time in increments of 9.44  $\mu$ s. This register is preset at every write to ISO Control register (0x01) according to the minimum tag response time defined by each standard.

The RX no response timer is controlled by the RX No Response Wait Time register (0x07). This timer measures the time from the start of slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in the IRQ Status register (0x0C). This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register in increments of 37.76  $\mu$ s. This register is also automatically preset for every new protocol selection.

### 6.7.1 Received Signal Strength Indicator (RSSI)

The TRF7962A incorporates three independent RSSI building blocks: Internal Main RSSI, Internal Auxiliary RSSI, and External RSSI. The internal RSSI blocks are measuring the amplitude of the subcarrier signal, and the external RSSI block measures the amplitude of the RF carrier signal at the receiver input.

#### 6.7.1.1 Internal RSSI – Main and Auxiliary Receivers

Each receiver path has its own RSSI block to measure the envelope of the demodulated RF signal (subcarrier). Internal Main RSSI and Internal Auxiliary RSSI are identical except that they are connected to different RF input pins. The Internal RSSI is intended for diagnostic purposes to set the correct RX path conditions.

The Internal RSSI values can be used to adjust the RX gain settings or decide which RX path (main or auxiliary) provides the greater amplitude and, hence, to decide if the MUX may need to be reprogrammed to swap the RX input signal. The measuring system latches the peak value, so the RSSI level can be read after the end of each receive packet. The RSSI register values are reset with every transmission (TX) by the reader. This guarantees an updated RSSI measurement for each new tag response.

The Internal RSSI has 7 steps (3 bit) with a typical increment of approximately 4 dB. The operating range is 600 mVpp to 4.2 Vpp with a typical step size of approximately 600 mV. Both RSSI values "Internal Main" and "Internal Aux" RSSI are stored in the RSSI Levels and Oscillator Status register (0x0F).

Figure 6-2 shows the nominal relationship between the input RF peak level and the RSSI value.

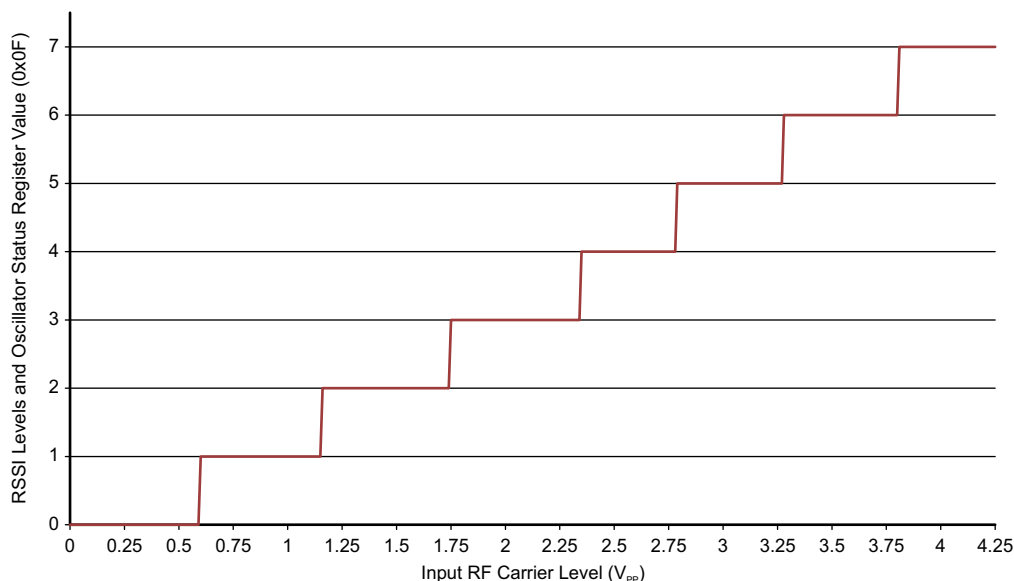


**Figure 6-2. Digital Internal RSSI (Main and Auxiliary) Value vs RF Input Level**

This RSSI measurement is done during the communication to the Tag; this means the TX must be on. Bit 1 in the Chip Status Control register (0x00) defines if internal RSSI or the external RSSI value is stored in the RSSI Levels and Oscillator Status register 0x0F. Direct command 0x18 is used to trigger an internal RSSI measurement.

#### 6.7.1.2 External RSSI

The external RSSI is mainly used for test and diagnostic to sense the amplitude of any 13.56-MHz signal at the receiver's RX\_IN1 input. The external RSSI measurement is typically done in active mode when the receiver is on but transmitter output is off. The level of the RF signal received at the antenna is measured and stored in the RSSI Levels and Oscillator Status register (0x0F).

Figure 6-3 shows the relationship between the voltage at the RX\_IN1 input and the 3-bit code.

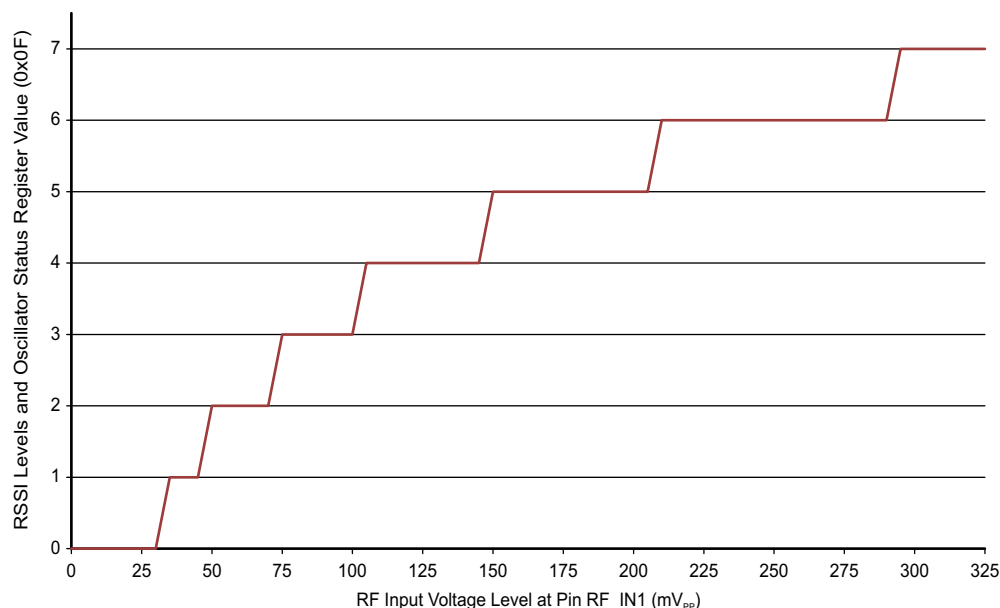


**Figure 6-3. Digital External RSSI Value vs RF Input Level**

The relation between the 3-bit code and the external RF field strength (A/m) sensed by the antenna must be determined by calculation or by experiments for each antenna design. The antenna Q-factor and connection to the RF input influence the result. Direct command 0x19 is used to trigger an internal RSSI measurement.

To check the internal or external RSSI value independent of any other operation:

1. Set transmitter to desired state (on or off) using Bit 5 of the Chip Status Control register (0x00) and enable receiver using Bit 1.
2. Check internal or external RSSI using direct commands 0x18 or 0x19, respectively. This action places the RSSI value in the RSSI register.
3. Delay at least 50  $\mu$ s.
4. Read the RSSI register using direct command 0x0F. Values can range from 0x40 to 0x7F.
5. Repeat steps 1 to 4 as desired; the register is reset after read.

## 6.8 Oscillator Section

The 13.56-MHz oscillator is controlled by the Chip Status Control register (0x00) and the EN and EN2 signals. The oscillator generates the RF frequency for the RF output stage and the clock source for the digital section. The buffered clock signal is available at pin 27 (SYS\_CLK) for external circuits. B4 and B5 inside the Modulation and SYS\_CLK register (0x09) can be used to divide the external SYS\_CLK signal at pin 27 by 1, 2, or 4.

Typical start-up time from complete power down is in the range of 3.5 ms.

During Power Down Mode 2 (EN = 0, EN2 = 1) the frequency of SYS\_CLK is switched to 60 kHz (typical).

The 13.56-MHz crystal must be connected between pin 30 and pin 31. The external shunt capacitors values for  $C_1$  and  $C_2$  must be calculated based on the specified load capacitance of the crystal being used. The external shunt capacitors are calculated as two identical capacitors in series plus the stray capacitance of the TRF7962A and parasitic PCB capacitance in parallel to the crystal.

The parasitic capacitance ( $C_S$ , stray and parasitic PCB capacitance) can be estimated at 4 to 5 pF (typical).

As an example, using a crystal with a required load capacitance ( $C_L$ ) of 18 pF, the calculation is as follows (see [Figure 6-4](#)):

$$C_1 = C_2 = 2 \times (C_L - C_S) = 2 \times (18 \text{ pF} - 4.5 \text{ pF}) = 27 \text{ pF}$$

Place a 27-pF capacitor on pins 30 and 31 to ensure proper crystal oscillator operation.

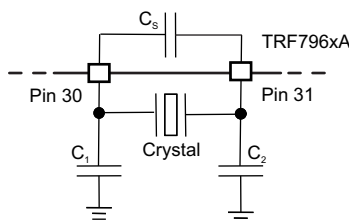


Figure 6-4. Crystal Block Diagram

Table 6-5 shows the minimum characteristics recommended for any crystal used with TRF7962A.

**Table 6-5. Minimum Crystal Recommendations**

| PARAMETER                   | SPECIFICATION |
|-----------------------------|---------------|
| Frequency                   | 13.56 MHz     |
| Mode of operation           | Fundamental   |
| Type of resonance           | Parallel      |
| Frequency tolerance         | ±20 ppm       |
| Aging                       | <5 ppm/year   |
| Operation temperature range | –40°C to 85°C |

As an alternative, an external clock oscillator source can be connected to pin 31 to provide the system clock, and pin 30 can be left open.

## 6.9 Transmitter - Analog Section

The 13.56-MHz oscillator generates the RF signal for the PA stage. The power amplifier consists of a driver with selectable output resistance of 4  $\Omega$  or 8  $\Omega$  (typical). The transmit power levels are selectable between 100 mW (half power) or 200 mW (full power) when configured for 5-V automatic operation. Selection of the transmit power level is set by bit B4 in the Chip Status Control register (0x00). When configured for 3-V automatic operation, the transmit power level is typically in the range of 33 mW (half power) or 70 mW (full power).

The ASK modulation depth is controlled by bits B0, B1, and B2 in the Modulator and SYS\_CLK Control register (0x09). The ASK modulation depth range can be adjusted from 7% to 30% or 100% (OOK).

External control of the transmit modulation depth is possible by setting the ISO Control register (0x01) to direct mode. While operating the TRF7962A in direct mode, the transmit modulation is made possible by selecting the modulation type ASK or OOK at pin 12. External control of the modulation type is made possible only if enabled by setting B6 in the Modulator and SYS\_CLK Control register (0x09) to 1.

In normal operation mode, the length of the modulation pulse is defined by the protocol selected in the ISO Control register (0x01). In case of a high-Q antenna, the modulation pulse is typically prolonged, and the tag detects a longer pulse than intended. For such cases, the modulation pulse length must be corrected by using the TX Pulse Length register (0x06).

If the register contains all zeros, then the pulse length is governed by the protocol selection. If the register contains a value other than 0x00, the pulse length is equal to the value of the register multiplied by 73.7 ns. This means the pulse length can be adjusted from 73.7 ns to 18.8  $\mu$ s in 73.7-ns increments.

## 6.10 Transmitter - Digital Section

The digital part of the transmitter is a mirror of the receiver. The settings controlled the ISO Control register (0x01) are applied to the transmitter just like the receiver. In the TRF7962A default mode (ISO Mode), the TRF7962A automatically adds all the special signals like start of communication, end of communication, SOF, EOF, parity bits and CRC bytes.

The data is then coded to modulation pulse levels and sent to the RF output stage modulation control unit. Just like with the receiver, this means that the external system MCU only must load the FIFO with data and all the microcoding is done automatically, again saving the firmware developer code space and time. Additionally, all the registers used for transmit parameter control are automatically preset to optimum values when a new selection is entered into the ISO Control register (0x01).

### NOTE

The FIFO must be reset before starting any transmission with direct command 0x0F.

There are two ways to start the transmit operation:

- Send the transmit command and the number of bytes to be transmitted first, and then start to send the data to the FIFO. The transmission starts when first data byte is written into the FIFO.
- Load the number of bytes to be sent into registers 0x1D and 0x1E and load the data to be sent into the FIFO (address 0x1F), followed by sending a transmit command (see Direct Commands section). The transmission then starts when the transmit command is received.

#### NOTE

If the data length is longer than the FIFO, the external system MCU is warned when the majority of data from the FIFO was already transmitted by sending an interrupt request with flag in IRQ register to indicate a FIFO low or high status. The external system should respond by loading next data packet into the FIFO.

At the end of a transmit operation, the external system MCU is notified by interrupt request (IRQ) with a flag in the IRQ register (0x0C) indicating TX is complete (example value = 0x80).

## 6.11 Transmitter – External Power Amplifier or Subcarrier Detector

The TRF7962A can be used in conjunction with an external TX power amplifier or external subcarrier detector for the receiver path. If this is the case, Bit B6 of the Regulator and I/O Control register (0x0B) must be set to 1. This setting has two functions: First, to provide a modulated signal for the transmitter, if needed. Second, to configure the TRF7962A receiver inputs for an external demodulated subcarrier input. The design of an external power amplifier requires detailed RF knowledge. There are also readily designed and certified high-power HF reader modules on the market.

## 6.12 Communication Interface

### 6.12.1 General Introduction

The communication interface to the reader can be configured in two ways: with a eight line parallel interface (D0:D7) plus DATA\_CLK, or with a 3- or 4-wire Serial Peripheral Interface (SPI). The SPI interface uses traditional master out/slave in (MOSI), master in/slave out (MISO), IRQ, and DATA\_CLK lines. The SPI can be operated with or without using the slave select line.

These communication modes are mutually exclusive, which means that only one mode can be used at a time in the application.

When the SPI interface is selected, the unused I/O\_2, I/O\_1, and I/O\_0 pins must be hard-wired according to [Table 6-6](#). At power up, the TRF7962A IC samples the status of these three pins and then enters one of the possible SPI modes in [Table 6-6](#).

samples the status of these three pins. If they are not the same (all high or all low), the IC enters one of the possible SPI modes.

The TRF7962A always behaves as the slave, while the microcontroller (MCU) behaves as the master device. The MCU initiates all communications with the TRF7962A. The TRF7962A makes use of the Interrupt Request (IRQ) pin in both parallel and SPI modes to prompt the MCU for servicing attention.

**Table 6-6. Pin Assignment in Parallel and Serial Interface Connection or Direct Mode**

| PIN      | PARALLEL | PARALLEL DIRECT                                  | SPI WITH SS                               | SPI WITHOUT SS                            |
|----------|----------|--------------------------------------------------|-------------------------------------------|-------------------------------------------|
| DATA_CLK | DATA_CLK | DATA_CLK                                         | DATA_CLK from master                      | DATA_CLK from master                      |
| I/O_7    | A/D[7]   |                                                  | MOSI <sup>(1)</sup> = data in (reader in) | MOSI <sup>(1)</sup> = data in (reader in) |
| I/O_6    | A/D[6]   | Direct mode, data out (subcarrier or bit stream) | MISO <sup>(2)</sup> = data out (MCU out)  | MISO <sup>(2)</sup> = data out (MCU out)  |

(1) MOSI = Master out, slave in

(2) MISO = Master in, slave out

**Table 6-6. Pin Assignment in Parallel and Serial Interface Connection or Direct Mode (continued)**

| PIN       | PARALLEL      | PARALLEL DIRECT                     | SPI WITH SS                      | SPI WITHOUT SS     |
|-----------|---------------|-------------------------------------|----------------------------------|--------------------|
| I/O_5 (3) | A/D[5]        | Direct mode, strobe (bit clock out) | See <sup>(3)</sup>               | See <sup>(3)</sup> |
| I/O_4     | A/D[4]        |                                     | SS (slave select) <sup>(4)</sup> | –                  |
| I/O_3     | A/D[3]        | –                                   | –                                | –                  |
| I/O_2     | A/D[2]        | –                                   | At VDD                           | At VDD             |
| I/O_1     | A/D[1]        | –                                   | At VDD                           | At VSS             |
| I/O_0     | A/D[0]        | –                                   | At VSS                           | At VSS             |
| IRQ       | IRQ interrupt | IRQ interrupt                       | IRQ interrupt                    | IRQ interrupt      |

- (3) The I/O\_5 pin is used only for information when data is put out of the chip (for example, reading 1 byte from the chip). It is necessary first to write in the address of the register (8 clocks) and then to generate another 8 clocks for reading out the data. The I/O\_5 pin goes high during the second 8 clocks. But for normal SPI operations I/O\_5 pin is not used.
- (4) The slave select pin is active low.

Communication is initialized by a start condition, which is expected to be followed by an Address/Command word (Adr/Cmd). The Adr/Cmd word is 8 bits long, and [Table 6-7](#) describes its format.

**Table 6-7. Address/Command Word Bit Distribution**

| BIT | DESCRIPTION             | BIT FUNCTION               | ADDRESS | COMMAND |
|-----|-------------------------|----------------------------|---------|---------|
| B7  | Command control bit     | 0 = Address<br>1 = Command | 0       | 1       |
| B6  | Read/Write              | 1 = Read<br>0 = Write      | R/W     | 0       |
| B5  | Continuous address mode | 1 = Continuous mode        | R/W     | 0       |
| B4  | Address/command bit 4   |                            | Adr 4   | Cmd 4   |
| B3  | Address/command bit 3   |                            | Adr 3   | Cmd 3   |
| B2  | Address/command bit 2   |                            | Adr 2   | Cmd 2   |
| B1  | Address/command bit 1   |                            | Adr 1   | Cmd 1   |
| B0  | Address/command bit 0   |                            | Adr 0   | Cmd 0   |

The MSB (bit 7) determines if the word is to be used as a command or as an address. The last two columns of [Table 6-7](#) list the function of the separate bits if either address or command is written. Data is expected once the address word is sent. In continuous address mode (continuous mode = 1), the first data that follows the address is written (or read) to (from) the given address. For each additional data, the address is incremented by one. Continuous mode can be used to write to a block of control registers in a single stream without changing the address; for example, setup of the predefined standard control registers from the MCU nonvolatile memory to the reader. In noncontinuous address mode (simple addressed mode), only one data word is expected after the address.

Address Mode is used to write or read the configuration registers or the FIFO. When writing more than 12 bytes to the FIFO, the Continuous Address Mode should be set to 1.

The Command Mode is used to enter a command that results in reader action (for example, initialize transmission, enable reader, and turn reader on or off).

The following examples show the expected communications between an MCU and the TRF7962A.

Table 6-8 lists the format of a continuous address register read, and Figure 6-5 and Figure 6-6 show examples.

**Table 6-8. Continuous Address Mode**

| Start | Adr x | Data(x) | Data(x+1) | Data(x+2) | Data(x+3) | Data(x+4) | ... | Data(x+n) | StopCont |
|-------|-------|---------|-----------|-----------|-----------|-----------|-----|-----------|----------|
|-------|-------|---------|-----------|-----------|-----------|-----------|-----|-----------|----------|

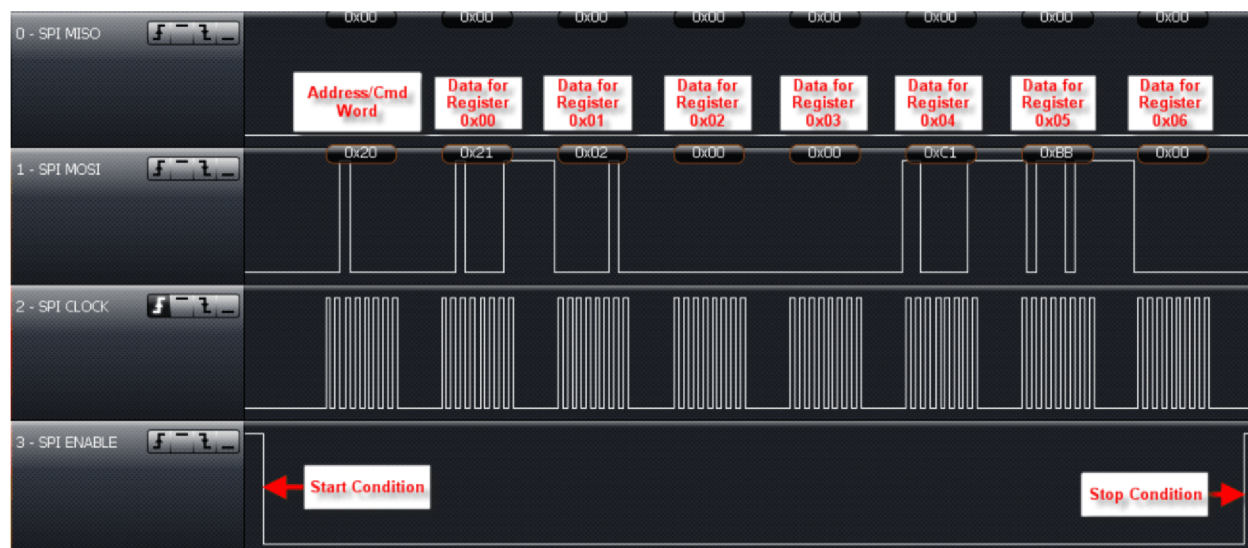


**Figure 6-5. Continuous Address Register Write Example Starting With Register 0x00 (Using SPI With SS Mode)**

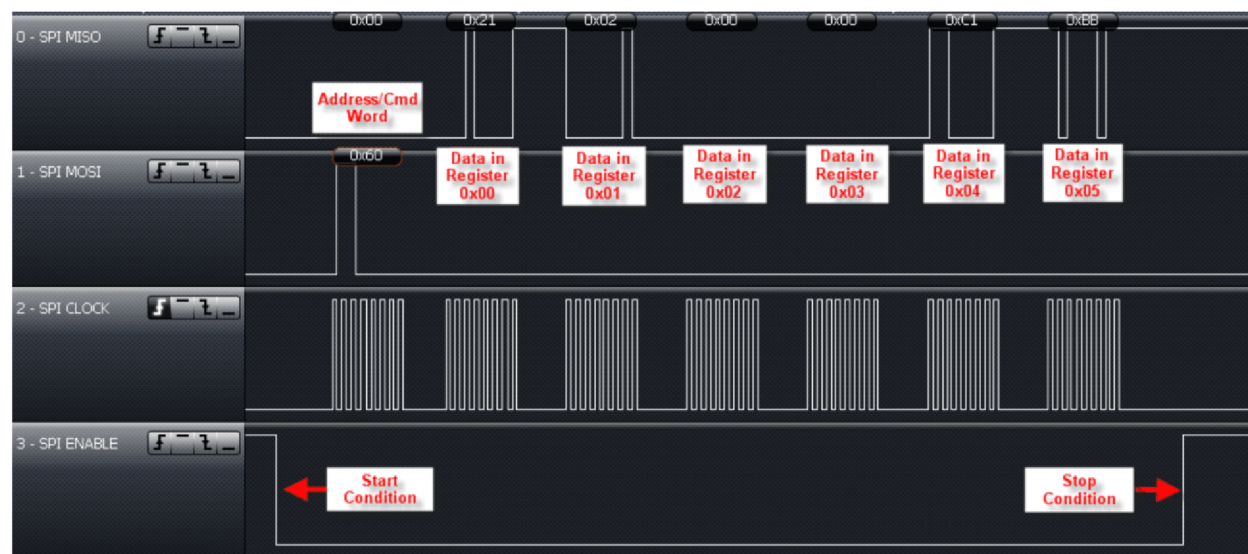


**Figure 6-6. Continuous Address Register Read Example Starting With Register 0x00 (Using SPI With SS Mode)**

Table 6-9 lists the format of a single address register read, and Figure 6-7 and Figure 6-8 show examples.

Table 6-9. Noncontinuous Address Mode (Single Address Mode)

| Start | Adr x | Data(x) | Adr y | Data(y) | ... | Adr z | Data(z) | StopSgl |
|-------|-------|---------|-------|---------|-----|-------|---------|---------|
|-------|-------|---------|-------|---------|-----|-------|---------|---------|

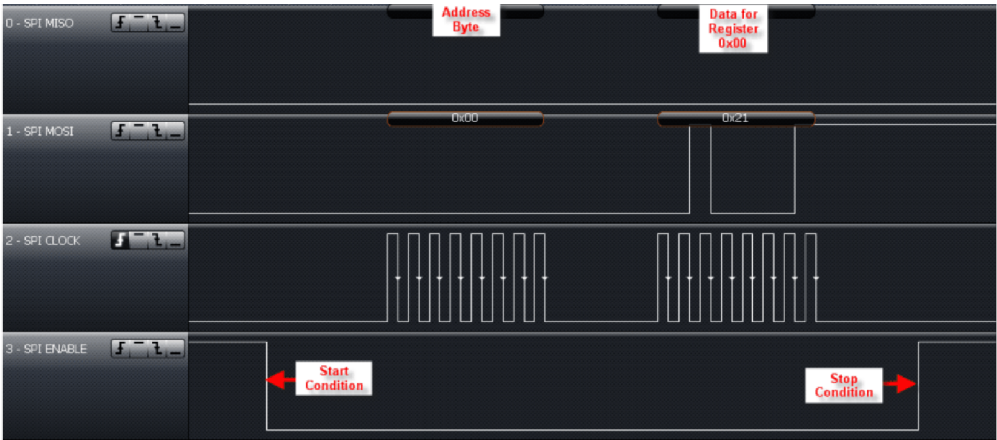


Figure 6-7. Single Address Register Write Example of Register 0x00 (Using SPI With SS Mode)

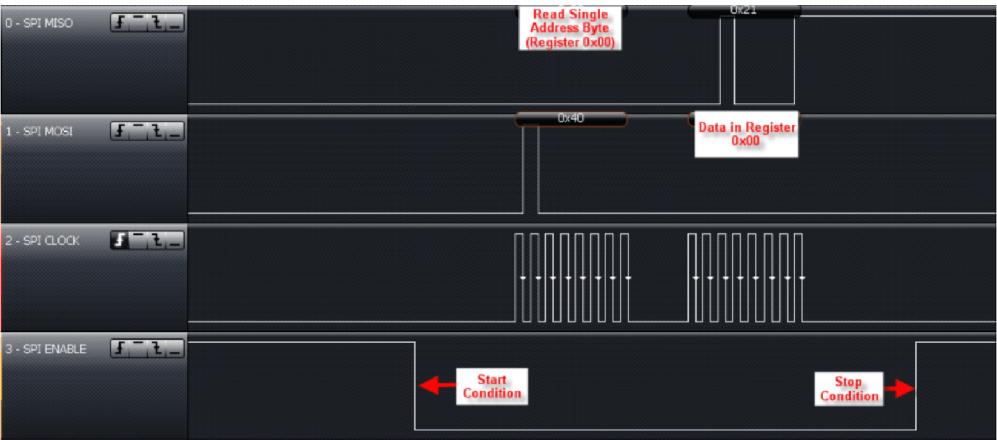


Figure 6-8. Single Address Register Read Example of Register 0x00 (Using SPI With SS Mode)

Table 6-10 lists the format of the direct command mode, and Figure 6-9 shows an example.

**Table 6-10. Direct Command Mode**

| Start | Cmd x | (Optional data or command) | Stop |
|-------|-------|----------------------------|------|
|-------|-------|----------------------------|------|

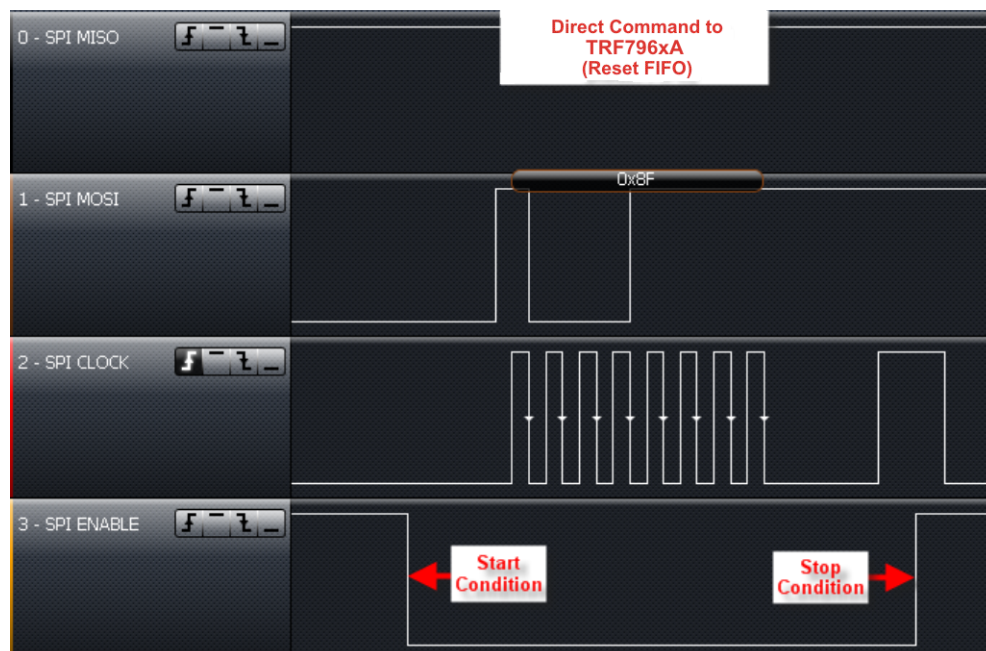


**Figure 6-9. Direct Command Example of Sending 0x0F (Reset) (Using SPI With SS Mode)**

The other Direct Command Codes from MCU to TRF7962A are described in [节 6.13](#).

### 6.12.2 FIFO Operation

The FIFO is a 12-byte register at address 0x1F with byte storage locations 0 to 11. FIFO data is loaded in a cyclical manner and can be cleared by a reset command (0x0F, see [Figure 6-9](#) showing this Direct Command).

Associated with the FIFO are two counters and three FIFO status flags. The first counter is a 4-bit FIFO byte counter (bits B0 to B3 in register 0x1C) that keeps track of the number of bytes loaded into the FIFO. If the number of bytes in the FIFO is  $n$ , the register value is  $n - 1$  (number of bytes in FIFO register). If 8 bytes are in the FIFO, the FIFO counter (bits B0 to B3 in register 0x1C) has the value 7.

A second counter (12 bits wide) indicates the number of bytes being transmitted (registers 0x1D and 0x1E) in a data frame. An extension to the transmission-byte counter is a 4-bit broken-byte counter also provided in register 0x1E (bits B0 to B3). Together these counters make up the TX length value that determines when the reader generates the EOF byte.

FIFO status flags are as follows:

1. **FIFO overflow** (bit B4 of register 0x1C): Indicates that the FIFO was loaded too soon
2. **FIFO level too low** (bit B5 of register 0x1C): Indicates that only three bytes are left to be transmitted (Can be used during transmission.)
3. **FIFO level high** (bit B6 of register 0x1C): Indicates that nine bytes are already loaded into the FIFO (Can be used during reception to generate a FIFO reception IRQ. This is to notify the MCU to service the reader in time to ensure a continuous data stream.)

During transmission, the FIFO is checked for an almost-empty condition, and during reception for an almost-full condition. The maximum number of bytes that can be loaded into the FIFO in a single sequence is 12 bytes.

#### NOTE

The number of bytes in a frame, transmitted or received, can be greater than 12 bytes.

During transmission, the MCU loads the TRF7962A FIFO (or, during reception, the MCU removes data from the FIFO), and the FIFO counter counts the number of bytes being loaded into the FIFO. Meanwhile, the byte counter keeps track of the number of bytes being transmitted. An interrupt request is generated if the number of bytes in the FIFO is less than 3 or greater than 9, so that MCU can send new data or remove the data as necessary. The MCU also checks the number of data bytes to be sent, so as to not surpass the value defined in TX length bytes. The MCU also signals the transmit logic when the last byte of data is sent or was removed from the FIFO during reception. Transmission starts automatically after the first byte is written into FIFO.

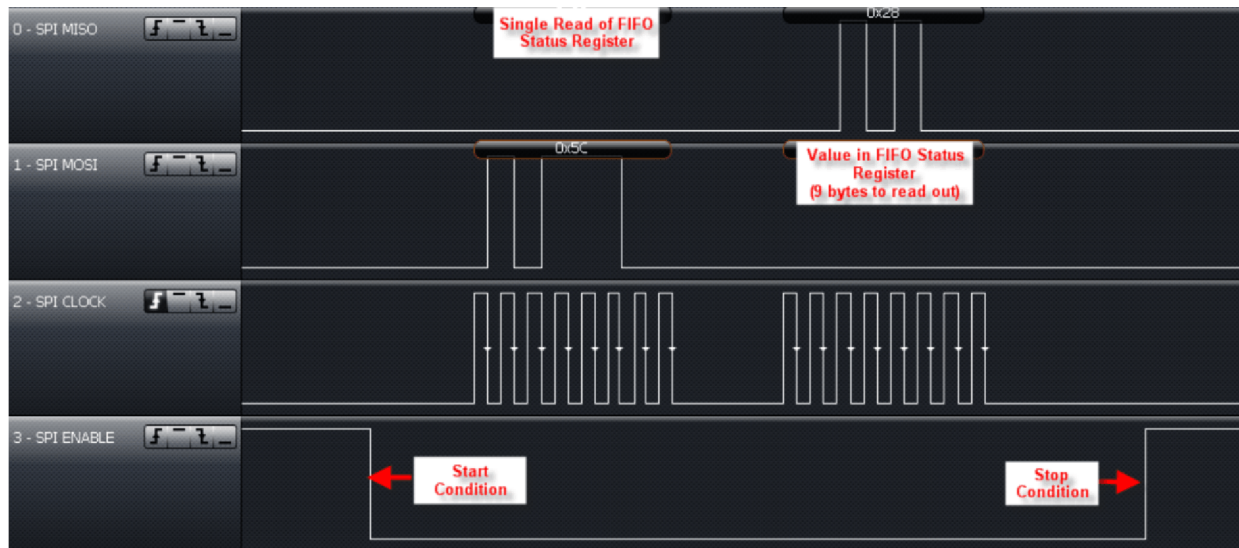


Figure 6-10. Checking the FIFO Status Register (Using SPI With SS Mode)

### 6.12.3 Parallel Interface Mode

In parallel mode, the start condition is generated on the rising edge of the I/O\_7 pin while the CLK is high.

This is used to reset the interface logic. Figure 6-11, Figure 6-12, and Figure 6-13 show the sequence of the data, with an 8-bit address word first, followed by data.

Communication is ended by:

- The StopSmpl condition, where a falling edge on the I/O\_7 pin is expected while CLK is high
- The StopCont condition, where the I/O\_7 pin must have a successive rising and falling edge while CLK is low to reset the parallel interface and be ready for the new communication sequence
- The StopSmpl condition is also used to terminate the direct mode.

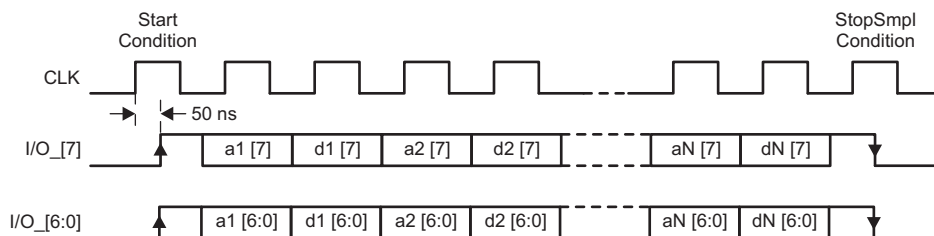


Figure 6-11. Parallel Interface Communication With Simple Stop Condition (StopSmpl)

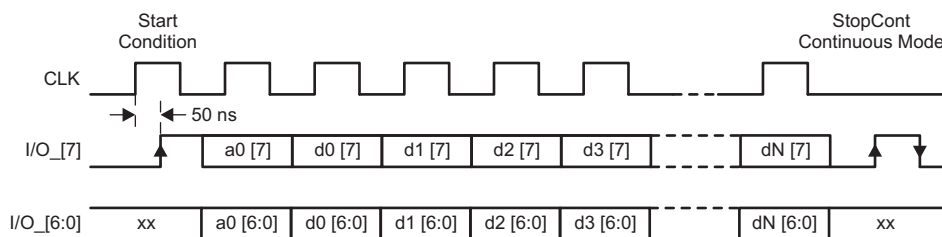


Figure 6-12. Parallel Interface Communication With Continuous Stop Condition (StopCont)

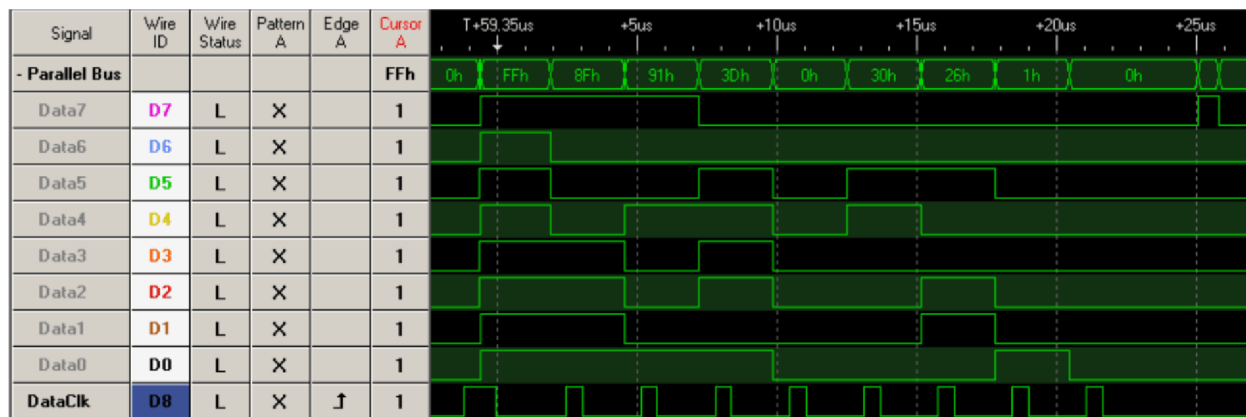


Figure 6-13. Parallel Interface Communication With Continuous Stop Condition

#### 6.12.4 Reception of Air Interface Data

At the start of a receive operation (when SOF is successfully detected), B6 is set in the IRQ Status register. An interrupt request is sent to the MCU at the end of the receive operation if the receive data string was shorter than or equal to 8 bytes. The MCU receives the interrupt request, then checks to determine the reason for the interrupt by reading the IRQ Status register (address 0x0C), after which the MCU reads the data from the FIFO.

If the received packet is longer than 8 bytes, the interrupt is sent before the end of the receive operation when the ninth byte is loaded into the FIFO (75% full). The MCU must read the FIFO status register (0x1C) to determine the number of bytes to be read from the FIFO. Next, the MCU must read the data in the FIFO. It is optional but recommended to read the FIFO Status register (0x1C) after reading the FIFO data to determine if the receive is complete. In the case of an IRQ\_FIFO, the MCU should expect either another IRQ\_FIFO or RX complete interrupt. This is repeated until an RX complete interrupt is generated.

If the reader detects a receive error, the corresponding error flag is set (framing error, CRC error) in the IRQ Status register, indicating to the MCU that reception was not completed correctly.

### 6.12.5 Data Transmission to MCU

Before beginning data transmission, the FIFO should always be cleared with a reset command (0x0F). Data transmission is initiated with a selected command (see [节 6.13](#)). The MCU then commands the reader to do a continuous write command (0x3D) (see [Table 6-7](#)) starting from register 0x1D. Data written into register 0x1D is the TX length byte 1 (upper and middle nibbles), while the following byte in register 0x1E is the TX length byte 2 (lower nibble and broken byte length). The TX byte length determines when the reader sends the EOF byte. After the TX length bytes are written, FIFO data is loaded in register 0x1F with byte storage locations 0 to 11. Data transmission begins automatically after the first byte is written into the FIFO. The loading of TX length bytes and the FIFO can be done with a continuous write command, as the addresses are sequential.

At the start of transmission, the flag B7 (IRQ\_TX) is set in the IRQ Status register. If the transmit data is shorter than or equal to 4 bytes, the interrupt is sent only at the end of the transmit operation. If the number of bytes to be transmitted is higher or equal to 5, then the interrupt is generated. This occurs also when the number of bytes in the FIFO reaches 3. The MCU should check the IRQ Status register and FIFO Status register and then load additional data to the FIFO, if needed. At the end of the transmit operation, an interrupt is sent to inform the MCU that the task is complete.

### 6.12.6 Serial Interface Communication (SPI)

When an SPI interface is used, I/O pins I/O\_2, I/O\_1, and I/O\_0 must be hard-wired as specified in [Table 6-6](#). On power up, the TRF7962A looks for the status of these pins; if they are not the same (not all high, or not all low), the reader enters into one of two possible SPI modes:

- SPI with slave select
- or
- SPI without slave select

The choice of one of these modes over the other should be made based on the available GPIOs and the desired control of the system.

The serial communications work in the same manner as the parallel communications with respect to the FIFO, except for the following condition. On receiving an IRQ from the reader, the MCU reads the TRF7962A IRQ Status register to determine how to service the reader. After this, the MCU must do a dummy read to clear the reader's IRQ Status register. The dummy read is required in SPI mode, because the reader's IRQ Status register needs an additional clock cycle to clear the register. This is not required in parallel mode, because the additional clock cycle is included in the Stop condition.

A procedure for a dummy read is as follows:

1. Starting the dummy read
  1. When using slave select (SS): set SS bit low
  2. When not using SS: start condition is when SCLK is high
2. Send address word to IRQ Status register (0x0C) with read and continuous address mode bits set to 1
3. Read 1 byte (8 bits) from IRQ Status register (0x0C)
4. Dummy read 1 byte from register 0Dh (collision position and interrupt mask)
5. Stopping the dummy read
  1. When using slave select (SS): set SS bit high
  2. When not using SS: stop condition when SCLK is high

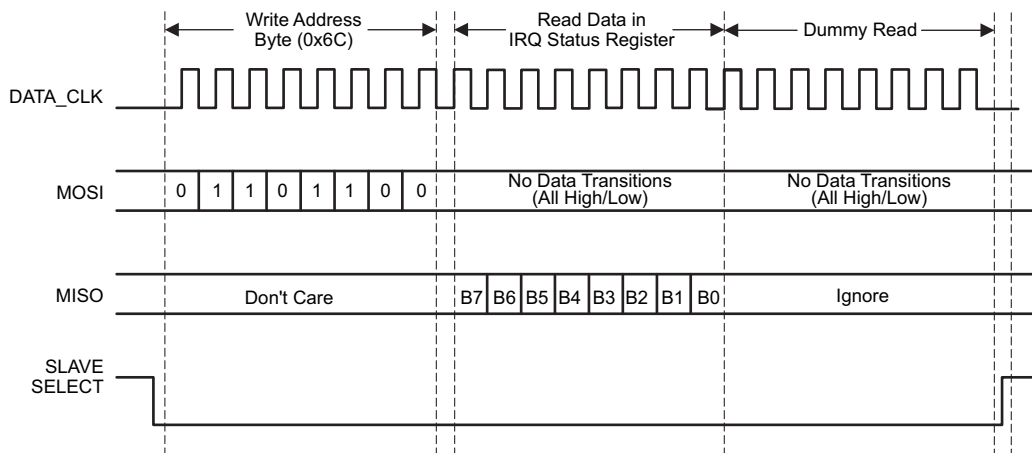


**Figure 6-14. Procedure for Dummy Read**

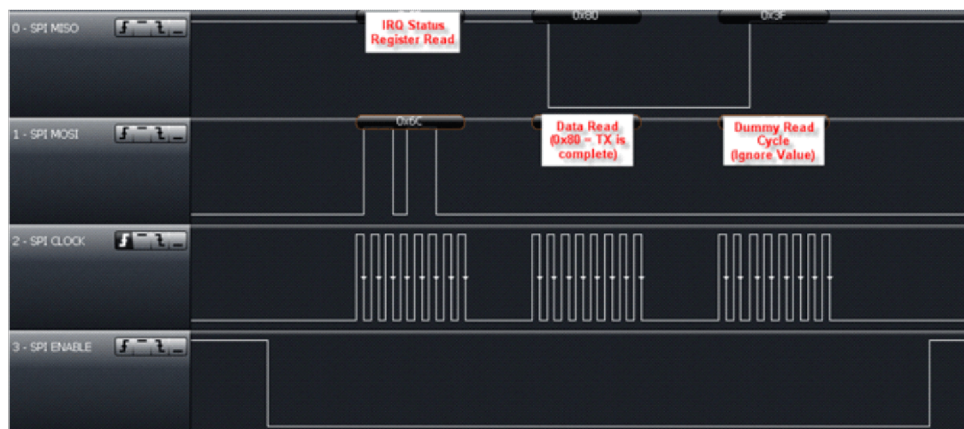


**Figure 6-15. Dummy Read Using SPI With SS**

#### 6.12.6.1 Serial Interface Mode Without Slave Select (SS)

The serial interface without the slave select pin must use delimiters for the start and stop conditions. Between these delimiters, the address, data, and command words can be transferred. All words must be 8 bits long with MSB transmitted first (see [Figure 6-16](#)).

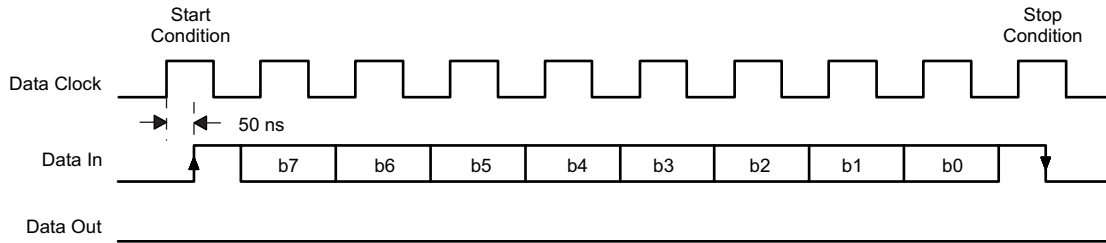


**Figure 6-16. SPI Without Slave Select Timing**

In this mode, a rising edge on data in (I/O\_7, pin 24) while SCLK is high resets the serial interface and prepares it to receive data. Data in can change only when SCLK is low, and it is read by the reader on the SCLK rising edge. Communication is terminated by the stop condition when the data in falling edge occurs during a high SCLK period.

### 6.12.6.2 Serial Interface Mode With Slave Select (SS)

The serial interface is in reset while the Slave Select signal is high. Serial data in (MOSI) changes on the falling edge and is validated in the reader on the rising edge (see [Figure 6-17](#)). Communication is terminated when the Slave Select signal goes high.

All words must be 8 bits long with the MSB transmitted first.

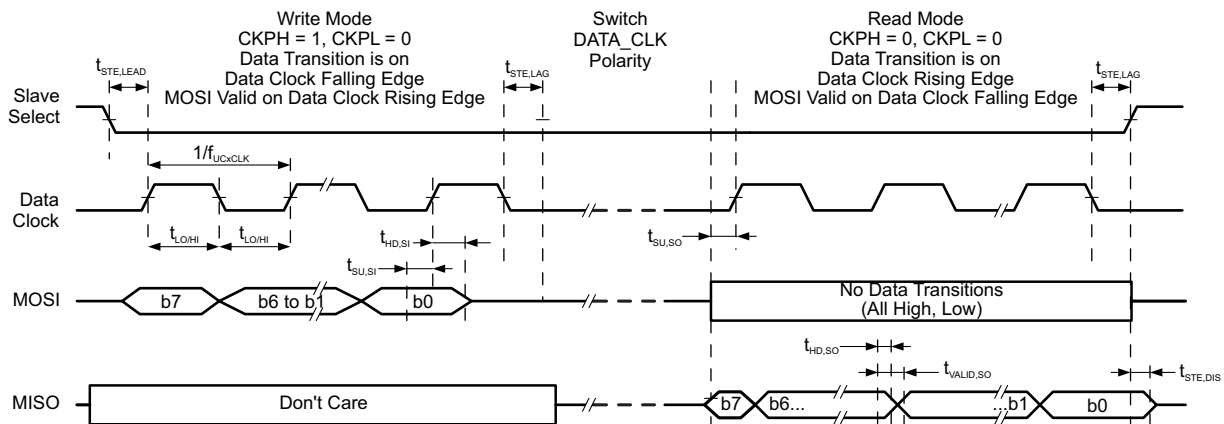


**Figure 6-17. SPI With Slave Select Timing**

The read command is sent out on the MOSI pin, MSB first, in the first eight clock cycles. MOSI data changes on the falling edge, and is validated in the reader on the rising edge, as shown in [Figure 6-17](#). During the write cycle, the serial data out (MISO) is not valid. After the last read command bit (B0) is validated at the eighth rising edge of SCLK, after half a clock cycle, valid data can be read on the MISO pin at the falling edge of SCLK. It takes eight clock edges to read out the full byte (MSB first).

When using the hardware SPI (for example, an MSP430 hardware SPI) to implement this feature, care must be taken to switch the SCLK polarity after write phase for proper read operation. The example clock polarity for the [Figure 6-17](#) shows the MSP430-specific environment in the write-mode and read-mode boxes. See the USART-SPI chapter for any specific microcontroller family for further information on the setting the appropriate clock polarity. This clock polarity switch must be done for all read (single or continuous) operations. The MOSI (serial data out) should not have any transitions (all high or all low) during the read cycle. The Slave Select should be low during the whole write and read operation.

See [Section 5.6, Switching Characteristics](#), for the timing values shown in [Figure 6-17](#).

[Figure 6-18](#) shows the continuous read operation.

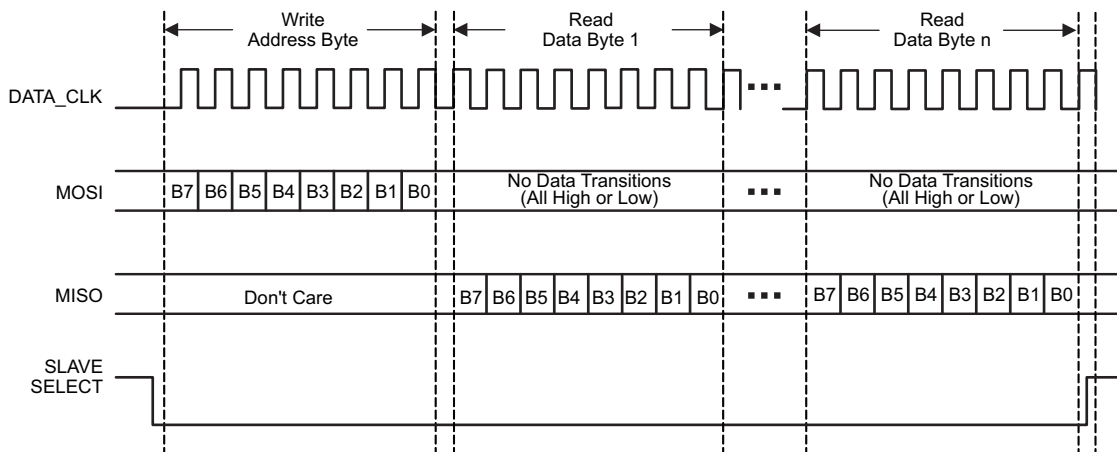


Figure 6-18. Continuous Read Operation Using SPI With Slave Select

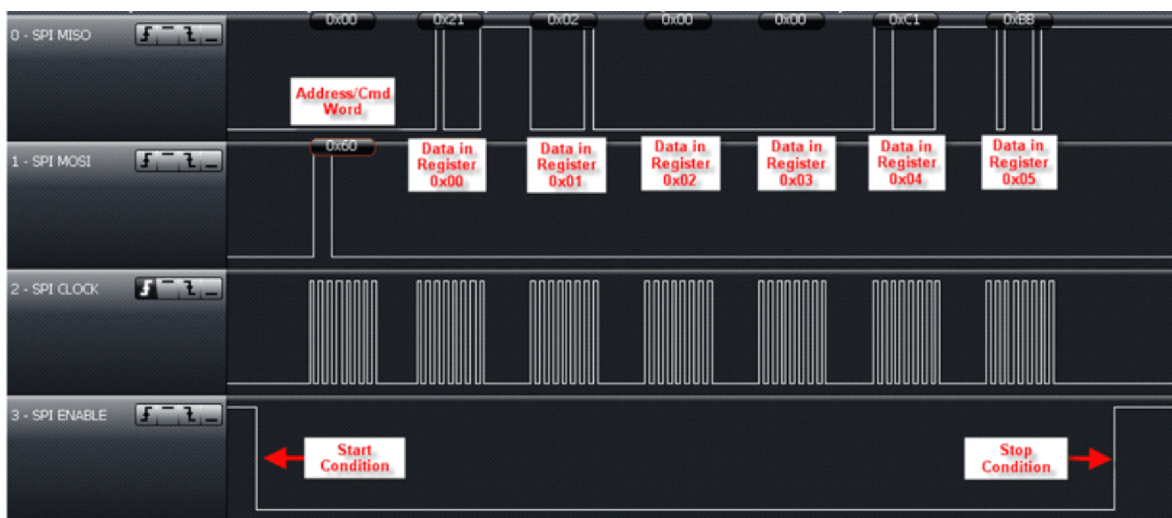


Figure 6-19. Continuous Read of Registers 0x00 to 0x05 Using SPI With SS

Figure 6-20 shows performing a Single Slot Inventory Command as an example. Reader registers (in this example) are configured for 5-VDC input and default operation. Full sequences for other settings and protocols can be downloaded from <http://www.ti.com/lit/zip/sloc240>.

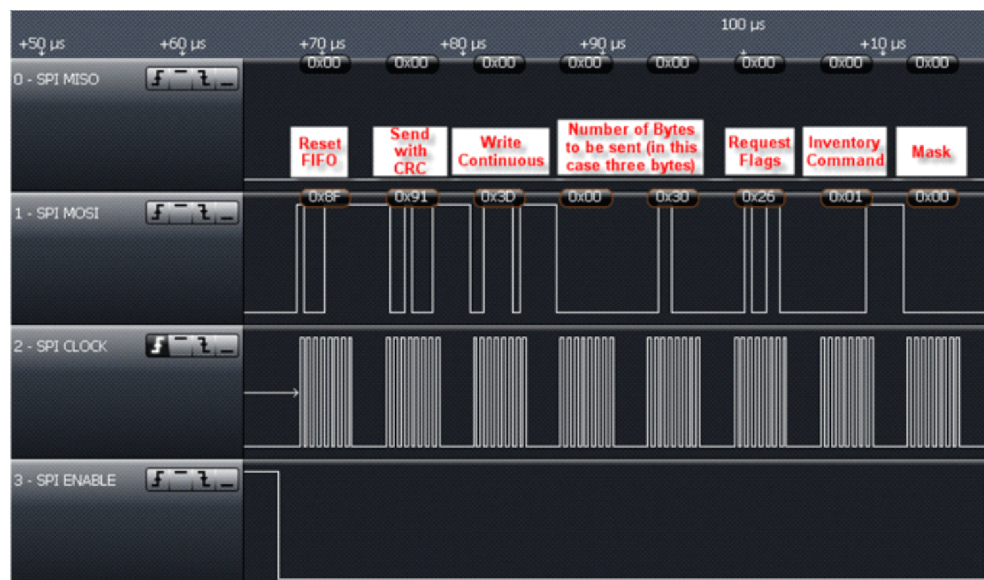


**Figure 6-20. Inventory Command Sent From MCU to TRF7962A**

The TRF7962A reads these bytes from the MCU and then sends out Request Flags, Inventory Command, and Mask over the air to the ISO/IEC 15693 transponder. After these three bytes have been transmitted, an interrupt occurs from the reader to indicate back to the MCU that the transmission has been completed. In the example shown in [Figure 6-21](#), this IRQ occurs approximately 1.6 ms after the SS line goes high after the Inventory command is sent out.

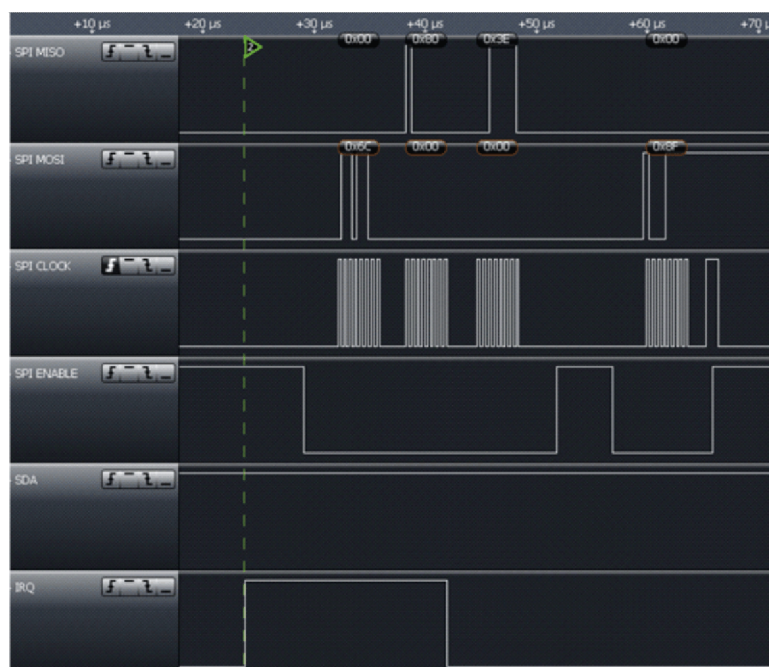


**Figure 6-21. IRQ After Inventory Command**

The IRQ Status register read (0x6C) yields 0x80, which indicates that TX is complete. This is followed by dummy clock and reset of FIFO with dummy clock. Then, if a tag is in the field and no error is detected by the reader, a second interrupt is expected and occurs (in this example) approximately 4 ms after first IRQ is read and cleared.

In the continuation of the example (see [Figure 6-22](#)), the IRQ Status register is read using method previously recommended, followed by a single read of the FIFO Status register, which indicates that there are at least 9 bytes to be read out.



**Figure 6-22. IRQ Status Register Read Followed by FIFO Status Register Read**

This is followed by a continuous read of the FIFO (see [Figure 6-23](#)). The first byte is 0x00 for no error. The next byte is the DSFID (usually shipped by manufacturer as 0x00), then the UID, shown here up to the next most significant byte (MSByte), the MFG code (0x07 to indicate TI silicon).

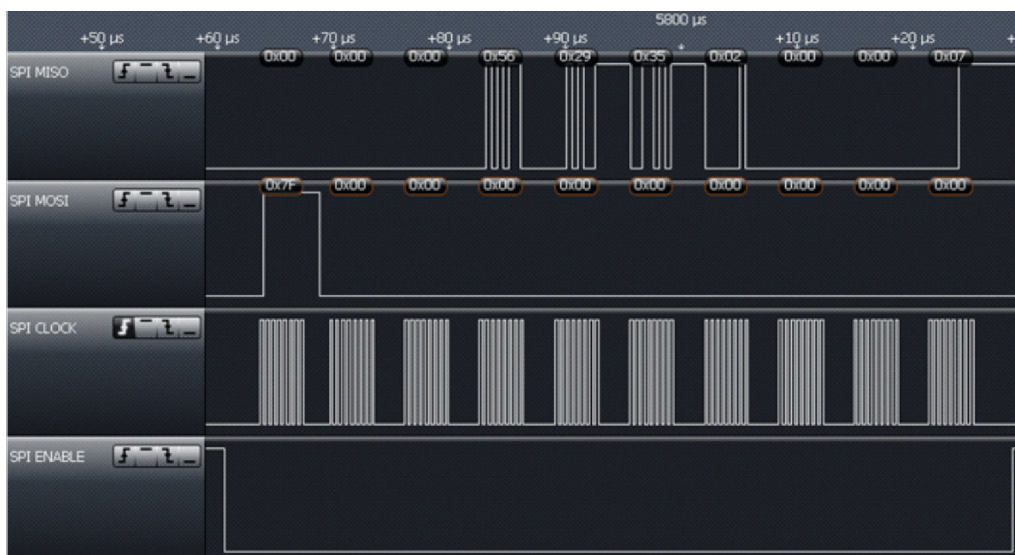


**Figure 6-23. Continuous Read of FIFO**

This is followed by another IRQ approximately 160  $\mu$ s later, as there is still one byte in FIFO, the MSB of the UID, which must be retrieved (see [Figure 6-24](#)). IRQ register read shows RX is complete and FIFO register status shows one byte available, as expected and it is the E0, indicating ISO/IEC 15693 transponder.

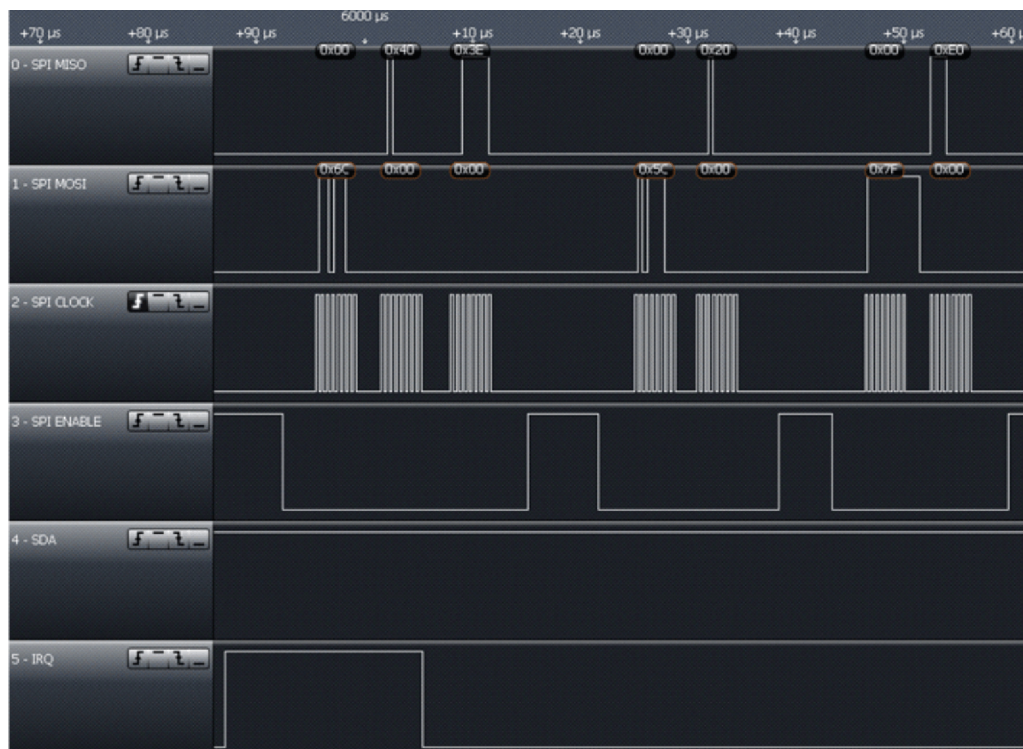


**Figure 6-24. IRQ With One Byte in FIFO**

TI recommends resetting the FIFO after receiving data. Additionally, the RSSI value of the tag can be read out at this time. In the example in [Figure 6-25](#), the transponder is very close to the antenna, so a value of 0x7E is recovered.



**Figure 6-25. Reset FIFO and Read RSSI**

### 6.12.7 Direct Mode

Direct mode lets the reader be configured in one of two ways:

Direct mode 0 (bit 6 = 0, as defined in ISO Control register) lets the application use only the front-end functions of the reader, bypassing the protocol implementation in the reader. For transmit functions, the application has direct access to the transmit modulator through the MOD pin (pin 14). On the receive side, the application has direct access to the subcarrier signal (digitized RF envelope signal) on I/O\_6 (pin 23).

Direct mode 1 (bit 6 = 1, as defined in ISO Control register) uses the subcarrier signal decoder of the selected protocol (as defined in ISO Control register). This means that the receive output is not the subcarrier signal but the decoded serial bit stream and bit clock signals. The serial data is available on I/O\_6 (pin 23), and the bit clock is available on I/O\_5 (pin 22). The transmit side is identical; the application has direct control over the RF modulation through the MOD input. This mode is provided so that the application can implement a protocol that has the same bit coding as one of the protocols implemented in the reader, but needs a different framing format.

To select direct mode, first choose which direct mode to enter by writing B6 in the ISO Control register. This bit determines if the receive output is the direct subcarrier signal (B6 = 0) or the serial data of the selected decoder. If B6 = 1, then the application must also define which protocol should be used for bit decoding by writing the appropriate setting in the ISO Control register.

The reader actually enters the direct mode when B6 (direct) is set to 1 in the Chip Status Control register. Direct mode starts immediately. The write command should not be terminated with a stop condition (see communication protocol), because the stop condition terminates the direct mode and clears B6. This is necessary as the direct mode uses one or two I/O pins (I/O\_6 and I/O\_5). Normal parallel communication is not possible in direct mode. Sending a stop condition terminates direct mode.

图 6-26 shows the different configurations available in direct mode.

- In mode 0, the reader is used as an AFE only, and protocol handling is bypassed.
- In mode 1, framing is not done, but SOF and EOF are present. This allows for a user-selectable framing level based on an existing ISO standard.
- In mode 2, data is ISO standard formatted. SOF, EOF, and error checking are removed, so the microprocessor receives only bytes of raw data through a 12-byte FIFO.

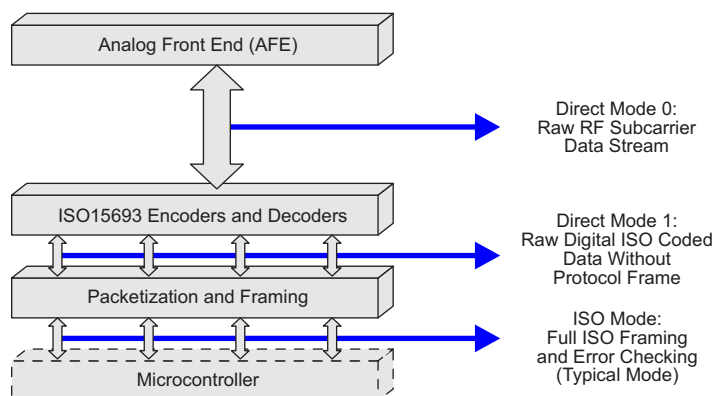


图 6-26. User-Configurable Modes

The steps to enter direct mode follow, using SPI with SS communication method only as one example, as direct modes are also possible with parallel and SPI without SS. The application must enter direct mode 0 to accommodate non-ISO standard compliant card type communications. direct mode can be entered at any time, so that if a card type started with ISO standard communications, then deviated from the standard after being identified and selected, the ability to go into direct mode 0 becomes very useful.

**Step 1:** Configure pins I/O\_0 to I/O\_2 for SPI with SS

**Step 2:** Set pin 12 of the TRF7962A (ASK/OOK pin) to 0 for ASK or 1 for OOK

**Step 3:** Program the TRF7962A registers

The following registers must be explicitly set before going into direct mode.

1. ISO Control register (0x01) to the appropriate standard:
  - 0x02 for ISO/IEC 15693 high data rate (26.48 kbps)
2. Modulator and SYS\_CLK Register (0x09) to the appropriate clock speed and modulation:
  - 0x21 for 6.78-MHz clock and OOK (100%) modulation
  - 0x20 for 6.78-MHz clock and ASK 10% modulation
  - 0x24 for 6.78-MHz clock and ASK 13% modulation
  - 0x25 for 6.78-MHz clock and ASK 16% modulation

See register 0x09 definition for all other possible values.

**Step 4:** Enter direct mode

The following registers must be reprogrammed to enter direct mode:

1. Set bit B6 of the Modulator and SYS\_CLK Control register (0x09) to 1.
2. Set bit B6 of the ISO Control register (0x01) to 0 for direct mode 0 (default its 0)
3. Set bit B6 of the Chip Status Control register (0x00) to 1 to enter direct mode (do not send a Stop condition after this command)

---

#### 注

- Do not terminate last write with a Stop condition. For SPI, this means that Slave Select (I/O\_4) continues to stay low.
  - Sending a Stop condition terminates the direct mode and clears bit B6 in the Chip Status Control register (0x00).
- 

#### 注

Access to registers, FIFO, and IRQ is not available during direct mode 0.

---

Remember that the reader enters direct mode 0 when bit 6 of the Chip Status Control register (0x00) is set to a 1, and it stays in direct mode 0 until a Stop condition is sent from the microcontroller.

---

#### 注

The write command should not be terminated with a Stop condition (for example, in SPI mode this is done by bringing the SS line high after the register write), because the Stop condition terminates the direct mode and clears bit 6 of the Chip Status Control register (0x00), making it a 0.

---

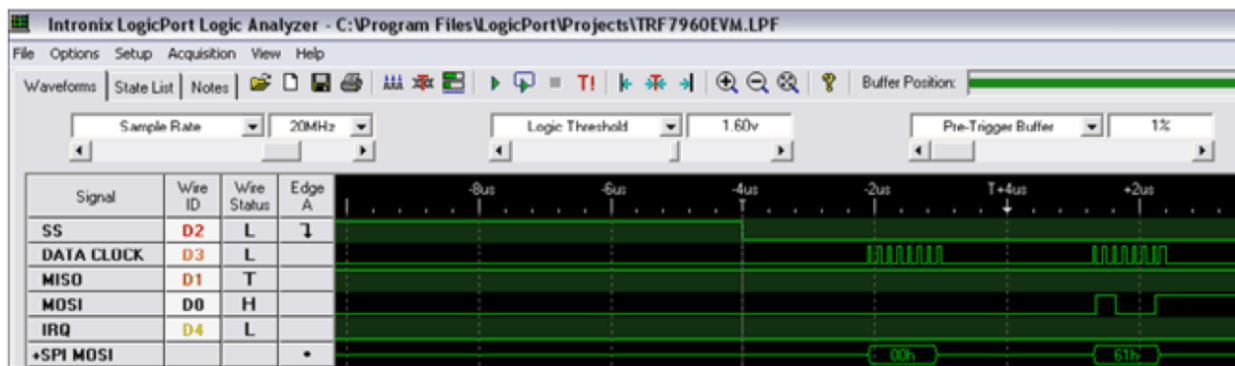


图 6-27. Entering Direct Mode 0

#### Step 5: Transmit data using direct mode

The user now has direct control over the RF modulation through the MOD input.

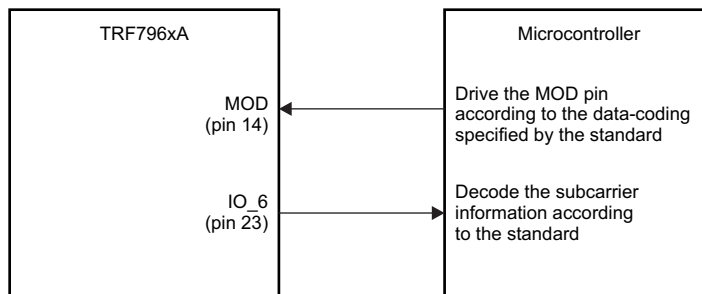


图 6-28. Control of RF Modulation Using MOD

The microcontroller is responsible for generating data according to the coding specified by the particular standard. The microcontroller must generate SOF, EOF, data, and CRC. In direct mode, the FIFO is not used and no IRQs are generated. See the applicable ISO standard to understand bit and frame definitions.

#### Step 6: Receive data using direct mode

After the TX operation is complete, the tag responds to the request and the subcarrier data is available on pin I/O\_6. The microcontroller must decode the subcarrier signal according to the standard. This includes decoding the SOF, data bits, CRC, and EOF. The CRC then must be checked to verify data integrity. The receive data bytes must be buffered locally.

#### Step 7: Exit direct mode 0

When an EOF is received, data transmission is over, and direct mode 0 can be terminated by sending a Stop condition (the SS signal goes high). The TRF7962A returns to ISO Mode (normal mode).

## 6.13 Direct Commands from MCU to Reader

### 6.13.1 Command Codes

表 6-11 lists the valid commands that the MCU can send to the reader.

表 6-11. Command Codes

| COMMAND CODE | COMMAND                              | COMMENTS                     |
|--------------|--------------------------------------|------------------------------|
| 0x00         | Idle                                 |                              |
| 0x03         | Software Initialization              | Same as power-on reset       |
| 0x0F         | Reset FIFO                           |                              |
| 0x10         | Transmission Without CRC             |                              |
| 0x11         | Transmission With CRC                |                              |
| 0x14         | End of Frame/Transmit Next Time Slot | Used for ISO/IEC 15693 only  |
| 0x16         | Block Receiver                       |                              |
| 0x17         | Enable Receiver                      |                              |
| 0x18         | Test Internal RF                     | RSSI at RX input with TX off |
| 0x19         | Test External RF                     | RSSI at RX input with TX off |
| 0x1A         | Receiver Gain Adjust                 |                              |

The command code values from 表 6-11 are substituted in 表 6-12, Bits 0 to 4. Also, the most significant bit (MSB) in 表 6-12 must be set to 1.

表 6-12. Address/Command Word Bit Distribution

| BIT | DESCRIPTION             | BIT FUNCTION               | ADDRESS         | COMMAND  |
|-----|-------------------------|----------------------------|-----------------|----------|
| B7  | Command control bit     | 0 = Address<br>1 = Command | 0               | 1        |
| B6  | Read/Write              | 0 = Write<br>1 = Read      | R/W             | 0        |
| B5  | Continuous address mode |                            | Continuous mode | Not used |
| B4  | Address/Command bit 4   |                            | Adr 4           | Cmd 4    |
| B3  | Address/Command bit 3   |                            | Adr 3           | Cmd 3    |
| B2  | Address/Command bit 2   |                            | Adr 2           | Cmd 2    |
| B1  | Address/Command bit 1   |                            | Adr 1           | Cmd 1    |
| B0  | Address/Command bit 0   |                            | Adr 0           | Cmd 0    |

The MSB determines if the word is to be used as a command or address. The last two columns of 表 6-12 show the function of separate bits depending on whether address or command is written. Command mode is used to enter a command resulting in reader action (for example, initialize transmission, enable reader, or turn the reader on or off).

### 6.13.2 Reset FIFO (0x0F)

The reset command clears the FIFO contents and FIFO Status register (0x1C). It also clears the register storing the collision error location (0x0E).

### 6.13.3 Transmission With CRC (0x11)

The transmission command must be sent first, followed by transmission length bytes, and FIFO data. The reader starts transmitting after the first byte is loaded into the FIFO. The CRC byte is included in the transmitted sequence.

#### 6.13.4 Transmission Without CRC (0x10)

The transmission command must be sent first, followed by transmission length bytes, and FIFO data. The reader starts transmitting after the first byte is loaded into the FIFO. This is the same as described in [节 6.13.3](#), except that the CRC is not included.

#### 6.13.5 Transmit Next Time Slot (0x14)

When this command is received, the reader transmits the next slot command. The next slot sign is defined by the protocol selection. This command is used by the ISO/IEC 15693 protocol.

#### 6.13.6 Block Receiver (0x16)

The block receiver command puts the digital part of receiver (bit decoder and framer) in reset mode. This is useful in an extremely noisy environment, where the noise level could otherwise cause a constant switching of the subcarrier input of the digital part of the receiver. The receiver (if not in reset) would try to catch a SOF signal, and if the noise pattern matched the SOF pattern, an interrupt would be generated, falsely signaling the start of a receive operation. A constant flow of interrupt requests can be a problem for the external system (MCU), so the external system can stop this by putting the receive decoders in reset mode.

The reset mode can be terminated in two ways:

The external system can send the enable receiver command (see [节 6.13.7](#)).

The reset mode is automatically terminated at the end of a transmit operation.

The receiver can stay in reset after end of transmit if the RX Wait Time register (0x08) is set. In this case, the receiver is enabled at the end of the wait time following the transmit operation.

#### 6.13.7 Enable Receiver (0x17)

This command clears the reset mode in the digital part of the receiver if the reset mode was entered by the block receiver command.

#### 6.13.8 Test Internal RF (RSSI at RX Input With TX On) (0x18)

The level of the RF carrier at RF\_IN1 and RF\_IN2 inputs is measured. The operating range is 300 mV<sub>P</sub> to 2.1 V<sub>P</sub> (the step size is 300 mV). The two values are reported in the RSSI Levels register (0x0F). The command is intended for diagnostic purposes to set correct RF\_IN levels. Optimum RFIN input level is approximately 1.6 V<sub>P</sub> or code 5 to 6. The nominal relationship between the RF peak level and RSSI code is described in [表 6-13](#) and in [Section 6.7.1.1](#).

#### 注

If the command is executed immediately after power-up and before any communication with tag was performed, the command must be preceded by the Enable RX command. The Check RF commands require full operation, so the receiver must be activated by enable receive or by a normal tag communication for the Check RF command to work properly.

**表 6-13. Test Internal RF**

|                                 |     |     |     |      |      |      |      |
|---------------------------------|-----|-----|-----|------|------|------|------|
| <b>RF_IN1 (mV<sub>P</sub>):</b> | 300 | 600 | 900 | 1200 | 1500 | 1800 | 2100 |
| <b>Decimal Code:</b>            | 1   | 2   | 3   | 4    | 5    | 6    | 7    |
| <b>Binary Code:</b>             | 001 | 010 | 011 | 001  | 101  | 011  | 111  |

### 6.13.9 Test External RF (RSSI at RX Input With TX Off) (0x19)

This command can be used in active mode when the RF receiver is on but RF output is off. This means bit B1 = 1 in the Chip Status Control register. The level of RF signal received on the antenna is measured and reported in the RSSI Levels register (0x0F). The relation between the 3-bit code and the external RF field strength [A/m] must be determinate by calculation or by experiments for each antenna type, because the antenna Q and connection to the RF input influence the result. 表 6-14 and Section 6.7.1.2 describe the nominal relation between the RF peak-to-peak voltage in the RF\_IN1 input and RSSI code, respectively.

#### 注

If the command is executed immediately after power-up and before any communication with tag was performed, the command must be preceded by the Enable RX command. The Check RF commands require full operation, so the receiver must be activated by enable RX or by a normal tag communication for the Check RF command to work properly.

表 6-14. Test External RF

|                                 |     |     |     |     |     |     |     |
|---------------------------------|-----|-----|-----|-----|-----|-----|-----|
| <b>RF_IN1 (mV<sub>p</sub>):</b> | 40  | 60  | 80  | 100 | 140 | 180 | 300 |
| <b>Decimal Code:</b>            | 1   | 2   | 3   | 4   | 5   | 6   | 7   |
| <b>Binary Code:</b>             | 001 | 010 | 011 | 001 | 101 | 011 | 111 |

### 6.13.10 Register Preset

After power-up and the EN pin low-to-high transition, the reader is in the default mode. The default configuration is ISO/IEC 15693, single subcarrier, high data rate, 1-out-of-4 operation. The low-level option registers (0x02 to 0x0B) are automatically set to adapt the circuitry optimally to the appropriate protocol parameters. When entering another protocol (by writing to the ISO Control register), the low-level option registers are automatically configured to the new protocol parameters. After selecting the protocol, it is possible to change some low-level register contents if needed. However, changing to another protocol and then back reloads the default settings; therefore, the custom settings must be reloaded.

The Clo0 and Clo1 bits in the Modulator and SYS\_CLK Control register (0x09), which define the microcontroller frequency available on the SYS\_CLK pin, are the only 2 bits in the configuration registers that are not cleared during protocol selection.

## 6.14 Register Description

### 6.14.1 Register Overview

表 6-15 lists the registers available in the TRF7962A. These registers are described in the following sections.

**表 6-15. Register Overview**

| ADDRESS<br>(hex)                     | REGISTER                                       | READ/WRITE | SECTION                      |
|--------------------------------------|------------------------------------------------|------------|------------------------------|
| <b>Main Control Registers</b>        |                                                |            |                              |
| 0x00                                 | Chip Status Control                            | R/W        | <a href="#">节 6.14.1.1.1</a> |
| 0x01                                 | ISO Control                                    | R/W        | <a href="#">节 6.14.1.1.2</a> |
| <b>Protocol Subsetting Registers</b> |                                                |            |                              |
| 0x06                                 | TX Pulse-Length Control                        | R/W        | <a href="#">节 6.14.1.2.1</a> |
| 0x07                                 | RX No Response Wait                            | R/W        | <a href="#">节 6.14.1.2.2</a> |
| 0x08                                 | RX Wait Time                                   | R/W        | <a href="#">节 6.14.1.2.3</a> |
| 0x09                                 | Modulator and SYS_CLK Control                  | R/W        | <a href="#">节 6.14.1.2.4</a> |
| 0x0A                                 | RX Special Setting                             | R/W        | <a href="#">节 6.14.1.2.5</a> |
| 0x0B                                 | Regulator and I/O Control                      | R/W        | <a href="#">节 6.14.1.2.6</a> |
| <b>Status Registers</b>              |                                                |            |                              |
| 0x0C                                 | IRQ Status                                     | R          | <a href="#">节 6.14.1.3.1</a> |
| 0x0D                                 | Collision Position and Interrupt Mask Register | R/W        | <a href="#">节 6.14.1.3.2</a> |
| 0x0E                                 | Collision Position                             | R          | <a href="#">节 6.14.1.3.2</a> |
| 0x0F                                 | RSSI Levels and Oscillator Status              | R          | <a href="#">节 6.14.1.3.3</a> |
| <b>FIFO Registers</b>                |                                                |            |                              |
| 0x1A                                 | Test                                           | R/W        | <a href="#">节 6.14.1.4.1</a> |
| 0x1B                                 | Test                                           | R/W        | <a href="#">节 6.14.1.4.2</a> |
| 0x1C                                 | FIFO Status                                    | R          | <a href="#">节 6.14.1.5.1</a> |
| 0x1D                                 | TX Length Byte1                                | R/W        | <a href="#">节 6.14.1.5.2</a> |
| 0x1E                                 | TX Length Byte2                                | R/W        | <a href="#">节 6.14.1.5.2</a> |
| 0x1F                                 | FIFO I/O Register                              | R/W        |                              |

### 6.14.1.1 Main Configuration Registers

#### 6.14.1.1.1 Chip Status Control Register (0x00)

表 6-16 describes the bit fields of the Chip Status Control register. This register controls the power mode, RF on or off, AM or PM, and direct mode.

**Default Value:** 0x01, set at EN = L or POR = H

**表 6-16. Chip Status Control Register (0x00)**

| BIT NO. | BIT NAME | FUNCTION                                              | DESCRIPTION                                                                                                                                                                               |
|---------|----------|-------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B7      | stby     | 1 = Standby mode                                      | Standby mode keeps all supply regulators and the 13.56-MHz SYS_CLK oscillator running (typical start-up time to full operation is 100 $\mu$ s).                                           |
|         |          | 0 = Active mode                                       | Active mode (default)                                                                                                                                                                     |
| B6      | direct   | 1 = Direct mode 0 or 1                                | Provides user direct access to AFE (direct mode 0) or lets the user add custom framing (direct mode 1). Bit 6 of the ISO Control register must be set before entering direct mode 0 or 1. |
|         |          | 0 = ISO mode (default)                                | Uses SPI or parallel communication with automatic framing and ISO decoders                                                                                                                |
| B5      | rf_on    | 1 = RF output active                                  | Transmitter on, receivers on                                                                                                                                                              |
|         |          | 0 = RF output not active                              | Transmitter off                                                                                                                                                                           |
| B4      | rf_pwr   | 1 = Half output power                                 | TX_OUT (pin 5) = 8- $\Omega$ output impedance<br>P = 100 mW (+20 dBm) at 5 V, P = 33 mW (+15 dBm) at 3.3 V                                                                                |
|         |          | 0 = Full output power                                 | TX_OUT (pin 5) = 4- $\Omega$ output impedance<br>P = 200 mW (+23 dBm) at 5 V, P = 70 mW (+18 dBm) at 3.3 V                                                                                |
| B3      | pm_on    | 1 = Selects aux RX input                              | RX_IN2 input is used                                                                                                                                                                      |
|         |          | 0 = Selects main RX input                             | RX_IN1 input is used                                                                                                                                                                      |
| B2      | Reserved |                                                       |                                                                                                                                                                                           |
| B1      | rec_on   | 1 = Receiver activated for external field measurement | Forces enabling of receiver and TX oscillator. Used for external field measurement.                                                                                                       |
|         |          | 0 = Automatic enable                                  | Allows enable of the receiver by bit 5 of this register                                                                                                                                   |
| B0      | vrs5_3   | 1 = 5-V operation                                     | Selects the VIN voltage range                                                                                                                                                             |
|         |          | 0 = 3-V operation                                     |                                                                                                                                                                                           |

#### 6.14.1.1.2 ISO Control Register (0x01)

表 6-17 描述了 ISO 控制寄存器的位域。该寄存器控制 ISO 标准协议、直接模式、和接收 CRC。

**Default Value:** 0x02 (ISO/IEC 15693 high bit rate, one subcarrier, 1 out of 4), reset at EN = L or POR = H

**表 6-17. ISO Control Register (0x01)**

| BIT NO. | BIT NAME | FUNCTION                   | DESCRIPTION                                                                                    |
|---------|----------|----------------------------|------------------------------------------------------------------------------------------------|
| B7      | rx_crc_n | CRC receive selection      | 1 = No RX CRC (CRC not present in the response)<br>0 = RX CRC (CRC is present in the response) |
| B6      | dir_mode | Direct mode type selection | 0 = Direct mode 0<br>1 = Direct mode 1                                                         |
| B5      | rfid     | RFID mode                  | 0 = RFID mode<br>1 = Reserved (should be set to 0)                                             |
| B4      | iso_4    | RFID                       | See 表 6-18 for B0:B4 settings based on the ISO protocol that the application requires.         |
| B3      | iso_3    | RFID                       |                                                                                                |
| B2      | iso_2    | RFID                       |                                                                                                |
| B1      | iso_1    | RFID                       |                                                                                                |
| B0      | iso_0    | RFID                       |                                                                                                |

**表 6-18. ISO Control Register: ISO\_4 to ISO\_0**

| iso_4 | iso_3 | iso_2 | iso_1 | iso_0 | PROTOCOL                                                                 | REMARKS            |
|-------|-------|-------|-------|-------|--------------------------------------------------------------------------|--------------------|
| 0     | 0     | 0     | 0     | 0     | ISO/IEC 15693 low bit rate, 6.62 kbps, one subcarrier, 1 out of 4        |                    |
| 0     | 0     | 0     | 0     | 1     | ISO/IEC 15693 low bit rate, 6.62 kbps, one subcarrier, 1 out of 256      |                    |
| 0     | 0     | 0     | 1     | 0     | ISO/IEC 15693 high bit rate, 26.48 kbps, one subcarrier, 1 out of 4      | Default for reader |
| 0     | 0     | 0     | 1     | 1     | ISO/IEC 15693 high bit rate, 26.48 kbps, one subcarrier, 1 out of 256    |                    |
| 0     | 0     | 1     | 0     | 0     | ISO/IEC 15693 low bit rate, 6.67 kbps, double subcarrier, 1 out of 4     |                    |
| 0     | 0     | 1     | 0     | 1     | ISO/IEC 15693 low bit rate, 6.67 kbps, double subcarrier, 1 out of 256   |                    |
| 0     | 0     | 1     | 1     | 0     | ISO/IEC 15693 high bit rate, 26.69 kbps, double subcarrier, 1 out of 4   |                    |
| 0     | 0     | 1     | 1     | 1     | ISO/IEC 15693 high bit rate, 26.69 kbps, double subcarrier, 1 out of 256 |                    |

## 6.14.1.2 Protocol Subsetting Registers

### 6.14.1.2.1 TX Pulse Length Control Register (0x06)

表 6-19 describes the bit fields of the TX Pulse Length Control register. This register controls the length of TX pulse.

**Default Value:** 0x00, set at POR = H or EN = L and at each write to ISO Control register

The length of the modulation pulse is defined by the protocol selected in the ISO Control register (0x01). With a high-Q antenna, the modulation pulse is typically prolonged, and the tag detects a longer pulse than intended. For such cases, the modulation pulse length can be corrected by using the TX pulse length register 0x06. If the register contains all zeros, then the pulse length is governed by the protocol selection. If the register contains a value other than 0x00, the pulse length is equal to the value of the register in 73.7-ns increments. This means the range of adjustment can be 73.7 ns to 18.8  $\mu$ s.

**表 6-19. TX Pulse Length Control Register (0x06)**

| BIT NO. | BIT NAME | FUNCTION                     | DESCRIPTION                                                                                                                                                                                                                                                                                             |
|---------|----------|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B7      | Pul_p2   | Pulse length. B7 is the MSB. | <p>The pulse range is 73.7 ns to 18.8 <math>\mu</math>s (1 to 255), step size 73.7 ns</p> <p>All bits low (00) = Pulse length control is disabled</p> <p>The following default timings are preset by the ISO Control register (0x01):<br/>9.44 <math>\mu</math>s for ISO/IEC 15693 (TI Tag-It HF-I)</p> |
| B6      | Pul_p1   |                              |                                                                                                                                                                                                                                                                                                         |
| B5      | Pul_p0   |                              |                                                                                                                                                                                                                                                                                                         |
| B4      | Pul_c4   |                              |                                                                                                                                                                                                                                                                                                         |
| B3      | Pul_c3   |                              |                                                                                                                                                                                                                                                                                                         |
| B2      | Pul_c2   |                              |                                                                                                                                                                                                                                                                                                         |
| B1      | Pul_c1   |                              |                                                                                                                                                                                                                                                                                                         |
| B0      | Pul_c0   |                              |                                                                                                                                                                                                                                                                                                         |

### 6.14.1.2.2 RX No Response Wait Time Register (0x07)

表 6-20 describes the bit fields of the RX No Response Wait Time register. This register defines the time when no response interrupt is sent.

**Default Value:** 0x0E, set at POR = H or EN = L and at each write to ISO Control register

The RX no response timer is controlled by the RX No Response Wait Time register. This timer measures the time from the start of slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in IRQ Status Control register (0x0C). This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register in increments of 37.76  $\mu$ s. This register is also preset, automatically, for every new protocol selection.

**表 6-20. RX No Response Wait Time Register (0x07)**

| BIT NO. | BIT NAME | FUNCTION                    | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---------|----------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B7      | NoResp7  | No response. B7 is the MSB. | <p>Defines the time when the <i>no response</i> interrupt is sent. Timing starts from the end of TX EOF. RX no response wait range is 37.76 <math>\mu</math>s to 9628 <math>\mu</math>s (1 to 255). Step size is 37.76 <math>\mu</math>s.</p> <p>The following default timings are preset by the ISO Control register (0x01):<br/>755 <math>\mu</math>s for ISO/IEC 15693 high data rate (TI Tag-It HF-I)<br/>1812 <math>\mu</math>s for ISO/IEC 15693 low data rate (TI Tag-It HF-I)</p> |
| B6      | NoResp6  |                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| B5      | NoResp5  |                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| B4      | NoResp4  |                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| B3      | NoResp3  |                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| B2      | NoResp2  |                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| B1      | NoResp1  |                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| B0      | NoResp0  |                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

### 6.14.1.2.3 RX Wait Time Register (0x08)

表 6-21 描述了 RX Wait Time 寄存器的位域。该寄存器定义了 TX EOF 之后 RX 输入被忽略的时间；例如，用于屏蔽由响应卡产生的电磁干扰。

**Default Value:** 0x1F, set at POR = H or EN = L and at each write to the ISO Control register

The RX wait time timer is controlled by the value in the RX Wait Time register. This timer defines the time after the end of the transmit operation in which the receive decoders are not active (held in reset state). This prevents incorrect detections resulting from transients following the transmit operation. The value of the RX wait time register defines this time in increments of 9.44  $\mu$ s. This register is preset at every write to ISO Control register according to the minimum tag response time defined by each standard.

**表 6-21. RX Wait Time Register (0x08)**

| BIT NO. | BIT NAME | FUNCTION                     | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                    |
|---------|----------|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B7      | Rxw7     | RX wait time. B7 is the MSB. | <p>Defines the time after the TX EOF during which the RX input is ignored. Time starts from the end of TX EOF.</p> <p>RX wait range is 9.44 <math>\mu</math>s to 2407 <math>\mu</math>s (1 to 255). Step size is: 9.44 <math>\mu</math>s.</p> <p>The following default timings are preset by the ISO Control register (0x01):<br/>293 <math>\mu</math>s for ISO/IEC 15693 (TI Tag-It HF-I)</p> |
| B6      | Rxw6     |                              |                                                                                                                                                                                                                                                                                                                                                                                                |
| B5      | Rxw5     |                              |                                                                                                                                                                                                                                                                                                                                                                                                |
| B4      | Rxw4     |                              |                                                                                                                                                                                                                                                                                                                                                                                                |
| B3      | Rxw3     |                              |                                                                                                                                                                                                                                                                                                                                                                                                |
| B2      | Rxw2     |                              |                                                                                                                                                                                                                                                                                                                                                                                                |
| B1      | Rxw1     |                              |                                                                                                                                                                                                                                                                                                                                                                                                |
| B1      | Rxw0     |                              |                                                                                                                                                                                                                                                                                                                                                                                                |

#### 6.14.1.2.4 Modulator and SYS\_CLK Control Register (0x09)

表 6-22 describes the bit fields of the Modulator and SYS\_CLK Control register. This register controls the modulation input and depth, ASK/OOK pin control, and clock output to an external system (an MCU).

**Default Value:** 0x11, set at POR = H or EN = L at each write to the ISO Control register for all bits except Clo1 and Clo0

The frequency of SYS\_CLK (pin 27) is programmable by bits B4 and B5 of this register. The frequency of the TRF7962A system clock oscillator is divided by 1, 2, or 4 resulting in available SYS\_CLK frequencies of 13.56 MHz, 6.78 MHz, or 3.39 MHz, respectively.

The ASK modulation depth is controlled by bits B0, B1, and B2. The range of ASK modulation is 7% to 30% or 100% (OOK). The selection between ASK and OOK (100%) modulation can also be done using direct input OOK (pin 12). The direct control of OOK or ASK using the OOK pin is only possible if the function is enabled by setting B6 = 1 (en\_ook\_p) in this register (0x09) and the ISO Control register (0x01, B6 = 1). When configured this way, the MOD pin (pin 14) is used as input for the modulation signal.

**表 6-22. Modulator and SYS\_CLK Control Register (0x09)**

| BIT NO. | BIT NAME | FUNCTION                                                                                                                          | DESCRIPTION                                                                                                                                                                                                                                       |      |                |                                |
|---------|----------|-----------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|----------------|--------------------------------|
| B7      | Unused   |                                                                                                                                   |                                                                                                                                                                                                                                                   |      |                |                                |
| B6      | en_ook_p | 1 = Enables external selection of ASK or OOK modulation<br><br>0 = Default operation as defined in bits B0 to B2 of this register | Enable ASK/OOK pin (pin 12) for change between any preselected ASK modulation as defined by B0 to B2 and OOK modulation.<br><br>If B6 is set to 1, pin 12 is configured as:<br>1 = OOK modulation<br>0 = Modulation as defined in B0 to B2 (0x09) |      |                |                                |
| B5      | Clo1     | SYS_CLK output frequency. B5 is the MSB.                                                                                          | Clo1                                                                                                                                                                                                                                              | Clo0 | SYS_CLK Output |                                |
|         |          |                                                                                                                                   | 0                                                                                                                                                                                                                                                 | 0    | Disabled       |                                |
|         |          |                                                                                                                                   | 0                                                                                                                                                                                                                                                 | 1    | 3.39 MHz       |                                |
| B4      | Clo0     |                                                                                                                                   | 1                                                                                                                                                                                                                                                 | 0    | 6.78 MHz       |                                |
|         |          |                                                                                                                                   | 1                                                                                                                                                                                                                                                 | 1    | 13.56 MHz      |                                |
| B3      | en_ana   | 1 = Sets pin 12 (ASK/OOK) as an analog output<br><br>0 = Default                                                                  | For test and measurement purpose. ASK/OOK pin 12 can be used to monitor the analog subcarrier signal before the digitizing with DC level equal to AGND.                                                                                           |      |                |                                |
| B2      | Pm2      | Modulation depth. B2 is the MSB.                                                                                                  | Pm2                                                                                                                                                                                                                                               | Pm1  | Pm0            | Modulation Type and Percentage |
|         |          |                                                                                                                                   | 0                                                                                                                                                                                                                                                 | 0    | 0              | ASK 10%                        |
|         |          |                                                                                                                                   | 0                                                                                                                                                                                                                                                 | 0    | 1              | OOK (100%)                     |
|         |          |                                                                                                                                   | 0                                                                                                                                                                                                                                                 | 1    | 0              | ASK 7%                         |
| B1      | Pm1      |                                                                                                                                   | 0                                                                                                                                                                                                                                                 | 1    | 1              | ASK 8.5%                       |
|         |          |                                                                                                                                   | 1                                                                                                                                                                                                                                                 | 0    | 0              | ASK 13%                        |
|         |          |                                                                                                                                   | 1                                                                                                                                                                                                                                                 | 0    | 1              | ASK 16%                        |
| B0      | Pm0      |                                                                                                                                   | 1                                                                                                                                                                                                                                                 | 1    | 0              | ASK 22%                        |
|         |          |                                                                                                                                   | 1                                                                                                                                                                                                                                                 | 1    | 1              | ASK 30%                        |

#### 6.14.1.2.5 RX Special Setting Register (0x0A)

表 6-23 描述了 RX Special Setting 寄存器的位域。该寄存器直接设置增益和滤波器。

**Default Value:** 0x40, set at POR = H or EN = L and at each write to the ISO Control register (0x01)

**表 6-23. RX Special Setting Register (0x0A)**

| BIT NO. | BIT NAME | FUNCTION                                                                                                                   | DESCRIPTION                                              |
|---------|----------|----------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|
| B7      | C212     | Band-pass 110 kHz to 570 kHz                                                                                               |                                                          |
| B6      | C424     | Band-pass 200 kHz to 900 kHz                                                                                               | Appropriate for 424-kHz subcarrier used in ISO/IEC 15693 |
| B5      | M848     | Band-pass 450 kHz to 1.5 MHz                                                                                               |                                                          |
| B4      | hbt      | Band-pass 100 kHz to 1.5 MHz<br>Gain reduced for 18 dB                                                                     |                                                          |
| B3      | gd1      | 00 = Gain reduction 0 dB<br>01 = Gain reduction for 5 dB<br>10 = Gain reduction for 10 dB<br>11 = Gain reduction for 15 dB | Sets the RX gain reduction and reduces sensitivity       |
| B2      | gd2      |                                                                                                                            |                                                          |
| B1      | Reserved |                                                                                                                            |                                                          |
| B0      | Reserved |                                                                                                                            |                                                          |

#### 注

The setting of bits B4, B5, B6, and B7 to zero selects band-pass characteristic of 240 kHz to 1.4 MHz.

#### 6.14.1.2.6 Regulator and I/O Control Register (0x0B)

表 6-24 describes the bit fields of the Regulator and I/O Control register. This register controls the three voltage regulators.

**Default Value:** 0x87, set at POR = H or EN = L

**表 6-24. Regulator and I/O Control Register (0x0B)**

| BIT NO. | BIT NAME  | FUNCTION                                        | DESCRIPTION                                                                                                                                                                                                |
|---------|-----------|-------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B7      | auto_reg  | 0 = Manual system<br>1 = Automatic system       | Automatic system settings:<br>VDD_RF = VIN – 250 mV<br>VDD_A = VIN – 250 mV<br>VDD_X = VIN – 250 mV, but not higher than 3.4 V<br><br>Manual system settings:<br>See B2 to B0                              |
| B6      | en_ext_pa | Support for external power amplifier            | Internal peak detectors are disabled, receiver inputs (RX_IN1 and RX_IN2) accept externally demodulated subcarrier. At the same time, the ASK/OOK pin becomes modulation output for external TX amplifier. |
| B5      | io_low    | 1 = Enable low peripheral communication voltage | When B5 = 1, maintains the output driving capabilities of the I/O pins connected to the level shifter under low-voltage operation. Should be set 1 when VDD_I/O voltage is 1.8 V to 2.7 V.                 |
| B4      | Unused    | No function                                     | Default is 0.                                                                                                                                                                                              |
| B3      | Unused    | No function                                     | Default is 0.                                                                                                                                                                                              |
| B2      | vrs2      | Voltage set. B2 is the MSB.                     | vrs3_5 = L:<br>VDD_RF, VDD_A, VDD_X range is 2.7 V to 3.4 V.<br><br>See 表 6-25, 表 6-26, 表 6-27, and 表 6-28.                                                                                                |
| B1      | vrs1      |                                                 |                                                                                                                                                                                                            |
| B0      | vrs0      |                                                 |                                                                                                                                                                                                            |
|         |           |                                                 |                                                                                                                                                                                                            |

**表 6-25. Supply Regulator Setting, Manual 5-V System**

| REGISTER | OPTION BITS SETTING IN CONTROL REGISTER |    |    |    |    |    |    |    | ACTION                                       |
|----------|-----------------------------------------|----|----|----|----|----|----|----|----------------------------------------------|
|          | B7                                      | B6 | B5 | B4 | B3 | B2 | B1 | B0 |                                              |
| 00       |                                         |    |    |    |    |    |    | 1  | 5-V system                                   |
| 0B       | 0                                       |    |    |    |    |    |    |    | Manual regulator setting                     |
| 0B       | 0                                       |    |    |    |    | 1  | 1  | 1  | VDD_RF = 5 V, VDD_A = 3.5 V, VDD_X = 3.4 V   |
| 0B       | 0                                       |    |    |    |    | 1  | 1  | 0  | VDD_RF = 4.9 V, VDD_A = 3.5 V, VDD_X = 3.4 V |
| 0B       | 0                                       |    |    |    |    | 1  | 0  | 1  | VDD_RF = 4.8 V, VDD_A = 3.5 V, VDD_X = 3.4 V |
| 0B       | 0                                       |    |    |    |    | 1  | 0  | 0  | VDD_RF = 4.7 V, VDD_A = 3.5 V, VDD_X = 3.4 V |
| 0B       | 0                                       |    |    |    |    | 0  | 1  | 1  | VDD_RF = 4.6 V, VDD_A = 3.5 V, VDD_X = 3.4 V |
| 0B       | 0                                       |    |    |    |    | 0  | 1  | 0  | VDD_RF = 4.5 V, VDD_A = 3.5 V, VDD_X = 3.4 V |
| 0B       | 0                                       |    |    |    |    | 0  | 0  | 1  | VDD_RF = 4.4 V, VDD_A = 3.5 V, VDD_X = 3.4 V |
| 0B       | 0                                       |    |    |    |    | 0  | 0  | 0  | VDD_RF = 4.3 V, VDD_A = 3.5 V, VDD_X = 3.4 V |

**表 6-26. Supply Regulator Setting, Manual 3-V System**

| REGISTER | OPTION BITS SETTING IN CONTROL REGISTER |    |    |    |    |    |    |    | ACTION                                       |
|----------|-----------------------------------------|----|----|----|----|----|----|----|----------------------------------------------|
|          | B7                                      | B6 | B5 | B4 | B3 | B2 | B1 | B0 |                                              |
| 00       |                                         |    |    |    |    |    |    | 0  | 3-V system                                   |
| 0B       | 0                                       |    |    |    |    |    |    |    | Manual regulator setting                     |
| 0B       | 0                                       |    |    |    |    | 1  | 1  | 1  | VDD_RF = 3.4 V, VDD_A = 3.4 V, VDD_X = 3.4 V |
| 0B       | 0                                       |    |    |    |    | 1  | 1  | 0  | VDD_RF = 3.3 V, VDD_A = 3.3 V, VDD_X = 3.3 V |
| 0B       | 0                                       |    |    |    |    | 1  | 0  | 1  | VDD_RF = 3.2 V, VDD_A = 3.2 V, VDD_X = 3.2 V |
| 0B       | 0                                       |    |    |    |    | 1  | 0  | 0  | VDD_RF = 3.1 V, VDD_A = 3.1 V, VDD_X = 3.1 V |
| 0B       | 0                                       |    |    |    |    | 0  | 1  | 1  | VDD_RF = 3.0 V, VDD_A = 3.0 V, VDD_X = 3.0 V |
| 0B       | 0                                       |    |    |    |    | 0  | 1  | 0  | VDD_RF = 2.9 V, VDD_A = 2.9 V, VDD_X = 2.9 V |
| 0B       | 0                                       |    |    |    |    | 0  | 0  | 1  | VDD_RF = 2.8 V, VDD_A = 2.8 V, VDD_X = 2.8 V |
| 0B       | 0                                       |    |    |    |    | 0  | 0  | 0  | VDD_RF = 2.7 V, VDD_A = 2.7 V, VDD_X = 2.7 V |

**表 6-27. Supply Regulator Setting, Automatic 5-V System**

| REGISTER | OPTION BITS SETTING IN CONTROL REGISTER |    |    |    |    |                   |    |    | ACTION                                             |
|----------|-----------------------------------------|----|----|----|----|-------------------|----|----|----------------------------------------------------|
|          | B7                                      | B6 | B5 | B4 | B3 | B2 <sup>(1)</sup> | B1 | B0 |                                                    |
| 00       |                                         |    |    |    |    |                   |    | 1  | 5-V system                                         |
| 0B       | 1                                       |    |    |    |    | x                 | 1  | 1  | Automatic regulator setting with 250-mV difference |
| 0B       | 1                                       |    |    |    |    | x                 | 1  | 0  | Automatic regulator setting with 350-mV difference |
| 0B       | 1                                       |    |    |    |    | x                 | 0  | 0  | Automatic regulator setting with 400-mV difference |

(1) x = don't care

**表 6-28. Supply Regulator Setting, Automatic 3-V System**

| REGISTER | OPTION BITS SETTING IN CONTROL REGISTER |    |    |    |    |                   |    |    | ACTION                                             |
|----------|-----------------------------------------|----|----|----|----|-------------------|----|----|----------------------------------------------------|
|          | B7                                      | B6 | B5 | B4 | B3 | B2 <sup>(1)</sup> | B1 | B0 |                                                    |
| 00       |                                         |    |    |    |    |                   |    | 0  | 3-V system                                         |
| 0B       | 1                                       |    |    |    |    | x                 | 1  | 1  | Automatic regulator setting with 250-mV difference |
| 0B       | 1                                       |    |    |    |    | x                 | 1  | 0  | Automatic regulator setting with 350-mV difference |
| 0B       | 1                                       |    |    |    |    | x                 | 0  | 0  | Automatic regulator setting with 400-mV difference |

(1) x = don't care

### 6.14.1.3 Status Registers

#### 6.14.1.3.1 IRQ Status Register (0x0C)

表 6-29 describes the bit fields of the IRQ Status register. This register provides information available about TRF7962A IRQ, TX, and RX status.

**Default Value:** 0x00, set at POR = H or EN = L and at each write to the ISO Control register (0x01). The register is also automatically reset at the end of a read phase. The reset also removes the IRQ flag.

To reset (clear) the register and the IRQ line, the register must be read. During transmit, the decoder is disabled, and only bits B5 and B7 can be changed. During receive, only bit B6 can be changed, but does not trigger the IRQ line immediately. The IRQ signal is set at the end of the transmit or receive phase.

**表 6-29. IRQ Status Register (0x0C)**

| BIT NO. | BIT NAME   | FUNCTION                   | DESCRIPTION                                                                                                                                                 |
|---------|------------|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B7      | Irq_tx     | IRQ set due to end of TX   | Signals that TX is in progress. The flag is set at the start of TX but the interrupt request (IRQ = 1) is sent when TX is finished.                         |
| B6      | Irq_srx    | IRQ set due to RX start    | Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX but the interrupt request (IRQ = 1) is sent when RX is finished. |
| B5      | Irq_fifo   | FIFO is high or low        | Signals when the FIFO is high or low (more than 8 bits during RX or less than 4 bits during TX). See <a href="#">Section 6.12.2</a> for details.            |
| B4      | Irq_err1   | CRC error                  | Indicates receive CRC error only if B7 (no RX CRC) of ISO Control register is set to 0.                                                                     |
| B3      | Irq_err2   | Parity error               | Indicates parity error                                                                                                                                      |
| B2      | Irq_err3   | Byte framing or EOF error  | Indicates framing error                                                                                                                                     |
| B1      | Irq_col    | Collision error            | Collision error for ISO/IEC 15693 single subcarrier.<br>Collision error bit can also be triggered by external noise.                                        |
| B0      | Irq_noresp | No-response time interrupt | No response within the "No-response time" defined in RX No-response Wait Time register (0x07). Signals the MCU that next slot command can be sent.          |

### 6.14.1.3.2 Collision Position and Interrupt Mask Registers (0x0D and 0x0E)

表 6-30 describes the bit fields of the Collision Position and Interrupt Mask register.

**Default Value:** 0x3E, set at POR = H and EN = L. Collision bits reset automatically after read operation.

**表 6-30. Collision Position and Interrupt Mask Register (0x0D)**

| BIT NO. | BIT NAME      | FUNCTION                                  | DESCRIPTION |
|---------|---------------|-------------------------------------------|-------------|
| B7      | Col9          | Bit position of collision MSB             |             |
| B6      | Col8          | Bit position of collision                 |             |
| B5      | En_irq_fifo   | Interrupt enable for FIFO                 | Default = 1 |
| B4      | En_irq_err1   | Interrupt enable for CRC                  | Default = 1 |
| B3      | En_irq_err2   | Interrupt enable for Parity               | Default = 1 |
| B2      | En_irq_err3   | Interrupt enable for Framing error or EOF | Default = 1 |
| B1      | En_irq_col    | Interrupt enable for collision error      | Default = 1 |
| B0      | En_irq_noresp | Enables no response interrupt             | Default = 0 |

表 6-31 describes the bit fields of the Collision Position register. This register displays the bit position of collision or error.

**Default Value:** 0x00, set at POR = H and EN = L. The register is also automatically reset after a read.

**表 6-31. Collision Position Register (0x0E)**

| BIT NO. | BIT NAME | FUNCTION                                  | DESCRIPTION                                                                                 |
|---------|----------|-------------------------------------------|---------------------------------------------------------------------------------------------|
| B7      | Col7     | Bit position of collision. B7 is the MSB. | This register shows the bit position of error. Either frame, SOF/EOF, parity, or CRC error. |
| B6      | Col6     |                                           |                                                                                             |
| B5      | Col5     |                                           |                                                                                             |
| B4      | Col4     |                                           |                                                                                             |
| B3      | Col3     |                                           |                                                                                             |
| B2      | Col2     |                                           |                                                                                             |
| B1      | Col1     |                                           |                                                                                             |
| B0      | Col0     |                                           |                                                                                             |

### 6.14.1.3.3 RSSI Levels and Oscillator Status Register (0x0F)

表 6-32 描述了 RSSI Levels and Oscillator Status 寄存器的位域。该寄存器报告接收通道和 RF 幅度在 RF 关闭期间的信号强度。RSSI 值在接收开始到下一次传输开始期间有效。

RSSI 测量块正在测量解调后的包络信号（除非在直接命令用于 RF 幅度测量的部分中描述）。测量系统正在锁存峰值，因此可以在接收数据包结束后读取 RSSI 值。RSSI 值在下次传输动作期间重置，因此可以测量新标签的响应水平。Section 6.7.1.1 和 Section 6.7.1.2 描述了计算到 RF\_IN1 和 RF\_IN2 的 RSSI 值。RSSI 有 7 步（3 位）以 4-dB 递增。输入水平是 RF 信号在单侧包络（正或负）上的峰值调制水平。

**表 6-32. RSSI Levels and Oscillator Status Register (0x0F)**

| BIT NO. | BIT NAME | FUNCTION                                | DESCRIPTION                                                                                                                                                                                                                        |
|---------|----------|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B7      | Unused   |                                         |                                                                                                                                                                                                                                    |
| B6      | osc_ok   | Crystal oscillator stable indicator     | 13.56-MHz frequency stable (approximately 200 $\mu$ s)                                                                                                                                                                             |
| B5      | rssi_x2  | MSB RSSI value of auxiliary RX (RX_IN2) | Auxiliary channel is by default RX_IN2. The input can be swapped by B3 = 1 (Chip State Control register). If "swapped", the auxiliary channel is connected to RX_IN1 and the auxiliary RSSI represents the signal level at RX_IN1. |
| B4      | rssi_x1  | Auxiliary channel RSSI                  |                                                                                                                                                                                                                                    |
| B3      | rssi_x0  | MSB RSSI value of auxiliary RX (RX_IN2) | Active channel is the default and can be set with option bit B3 = 0 of the Chip Status Control register (0x00).                                                                                                                    |
| B2      | rssi_2   | MSB RSSI value of Main RX (RX_IN1)      |                                                                                                                                                                                                                                    |
| B1      | rssi_1   | Main channel RSSI                       |                                                                                                                                                                                                                                    |
| B0      | rssi_0   | LSB RSSI value of Main RX (RX_IN1)      |                                                                                                                                                                                                                                    |

#### 6.14.1.4 Test Registers

##### 6.14.1.4.1 Test Register (0x1A)

表 6-33 describes the bit fields of the Test register at 0x1A.

**Default Value:** 0x00, set at POR = H and EN = L

**表 6-33. Test Register (0x1A) (for Test or Direct Use)**

| BIT NO. | BIT NAME     | FUNCTION                                         | DESCRIPTION                                                                                                             |
|---------|--------------|--------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|
| B7      | OOK_Subc_In  | Subcarrier input                                 | OOK pin becomes decoder digital input                                                                                   |
| B6      | MOD_Subc_Out | Subcarrier output                                | MOD pin becomes receiver subcarrier output                                                                              |
| B5      | MOD_Direct   | Direct TX modulation and RX reset                | MOD pin becomes receiver subcarrier output                                                                              |
| B4      | o_sel        | First stage output selection                     | 0 = First stage output used for analog out and digitizing<br>1 = Second stage output used for analog out and digitizing |
| B3      | low2         | Second stage gain –6 dB, HP corner frequency / 2 |                                                                                                                         |
| B2      | low1         | First stage gain –6 dB, HP corner frequency / 2  |                                                                                                                         |
| B1      | zun          | Input followers test                             |                                                                                                                         |
| B0      | Test_AGC     | AGC test, AGC level is seen on rssi_210 bits     |                                                                                                                         |

##### 6.14.1.4.2 Test Register (0x1B)

表 6-34 describes the bit fields of the Test register at 0x1B. When a test\_dec or test\_io is set, the IC is switched to test mode. Test mode persists until a stop condition arrives. At stop condition, the test\_dec and test\_io bits are cleared.

**Default Value:** 0x00, set at POR = H and EN = L

**表 6-34. Test Register 2 (0x1B) (for Test or Direct Use)**

| BIT NO. | BIT NAME      | FUNCTION              | DESCRIPTION               |
|---------|---------------|-----------------------|---------------------------|
| B7      | test_rf_level | RF level test         |                           |
| B6      |               |                       |                           |
| B5      |               |                       |                           |
| B4      |               |                       |                           |
| B3      | test_io1      | I/O test              | Not implemented           |
| B2      | test_io0      |                       |                           |
| B1      | test_dec      | Decoder test mode     |                           |
| B0      | clock_su      | Coder clock 13.56 MHz | For faster test of coders |

### 6.14.1.5 FIFO Control Registers

#### 6.14.1.5.1 FIFO Status Register (0x1C)

表 6-35 描述了 FIFO 状态寄存器的位域。该寄存器包含要传输的完整字节的低半字节的信息以及关于损坏字节和要从中传输的位的数量。

**表 6-35. FIFO Status Register (0x1C)**

| BIT NO. | BIT NAME | FUNCTION            | DESCRIPTION                                                                                                                                                                                     |
|---------|----------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B7      | RFU      | B7 = 0              | Reserved for future use (RFU)                                                                                                                                                                   |
| B6      | Fhil     | FIFO level high     | Indicates that 9 bytes are already in the FIFO (for RX) (also see register 0x0C bit 5)                                                                                                          |
| B5      | Flo1     | FIFO level low      | Indicates that only 3 bytes are in the FIFO (for TX) (also see register 0x0C bit 5)                                                                                                             |
| B4      | Fove     | FIFO overflow error | Too many bytes were written to the FIFO                                                                                                                                                         |
| B3      | Fb3      | FIFO bytes fb[3]    | Bits B0:B3 indicate how many bytes that are loaded in FIFO were not read out yet (displays N – 1 number of bytes). If 8 bytes are in the FIFO, this number is 7 (also see register 0x0C bit 6). |
| B2      | Fb2      | FIFO bytes fb[2]    |                                                                                                                                                                                                 |
| B1      | Fb1      | FIFO bytes fb[1]    |                                                                                                                                                                                                 |
| B0      | Fb0      | FIFO bytes fb[0]    |                                                                                                                                                                                                 |

#### 6.14.1.5.2 TX Length Byte1 Register (0x1D) and TX Length Byte2 Register (0x1E)

表 6-36 描述了 TX 长度字节 1 寄存器的位域。该寄存器包含要传输的完整字节的两个高半字节。

**Default Value:** 0x00, set at POR and EN = 0. The register is also automatically reset at TX EOF.

**表 6-36. TX Length Byte1 Register (0x1D)**

| BIT NO. | BIT NAME | FUNCTION                       | DESCRIPTION                                                |
|---------|----------|--------------------------------|------------------------------------------------------------|
| B7      | Txl11    | Number of complete byte bn[11] | High nibble of complete intended bytes to be transmitted   |
| B6      | Txl10    | Number of complete byte bn[10] |                                                            |
| B5      | Txl9     | Number of complete byte bn[9]  |                                                            |
| B4      | Txl8     | Number of complete byte bn[8]  |                                                            |
| B3      | Txl7     | Number of complete byte bn[7]  | Middle nibble of complete intended bytes to be transmitted |
| B2      | Txl6     | Number of complete byte bn[6]  |                                                            |
| B1      | Txl5     | Number of complete byte bn[5]  |                                                            |
| B0      | Txl4     | Number of complete byte bn[4]  |                                                            |

表 6-37 describes the bit fields of the TX Length Byte2 register. This register contains the low nibble of the complete bytes to be transferred through FIFO, and information about a broken byte and number of bits to be transferred from it.

**Default Value:** 0x00, set at POR and EN = 0. The register is also automatically reset at TX EOF.

**表 6-37. TX Length Byte2 Register (0x1E)**

| BIT NO. | BIT NAME | FUNCTION                         | DESCRIPTION                                                                                                                      |
|---------|----------|----------------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| B7      | Txl3     | Number of complete byte bn[3]    | Low nibble of complete intended bytes to be transmitted                                                                          |
| B6      | Txl2     | Number of complete byte bn[2]    |                                                                                                                                  |
| B5      | Txl1     | Number of complete byte bn[1]    |                                                                                                                                  |
| B4      | Txl0     | Number of complete byte bn[0]    |                                                                                                                                  |
| B3      | Bb2      | Broken byte number of bits bb[2] | Number of bits in the last broken byte to be transmitted.<br>This value is taken into account only when broken byte flag is set. |
| B2      | Bb1      | Broken byte number of bits bb[1] |                                                                                                                                  |
| B1      | Bb0      | Broken byte number of bits bb[0] |                                                                                                                                  |
| B0      | Bbf      | Broken byte flag                 | B0 = 1 indicates that last byte is not complete 8 bits wide.                                                                     |



## 7.2 System Design

### 7.2.1 Layout Considerations

Keep all decoupling capacitors as close to the IC as possible, with the high-frequency decoupling capacitors (10 nF) closer than the low-frequency decoupling capacitors (2.2  $\mu$ F).

Place ground vias as close as possible to the ground side of the capacitors and reader IC pins to minimize any possible ground loops.

It is not recommend using any inductor sizes below 0603 as the output power can be compromised. If smaller sized inductors are absolutely necessary, the designer must confirm output performance.

Pay close attention to the required load capacitance of the used crystal and adjust the two external shunt capacitors accordingly. Follow the recommendations of the crystal manufacturer for those values.

There should be a common ground plane for the digital and analog sections. The multiple ground sections or "islands" should have vias that tie the different sections of the planes together.

Ensure that the exposed thermal pad at the center of the IC is properly laid out. It should be tied to ground to help dissipate heat from the package.

Trace line lengths should be minimized whenever possible, particularly the RF output path, crystal connections, and control lines from the reader to the microprocessor. Proper placement of the TRF7962A, microprocessor, crystal, and RF connection/connector help facilitate this.

Avoid crossing of digital lines under RF signal lines. Also, avoid crossing of digital lines with other digital lines whenever possible. If the crossings are unavoidable, 90° crossings should be used to minimize coupling of the lines.

Depending on the production test plan, the designer should consider possible implementations of test pads or test vias for use during testing. The necessary pads and vias should be placed in accordance with the proposed test plan to help enable easy access to those test points.

If the system implementation is complex (for example, if the RFID reader module is a subsystem of a larger system with other modules such as *Bluetooth*®, *Wi-Fi*®, microprocessors, and clocks), special considerations should be taken to ensure that there is no noise coupling into the supply lines. If needed, special filtering or regulator considerations should be used to minimize or eliminate noise in these systems.

For more information and details on layout considerations, see the [TRF796x HF-RFID Reader Layout Design Guide](#).

### 7.2.2 Impedance Matching TX\_Out (Pin 5) to 50 $\Omega$

The output impedance of the TRF7962A when operated at full power out setting is nominally  $4 + j0 \Omega$  (4  $\Omega$  real). This impedance must be matched to a resonant circuit, and TI recommends a matching circuit from 4  $\Omega$  to 50  $\Omega$ , as commercially available test equipment (for example, spectrum analyzers, power meters, and network analyzers) are 50- $\Omega$  systems. See [图 7-2](#) and [图 7-3](#) for an impedance match reference circuit. This section explains how the values were calculated.

Starting with the 4- $\Omega$  source, [图 7-2](#) and [图 7-3](#) shows the process of going from 4  $\Omega$  to 50  $\Omega$  by showing it represented on a Smith Chart simulator (available from <http://www.fritz.dellsperger.net/>). The elements are grouped together where appropriate.

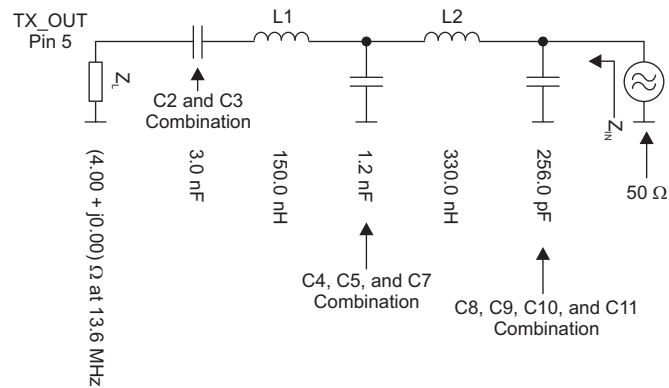


图 7-2. Impedance Matching Circuit

This yields the following Smith Chart simulation.

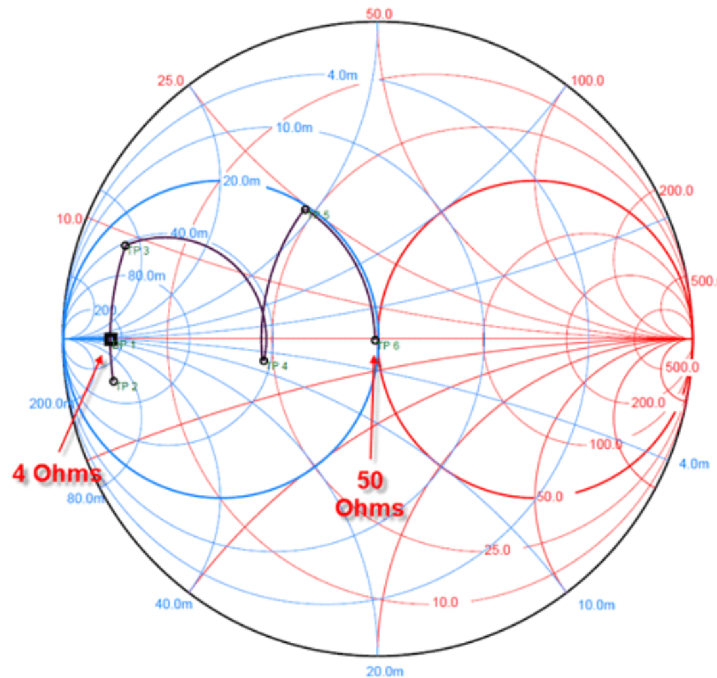


图 7-3. Impedance Matching Smith Chart

Resulting power out can be measured with a power meter, spectrum analyzer with power meter function, or other equipment capable of making a "hot" measurement. Take care to observe maximum power input levels on test equipment and use attenuators whenever available to avoid any possibility of damage to expensive equipment. Table 6-3 lists the expected output power levels under various operating conditions.

### 7.2.3 Reader Antenna Design Guidelines

For HF antenna design considerations using the TRF7962A, see the following documentation:

[Antenna Matching for the TRF7960 RFID Reader](#)

[TRF7960TB HF RFID Reader Module User's Guide](#), with antenna details at end of manual

## 8 器件和文档支持

### 8.1 入门和后续步骤

有关 TI NFC/RFID 器件以及有助于开发的工具和软件的更多信息，请访问 [NFC/RFID 概述](#)。

### 8.2 器件命名规则

为了标示产品开发周期所处的阶段，TI 为器件的部件号分配了前缀。每个商用系列产品成员都具有以下三个前缀之一：x、p 或无前缀。这些前缀代表了从工程原型（带有前缀 x）到完全合格的生产器件（无前缀）的产品开发进化阶段。

器件开发进化流程：

**xTRF...** – 实验器件，不一定代表最终器件的电气规格

**pTRF...** – 最终器件，符合最终产品的电气规格，但是未完成质量和可靠性验证

**TRF...** – 完全合格的生产器件

具有 x 或 p 前缀的器件供货时附带如下免责声明：

“开发的产品用于内部评估用途。”

生产器件已进行完全特性化，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件的故障率大于标准生产器件。由于这些器件的预计最终使用故障率仍未定义，德州仪器 (TI) 建议不要将它们用于任何生产系统。只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。此后缀表示封装类型和可选的温度范围。图 8-1 提供了解读完整器件名称的图例。

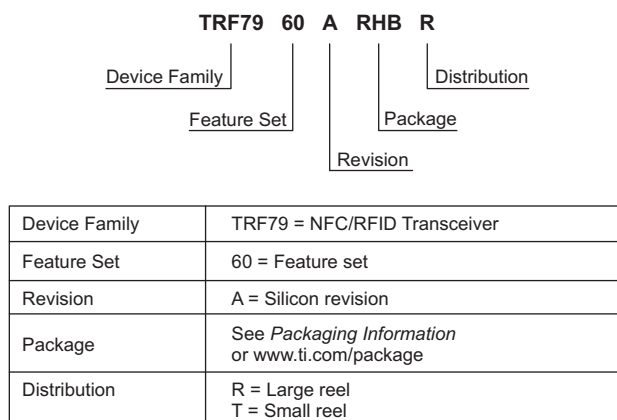


图 8-1. 器件命名规则

### 8.3 工具和软件

#### 设计套件和评估模块

**TRF7960A 评估模块** TRF7960EVM 可以让软件应用程序开发人员试用 TRF796x 多标准全集成 13.56MHz RFID 模拟前端和数据成帧读取器系统的功能。

**TRF7960A 目标板** TRF7960ATB EVM 可以让软件应用程序开发人员在所选的德州仪器 (TI) 嵌入式微控制器平台上试用 TRF796x 多标准全集成 13.56MHz RFID 读/写器 IC 的功能，而无需担心射频部分。

#### 软件

**TRF7960A C 代码示例** 通过寄存器对器件功能进行直接控制的示例源代码。

**TRF7960EVM GUI 源代码** 包含在 **TRF7960A 评估模块** 中的 GUI 源代码。

**TRF7960EVM GUI 软件** 运行在主机 PC 上以便与 TRF7960A 评估模块配合使用的 GUI。

### 8.4 文档支持

以下文档对 TRF7962A 器件进行了介绍。[www.ti.com.cn](http://www.ti.com.cn) 网站上提供了这些文档的副本。

#### 接收文档更新通知

要接收文档更新（包括器件勘误表）通知，请访问 [ti.com](http://ti.com) 上相关器件的产品文件夹（例如 **TRF7962A**）。单击右上角的“提醒我”(Alert me) 按钮。点击后，您将每周定期收到已更改的产品信息（如果有的话）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

#### 应用手册

《**TRF79xxA HF-RFID 读取器布局设计指南**》介绍有关 TRF79xxA 系列 HF RFID 读取器布局的一些建议性指导原则。

《**TRF7960 RFID 读取器的天线匹配**》介绍确定天线匹配电路的设计方法。

《**TRF7960A 固件设计提示**》该参考资料可为固件开发人员提供 TRF7960A 和微控制器（例如 MSP430™ 或 ARM™ 器件）方面的使用知识。

《**TRF7960 和 TRF7960A 启动序列管理**》系统开发人员需要最大限度地减小 TRF7960、TRF7960A 及其变型系统在启动时的电流消耗，该参考资料可向他们提供有关处理稳压器控制寄存器 (0x0B) 值方面的指导。此指导的有效应用用例为电池供电型 RFID 应用，在此类应用中控制整个系统随时间推移的电流消耗至关重要。

《**TRF7960A RFID 多路复用器示例系统**》此应用报告介绍了 TI 为客户应用设计的 16 通道高频 (HF) (13.56MHz) RFID 读取器系统（基于 TRF7960A IC）。位于 MSP430F2370 MCU 上系统固件除了与主机进行通信之外，还支持 ISO/IEC 15693 协议。

《**TRF7960A 参考固件 说明**》此应用报告介绍了 MSP430F2370 中实现的与 TI TRF7960A 评估模块 (EVM) 结合使用的固件。TRF7960AEVM 是多标准全集成 13.56MHz RFID 模拟前端和数据成帧读取器系统。此文档的目标读者是可能有或没有 RFID 固件开发经验并希望了解参考固件和开发自己的 TRF7960A 相关固件的开发者。

《**TRF7960 和 TRF7960A 对比**》此应用报告帮助 TRF7960 高频 RFID/NFC 读取器的当前用户和新用户了解 TRF7960 和 TRF7960A 器件之间的差异。详细了解这些差异并将这些知识运用于应用特定要求，有助于设计人员就是否需要更改物料清单做出明智的决定。

### 8.5 社区资源

单击以下链接访问 TI 社区资源。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《**使用条款**》。

#### TI E2E™ 社区

**TI 工程师间 (E2E) 社区**。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、共享知识、探索思路，在同领域工程师的帮助下解决问题。

### 8.6 商标

E2E is a trademark of Texas Instruments.

Bluetooth is a registered trademark of Bluetooth SIG.

Wi-Fi is a registered trademark of Wi-Fi Alliance.

## 8.7 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 8.8 出口管制提示

接收方同意：如果美国或其他适用法律限制或禁止将通过非披露义务的披露方获得的任何产品或技术数据（其中包括软件）（见美国、欧盟和其他出口管理条例之定义）、或者其他适用国家条例限制的任何受管制产品或此项技术的任何直接产品出口或再出口至任何目的地，那么在没有事先获得美国商务部和其他相关政府机构授权的情况下，接收方不得在知情的情况下，以直接或间接的方式将其出口。

## 8.9 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

## 9 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TRF7962ARHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -20 to 85    | TRF<br>7962A        |
| TRF7962ARHBR.B               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -20 to 85    | TRF<br>7962A        |
| <a href="#">TRF7962ARHBT</a> | Active        | Production           | VQFN (RHB)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -20 to 85    | TRF<br>7962A        |
| TRF7962ARHBT.B               | Active        | Production           | VQFN (RHB)   32 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -20 to 85    | TRF<br>7962A        |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

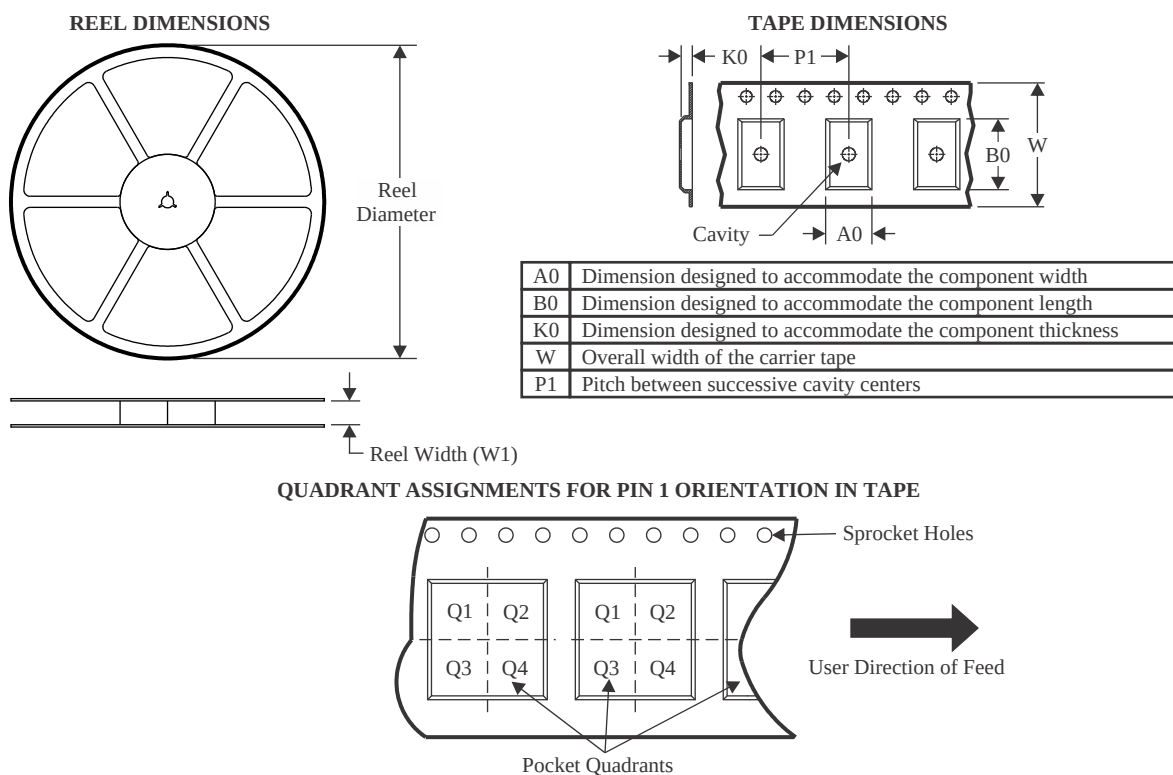
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



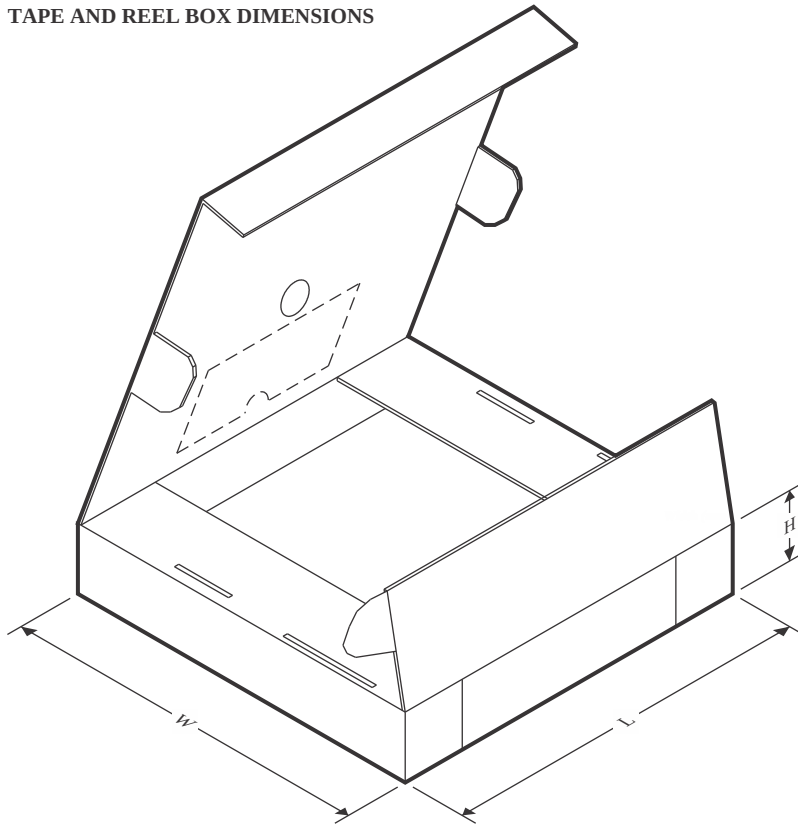
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TRF7962ARHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |
| TRF7962ARHBT | VQFN         | RHB             | 32   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TRF7962ARHBR | VQFN         | RHB             | 32   | 3000 | 353.0       | 353.0      | 32.0        |
| TRF7962ARHBT | VQFN         | RHB             | 32   | 250  | 213.0       | 191.0      | 35.0        |

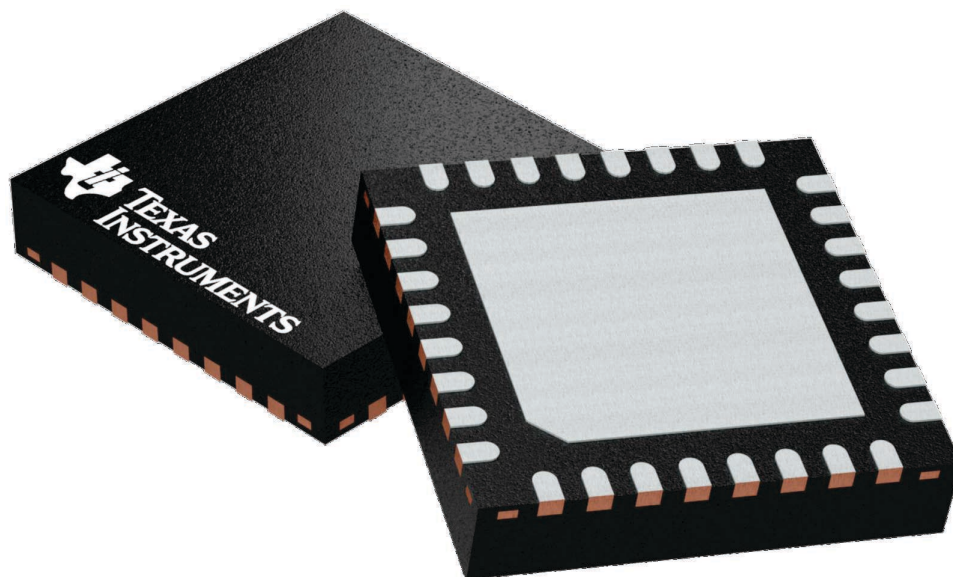
## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224745/A

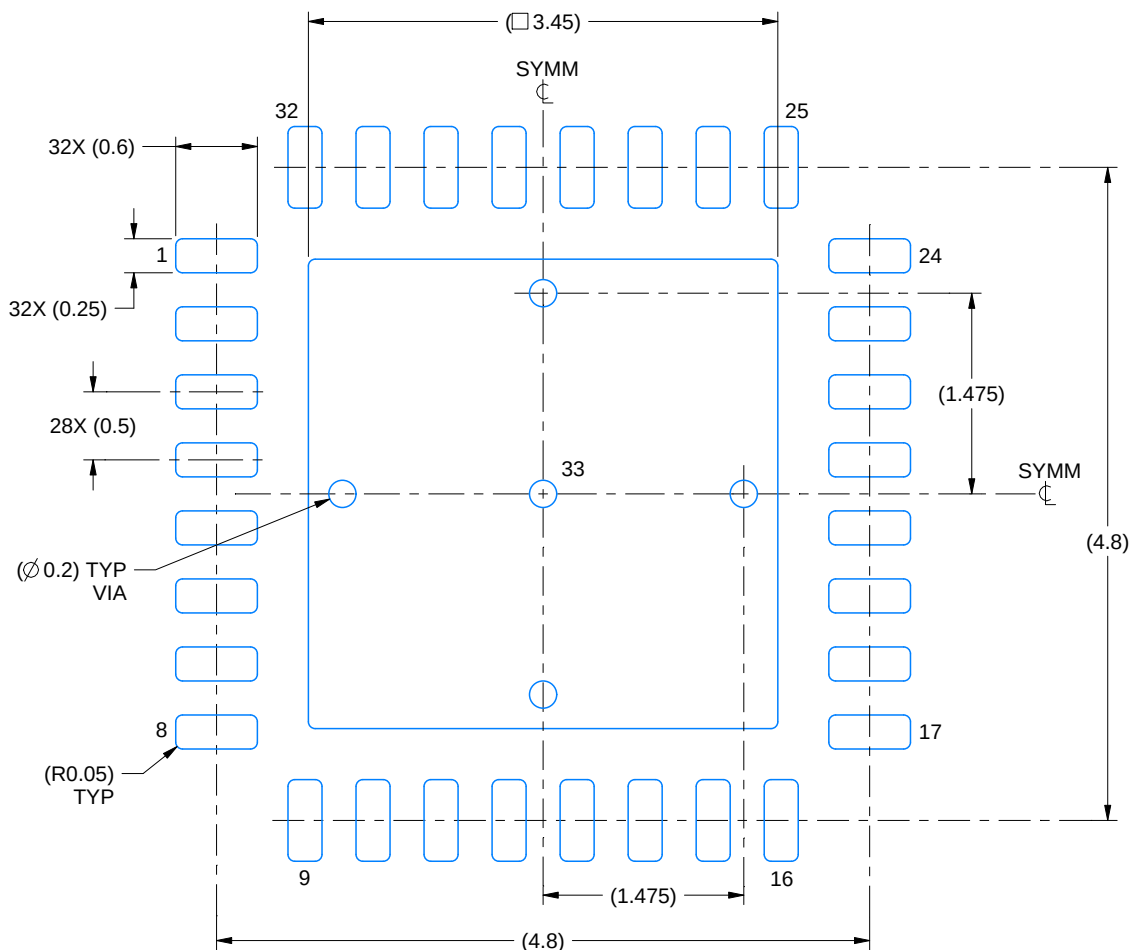
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RHB0032E

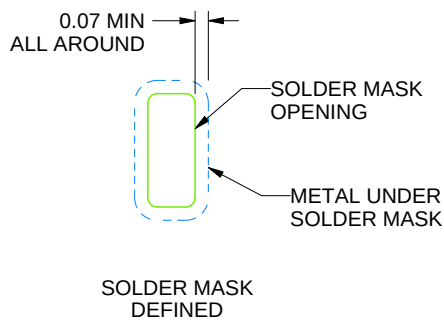
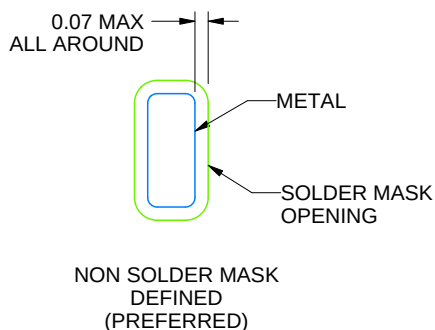
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE

SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

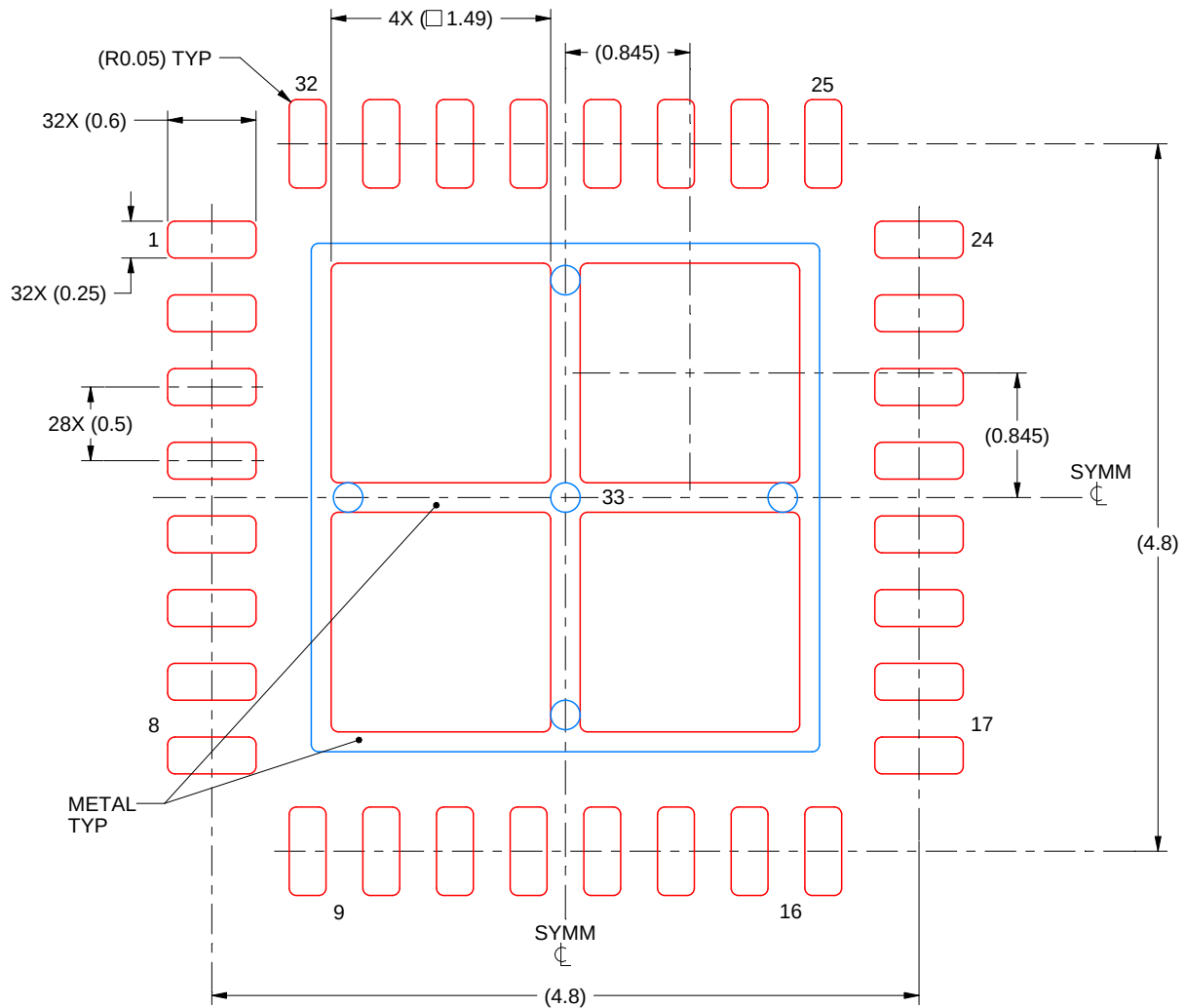
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:  
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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