

TPS791

超低噪声、高 PSRR、快速射频 100mA 低压降线性稳压器

1 特性

- 带 EN 引脚的 100mA 低压降稳压器
- 支持 1.8V、3.3V、4.7V，可调节
- 高 PSRR（频率为 10kHz 时 70dB）
- 超低噪声 (15 μV_{RMS})
- 快速启动时间 (63 μs)
- 借助任何 1 μF 陶瓷电容器实现稳定
- 出色的负载和线路瞬态
- 极低压差电压（全负载时为 38mV，TPS79147）
- 5 引脚 SOT23 (DBV) 封装
- TPS792xx 提供 EN 选项

2 应用

- 为 VCO 和 PLL 供电添加了项目符号
- 蓝牙和无线局域网
- 便携式和电池供电

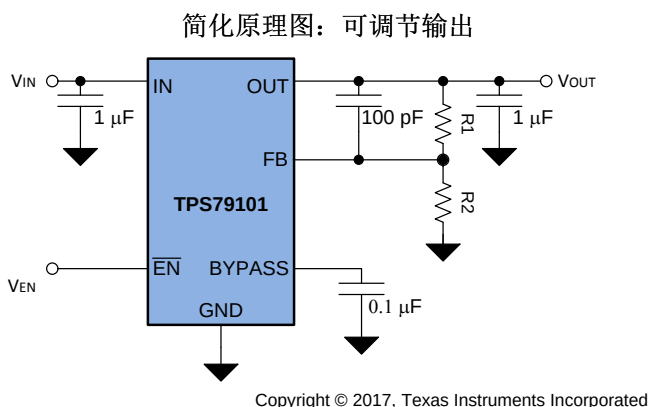
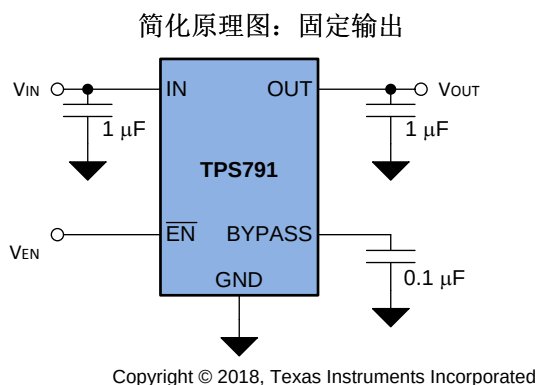
3 说明

TPS791 器件是低压差 (LDO) 低功耗线性稳压器，具有 高电源抑制比 (PSRR)、超低噪声、快速启动和出色的线性和负载瞬态响应，并且采用小型 SOT23 封装。该器件在输出端使用小型 1 μF 陶瓷电容器实现稳定工作。TPS791 使用先进的专有 BiCMOS 制造工艺，能够产生极低压差的电压（例如，100mA 时为 38mV，TPS79147）。该器件可实现快速启动时间（使用一个 0.001 μF 旁路电容器时大约为 63 μs ），同时消耗非常低的静态电流（典型值 170 μA ）。而且，当此器件处于待机模式时，电源电流减少到低于 1 μA 。TPS79118 在使用一个 0.1 μF 旁路电容器时的输出电压噪声大概为 15 μV_{RMS} 。具有对噪声敏感的模拟组件的应用，例如便携式射频电子器件，将受益于高 PSRR 和低噪声特性以及快速响应时间。的最后一段

器件信息⁽¹⁾

器件型号	封装	封装尺寸（标称值）
TPS791	SOT23 (5)	2.90mm x 1.60mm
	SOT23 (6)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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4 修订历史记录

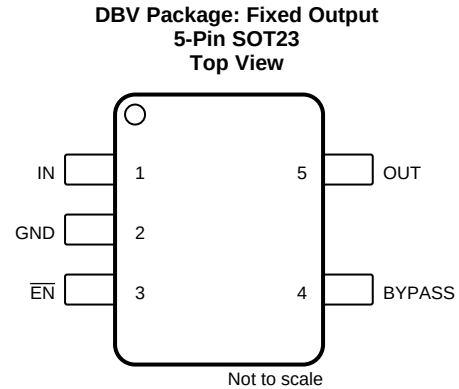
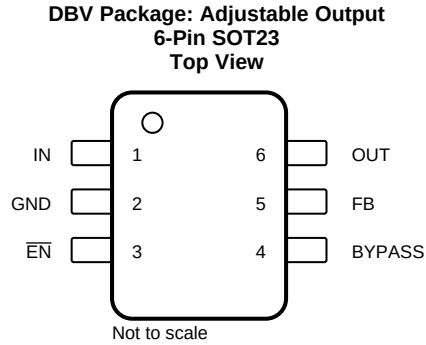
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (May 2002) to Revision D

Page

• 已添加 器件信息 表、简化原理 图添加到第 1 页，ESD 额定值 表、热性能信息 表、引脚配置和功能 部分、概述 部分、特性 说明部分，器件功能模式部分，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分	1
• 已更改 通篇将 TPS791xx 更改成了 TPS791	1
• 已更改 应用 部分	1
• 已更改 说明部分.....	1
• Deleted Ordering Information table	3
• Changed $\overline{\text{EN}}$ pin description	3
• Added I/O data for GND pin	3
• Deleted Package Dissipation Rating table	3
• Changed V_I to V_{IN} , I_O to I_{OUT} , C_O to C_{OUT} , $C_{O(byp)}$ and $C_{(byp)}$ to C_{BYPASS} throughout document	3
• Changed formula in footnote 1 of Recommended Operating Conditions table.....	4
• Added VREF parameter to Electrical Characteristics table.....	5
• Changed V_{CC} to V_{IN} in test conditions of UVLO threshold and UVLO hysteresis parameters.....	5
• Added PSRR and V_{DO} symbols to Power-supply ripple rejection and Dropout voltage parameters.....	5
• Added conditions statement to Typical Characteristics section	6
• Changed I_{OUT} to C_{BYPASS} in TPS79118 Output Spectral Noise Density vs Frequency figure	7
• Changed I_{OUT} to C_{BYPASS} in TPS79133 Output Spectral Noise Density vs Frequency figure	7
• Changed third bullet in Normal Operation section	15
• Changed first bullet in Disabled section	15
• Changed V_{EN} column in Device Functional Mode Comparison table.....	15
• Added active-low to Application Information description	16

5 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	ADJ	FIXED		
BYPASS	4	4	—	An external bypass capacitor connected to this pin, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
$\overline{\text{EN}}$	3	3	I	The $\overline{\text{EN}}$ pin is an input which enables or shuts down the device. The enable signal is an active-low digital control that enables the device, so when $\overline{\text{EN}}$ is a logic high ($> 2\text{ V}$), the device is in shutdown mode. When $\overline{\text{EN}}$ is logic low ($< 0.7\text{ V}$), the device is enabled.
FB	5	N/A	I	This pin is the feedback input voltage for the adjustable device.
GND	2	2	—	Regulator ground.
IN	1	1	I	The IN pin is the input to the device.
OUT	6	5	O	The OUT pin is the regulated output of the device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Input voltage range ⁽²⁾	−0.3	6	V
Voltage range at $\overline{\text{EN}}$	−0.3	$V_{\text{IN}} + 0.3$	V
Voltage on OUT	−0.3	6	V
Peak output current	Internally limited		
Continuous total power dissipation	See Thermal Information table		
Operating virtual junction temperature, T_J	−40	150	°C
Operating ambient temperature, T_A	−40	85	°C
Storage temperature, T_{stg}	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V _{IN} Input voltage ⁽¹⁾	2.7		5.5	V
I _{OUT} Continuous output current ⁽²⁾	0		100	mA
T _J Operating junction temperature	–40		125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following formula:

$V_{IN(min)} = V_{OUT(max)} + \text{dropout voltage } (V_{DO}) \text{ at maximum load.}$

(2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but the device is not recommended to be operated under conditions beyond those specified in this table for extended periods of time.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS791		UNIT
		DBV (SOT23)	DBV (SOT23)	
		5 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	192.6	168.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	104.2	87.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	55.2	36.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	24.1	17.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	54.8	36.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range, ($T_J = -40^\circ\text{C}$ to 125°C), $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage	TPS79101	T _J = 25°C, 1.22 V ≤ V _{OUT} ≤ 5.2 V		V _{OUT}			V
		0 μA < I _{OUT} < 100 mA ⁽¹⁾ , 1.22 V ≤ V _{OUT} ≤ 5.2 V		0.98 V _{OUT}	1.02 V _{OUT}		
	TPS79118	T _J = 25°C		1.8			
		0 μA < I _{OUT} < 100 mA, 2.8 V < V _{IN} < 5.5 V		1.764	1.836		
	TPS79133	T _J = 25°C		3.3			
		0 μA < I _{OUT} < 100 mA, 4.3 V < V _{IN} < 5.5 V		3.234	3.366		
	TPS79147	T _J = 25°C		4.7			
		0 μA < I _{OUT} < 100 mA, 5.2 V < V _{IN} < 5.5 V		4.606	4.794		
VREF	Reference voltage				1.2246		V
Quiescent current (GND current)		0 μA < I _{OUT} < 100 mA, T _J = 25°C		170			μA
		0 μA < I _{OUT} < 100 mA		250			
Load regulation		0 μA < I _{OUT} < 100 mA, T _J = 25°C		5			mV
ΔV _{OUT} /V _{OUT}	Output voltage line regulation ⁽²⁾		V _{OUT} + 1 V < V _{IN} ≤ 5.5 V, T _J = 25°C		0.05		% / V
			V _{OUT} + 1 V < V _{IN} ≤ 5.5 V		0.12		
Output noise voltage (TPS79118)		BW = 100 Hz to 100 kHz, I _{OUT} = 100 mA, T _J = 25°C	C _{BYPASS} = 0.001 μF	32		μV _{RMS}	
			C _{BYPASS} = 0.0047 μF	17			
			C _{BYPASS} = 0.01 μF	16			
			C _{BYPASS} = 0.1 μF	15			
Time, start-up (TPS79133)		R _L = 33 Ω, C _{OUT} = 1 μF, T _J = 25°C	C _{BYPASS} = 0.001 μF	53		μs	
			C _{BYPASS} = 0.0047 μF	67			
			C _{BYPASS} = 0.01 μF	98			
Output current limit		V _{OUT} = 0 V ⁽¹⁾		285	600	mA	
UVLO threshold		V _{IN} rising		2.25	2.65	V	
UVLO hysteresis		T _J = 25°C, V _{IN} rising		100		mV	
Standby current		$\overline{\text{EN}}$ = V _{IN} , 2.7 V < V _{IN} < 5.5 V		0.07	1	μA	
High level enable input voltage		2.7 V < V _{IN} < 5.5 V		2		V	
Low level enable input voltage		2.7 V < V _{IN} < 5.5 V			0.7	V	
Input current ($\overline{\text{EN}}$)		$\overline{\text{EN}}$ = V _{IN}		−1	1	μA	
PSRR	Power-supply ripple rejection	TPS79118	f = 100 Hz, T _J = 25°C, I _{OUT} = 10 mA	80		dB	
			f = 100 Hz, T _J = 25°C, I _{OUT} = 100 mA	75			
			f = 10 kHz, T _J = 25°C, I _{OUT} = 100 mA	72			
			f = 100 kHz, T _J = 25°C, I _{OUT} = 100 mA	45			
	TPS79133	f = 100 Hz, T _J = 25°C, I _{OUT} = 10 mA	70				
		f = 100 Hz, T _J = 25°C, I _{OUT} = 100 mA	75				
		f = 10 kHz, T _J = 25°C, I _{OUT} = 100 mA	73				
		f = 100 kHz, T _J = 25°C, I _{OUT} = 100 mA	37				
V _{DO}	Dropout voltage ⁽³⁾	TPS79133	I _{OUT} = 100 mA, T _J = 25°C	50		mV	
			I _{OUT} = 100 mA	90			
	TPS79147	I _{OUT} = 100 mA, T _J = 25°C	38				
		I _{OUT} = 100 mA	70				

(1) The minimum V_{IN} operating voltage is 2.7 V or $V_{OUT(\text{typ})} + 1\text{ V}$, whichever is greater. The maximum V_{IN} voltage is 5.5 V . The maximum output current is 100 mA .

(2) If $V_{OUT} \leq 1.8\text{ V}$ then $V_{IN\text{min}} = 2.7\text{ V}$ and $V_{IN\text{max}} = 5.5\text{ V}$.

(3) Equals V_{IN} voltage – $V_{OUT(\text{typ})} - 100\text{ mV}$; the TPS79118 dropout voltage is limited by the minimum input voltage range limitations.

6.6 Typical Characteristics

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)

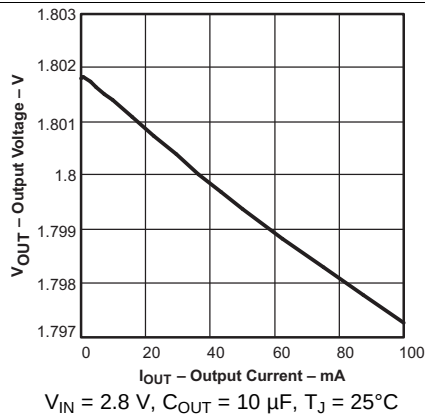


Figure 1. TPS79118 Output Voltage vs Output Current

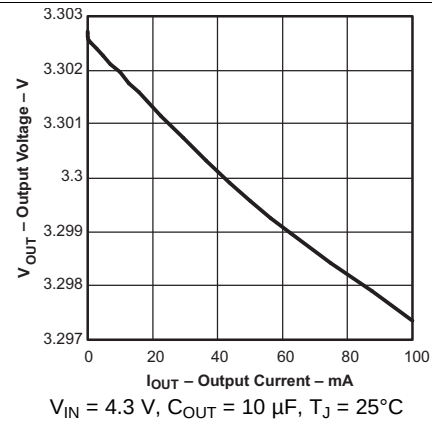


Figure 2. TPS79133 Output Voltage vs Output Current

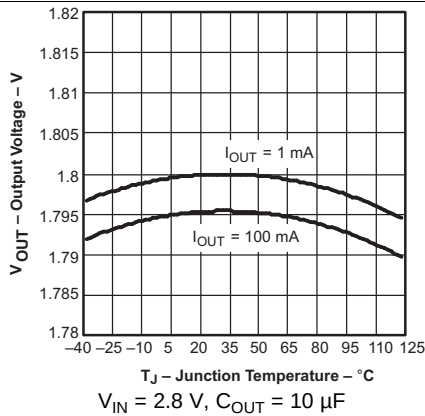


Figure 3. TPS79118 Output Voltage vs Junction Temperature

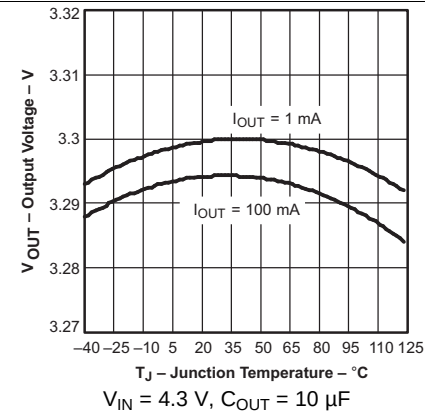


Figure 4. TPS79133 Output Voltage vs Junction Temperature

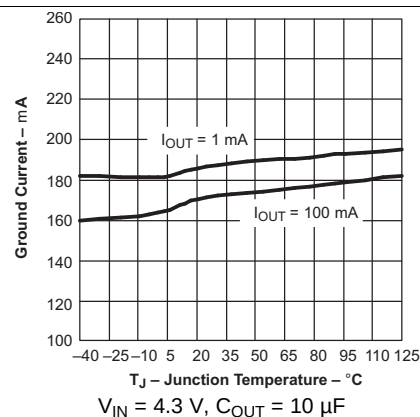


Figure 5. TPS79133 Ground Current vs Junction Temperature

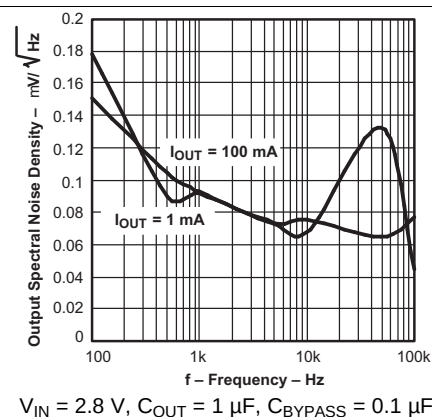
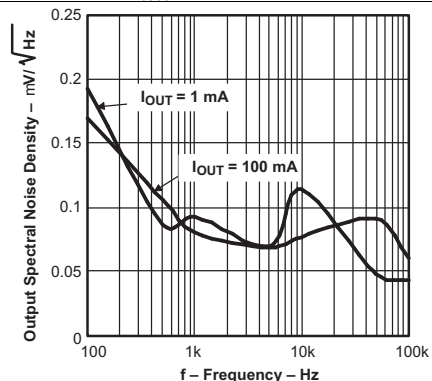


Figure 6. TPS79118 Output Spectral Noise Density vs Frequency

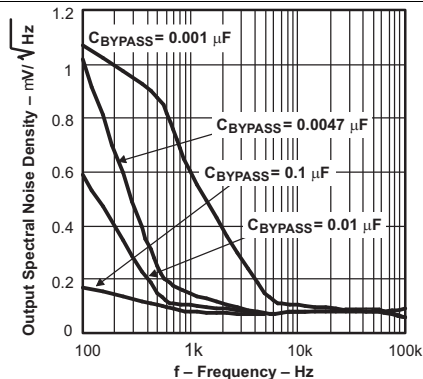
Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)



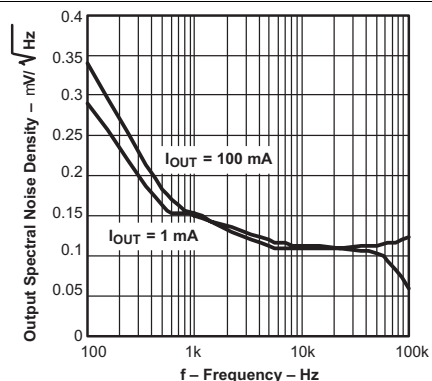
$V_{IN} = 2.8\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$

Figure 7. TPS79118 Output Spectral Noise Density vs Frequency



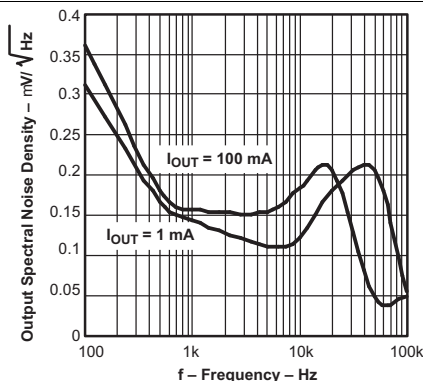
$V_{IN} = 2.8\text{ V}$, $I_{OUT} = 100\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$

Figure 8. TPS79118 Output Spectral Noise Density vs Frequency



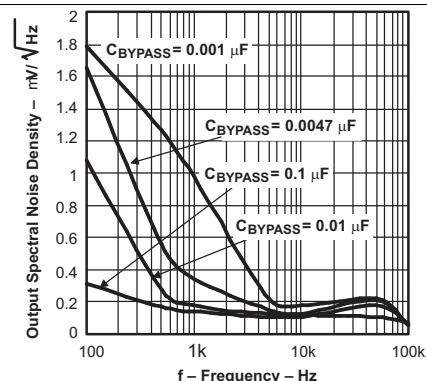
$V_{IN} = 4.3\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$

Figure 9. TPS79133 Output Spectral Noise Density vs Frequency



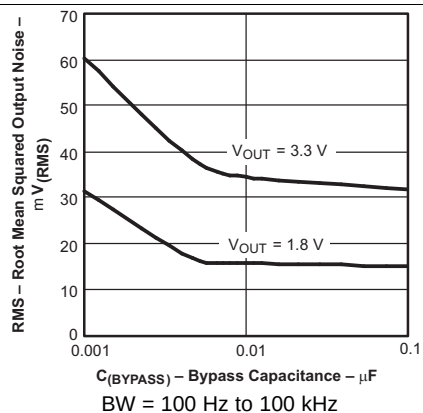
$V_{IN} = 4.3\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$

Figure 10. TPS79133 Output Spectral Noise Density vs Frequency



$V_{IN} = 4.3\text{ V}$, $I_{OUT} = 100\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$

Figure 11. TPS79133 Output Spectral Noise Density vs Frequency



C_{BYPASS} - Bypass Capacitance - μF

BW = 100 Hz to 100 kHz

Figure 12. Root Mean Squared Output Noise vs Bypass Capacitance

Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)

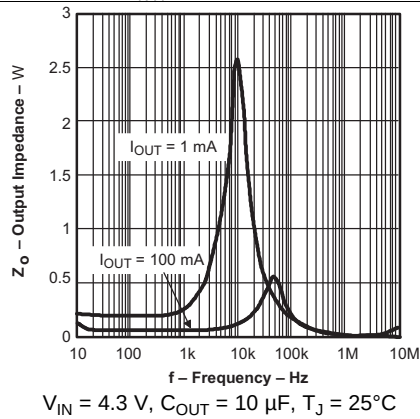


Figure 13. TPS79133 Output Impedance vs Frequency

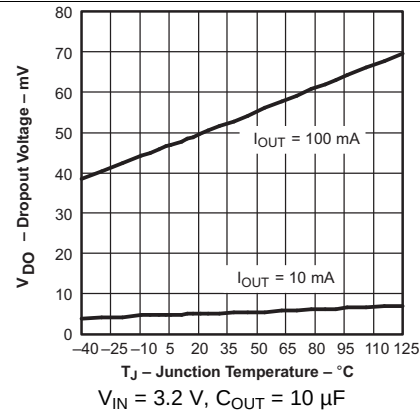


Figure 14. TPS79133 Dropout Voltage vs Junction Temperature

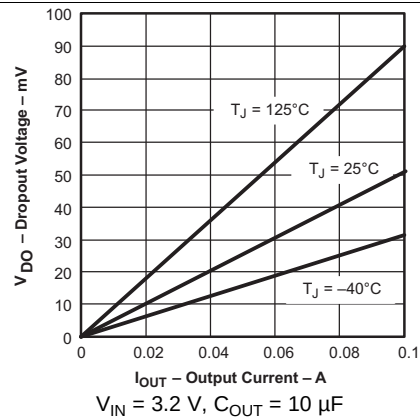


Figure 15. TPS79133 Dropout Voltage vs Output Current

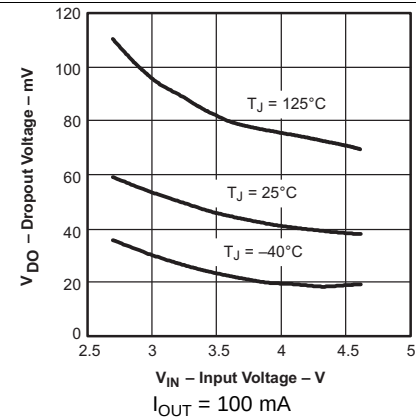


Figure 16. TPS79101 Dropout Voltage vs Input Voltage

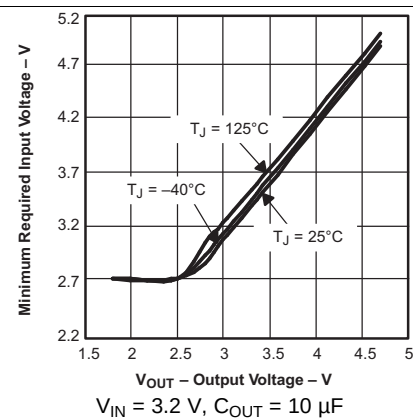


Figure 17. Minimum Required Input Voltage vs Output Voltage

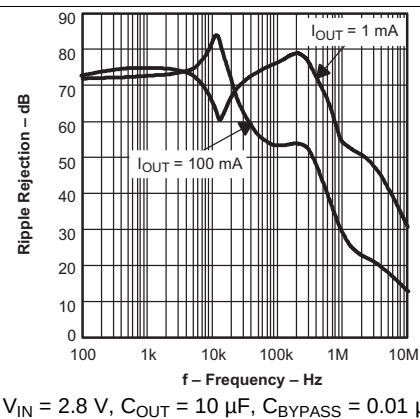
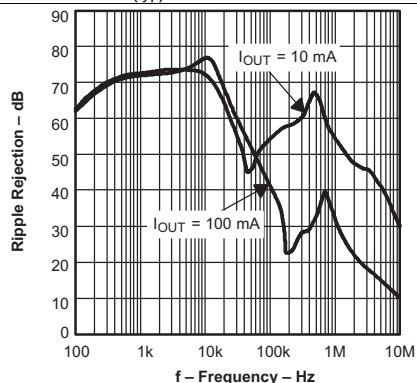


Figure 18. TPS79118 Ripple Rejection vs Frequency

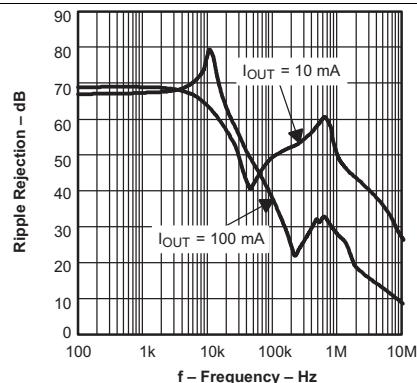
Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)



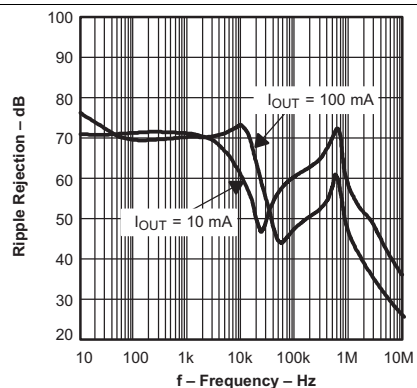
$V_{IN} = 2.8\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $C_{BYPASS} = 0.01\text{ }\mu\text{F}$

Figure 19. TPS79118 Ripple Rejection vs Frequency



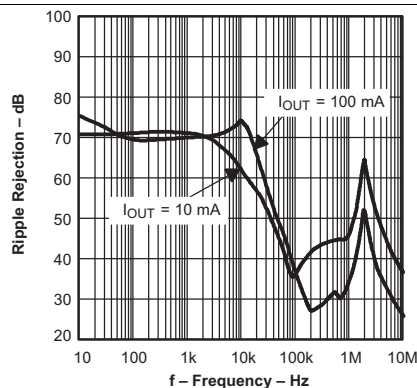
$V_{IN} = 2.8\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$

Figure 20. TPS79118 Ripple Rejection vs Frequency



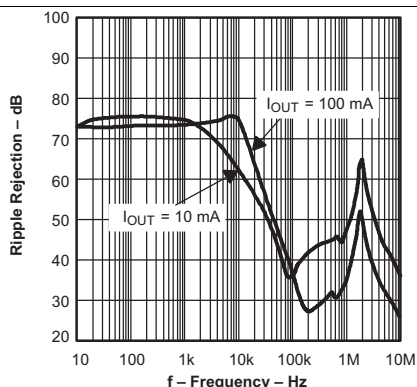
$V_{IN} = 4.3\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{BYPASS} = 0.01\text{ }\mu\text{F}$

Figure 21. TPS79133 Ripple Rejection vs Frequency



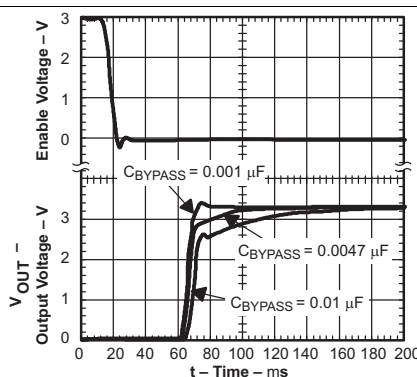
$V_{IN} = 4.3\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $C_{BYPASS} = 0.01\text{ }\mu\text{F}$

Figure 22. TPS79133 Ripple Rejection vs Frequency



$V_{IN} = 4.3\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$

Figure 23. TPS79133 Ripple Rejection vs Frequency



$V_{IN} = 4.3\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 100\text{ mA}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$

Figure 24. TPS79133 Output Voltage, Enable Voltage vs Time (Start-Up)

Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)

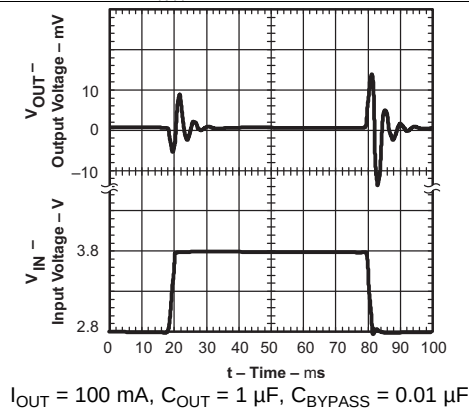


Figure 25. TPS79118 Line Transient Response

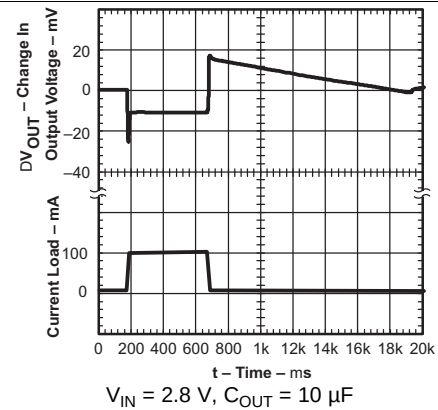


Figure 26. TPS79118 Load Transit Response

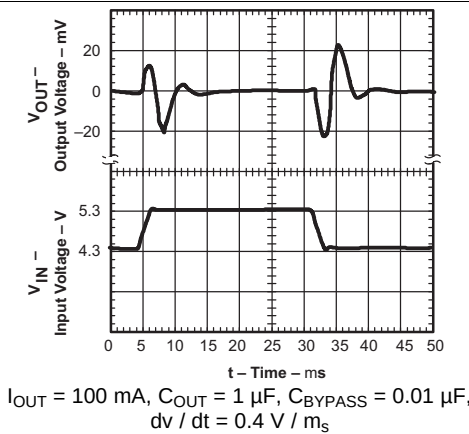


Figure 27. TPS79133 Line Transient Response

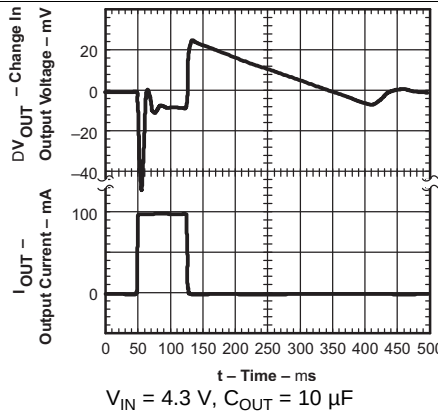


Figure 28. TPS79133 Load Transit Response

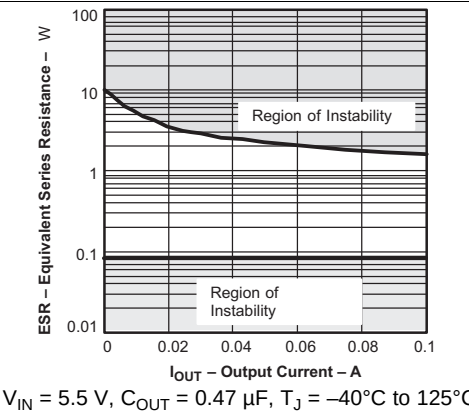


Figure 29. TPS79118 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

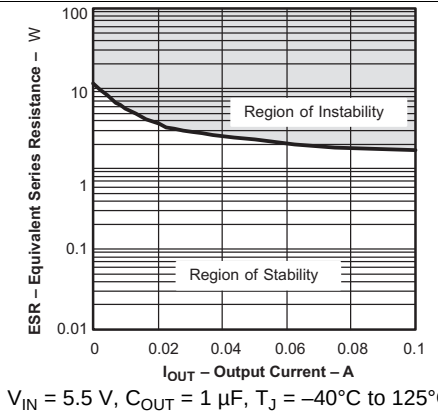


Figure 30. TPS79118 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)

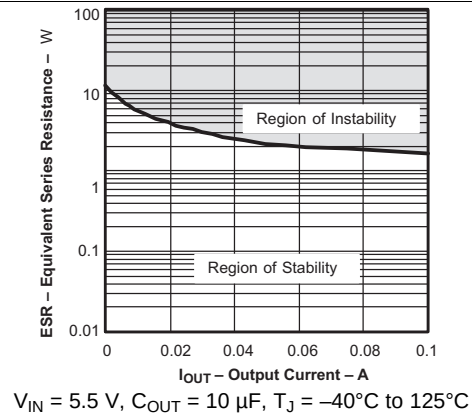


Figure 31. TPS79118 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

7.3 Feature Description

7.3.1 Power Dissipation and Junction Temperature

Specified regulator operation is confirmed at a junction temperature of 125°C; restrict the maximum junction temperature to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where

- T_{Jmax} is the maximum allowable junction temperature
 - $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the [Thermal Information](#) table)
 - T_A is the ambient temperature
- (1)

The regulator dissipation is calculated using:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$
(2)

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

7.3.2 Programming the TPS79101 Adjustable Regulator

The output voltage of the TPS79101 adjustable regulator is programmed using an external resistor divider; see [Figure 32](#). The output voltage is calculated using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2} \right)$$

where

- $V_{REF} = 1.2246 \text{ V typ}$ (the internal reference voltage)
- (3)

Select resistors R1 and R2 for approximately a 50-μA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Avoid higher resistor values because leakage current into or out of FB across R1, R2 creates an offset voltage that artificially increases or decreases the feedback voltage and thus erroneously decreases or increases V_{OUT} . The recommended design procedure is to choose $R2 = 30.1 \text{ k}\Omega$ to set the divider current at 50 μA, $C1 = 15 \text{ pF}$ for stability, and then calculate R1 using:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2$$
(4)

In order to improve the stability of the adjustable version, a small compensation capacitor is suggested to be placed between OUT and FB. For voltages < 1.8 V, the value of this capacitor must be 100 pF. For voltages > 1.8 V, the approximate value of this capacitor can be calculated as:

$$C1 = \frac{(3 \times 10^{-7}) \times (R1 + R2)}{(R1 \times R2)}$$
(5)

Feature Description (continued)

The table in [Figure 34](#) shows the suggested value of this capacitor for several resistor ratios. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage < 1.8 V is chosen, then the minimum recommended output capacitor is 2.2 μF instead of 1 μF .

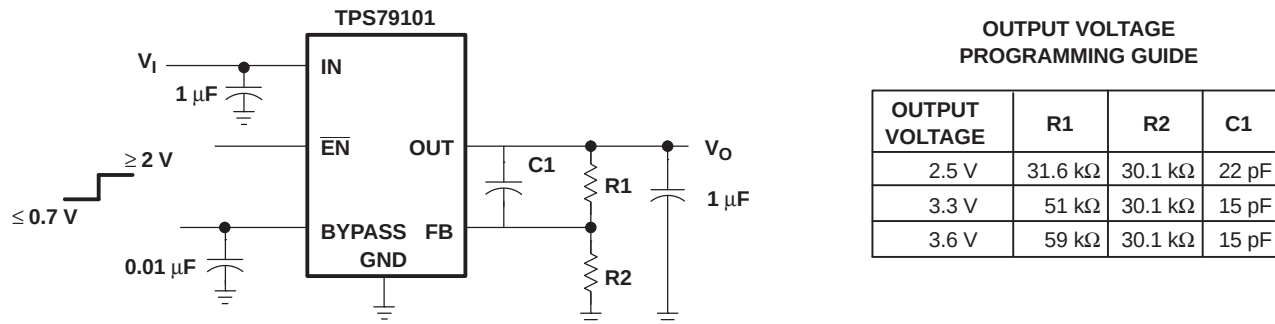


Figure 34. TPS79101 Adjustable LDO Regulator Programming

7.3.3 Regulator Protection

The TPS791 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting may be appropriate.

The TPS791 features internal current limiting and thermal protection. During normal operation, the TPS791 limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Although current limiting is designed to prevent gross device failure, care must be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts the device down. When the device cools down to below approximately 140°C, regulator operation resumes.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as the $|V_{IN(min)}|$
- The input voltage magnitude is greater than the nominal output voltage magnitude added to the dropout voltage
- $|V_{EN}| < \text{low-level enable pin input voltage (0.7 V)}$
- The output current is less than the current limit
- The device junction temperature is less than the maximum specified junction temperature

7.4.2 Dropout Operation

If the input voltage magnitude is lower than the nominal output voltage magnitude plus the specified dropout voltage magnitude, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage magnitude is the same as the input voltage magnitude minus the dropout voltage magnitude. The transient performance of the device is significantly degraded because the pass device (such as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- $|V_{EN}| > \text{high-level enable pin input voltage (2 V)}$
- The device junction temperature is greater than the thermal shutdown temperature

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$ V_{IN} > \{ V_{OUT(nom)} + V_{DO} , V_{IN(min)} \}$	$ V_{EN} < 0.7 \text{ V}$	$I_{OUT} < I_{CL}$	$T_J < 125^\circ\text{C}$
Dropout mode	$ V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO} $	$ V_{EN} < 0.7 \text{ V}$	—	$T_J < 125^\circ\text{C}$
Disabled mode (any true condition disables the device)	—	$ V_{EN} > 2 \text{ V}$	—	$T_J > 170^\circ\text{C}$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS791 low-dropout (LDO) regulator is optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 μA typically), and an active-low, enable input to reduce supply currents to less than 1 μA when the regulator is turned off.

8.1.1 External Capacitor Requirements

A 0.1- μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS791, is required for stability and to improve transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

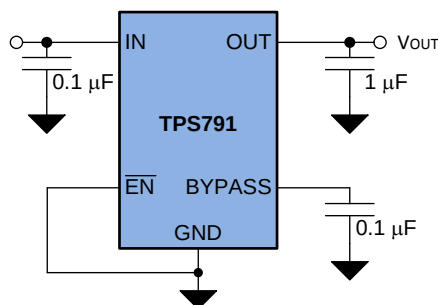
Like all low dropout regulators, the TPS791 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 1 μF . Any 1- μF or larger ceramic capacitor is suitable. The device is also stable with a 0.47- μF ceramic capacitor with at least 75 m Ω of ESR.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS791 has a BYPASS pin that is connected to the voltage reference through a 250-k Ω internal resistor. The 250-k Ω internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79118 exhibits approximately 15 μV_{RMS} of output voltage noise using a 0.1- μF ceramic bypass capacitor and a 1- μF ceramic output capacitor. The output starts up slower as the bypass capacitance increases because of the RC time constant at the bypass pin that is created by the internal 250-k Ω resistor and external capacitor.

8.2 Typical Application

Figure 35 shows a typical application circuit.



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Figure 35. Typical Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

Table 2 shows the parameters used for this design example.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.3 V to 3.5 V (Lithium Ion battery)
Output voltage	3.3 V
DC output current	10 mA
Peak output current	100 mA
Maximum ambient temperature	60°C

8.2.2 Detailed Design Procedure

Select the desired output voltage option. An input capacitor of 0.1 μF is used because the battery is connected to the input through a via and a short 10-mil (0.01-in) trace. An output capacitor of 1 mF is used in this design example. A smaller size output capacitor can be used up to a minimum of 1 μF to stabilize the internal control loop.

8.2.3 Application Curves

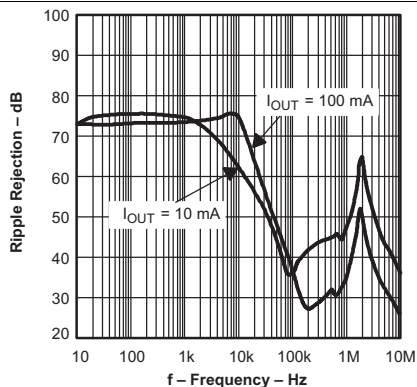


Figure 36. TPS79133 Ripple Rejection vs Frequency

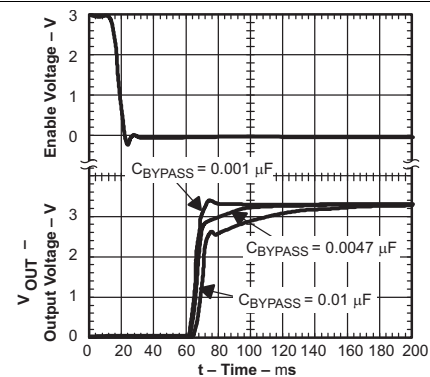


Figure 37. TPS79133 Output Voltage, Enable Voltage vs Time (Start-Up)

8.3 Do's and Don'ts

Do place at least one, low-ESR, 1- μF capacitor as close as possible between the OUT pin of the regulator and the GND pin.

Do place at least one, low-ESR, 0.1- μF capacitor as close as possible between the IN pin of the regulator and the GND pin.

Do provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the Enable (EN) pin.

Do not resistively or inductively load the BYPASS pin.

Do not let the output voltage get more than 0.3 V above the input voltage.

9 Power Supply Recommendations

This device is designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. A 0.1- μ F input capacitor is required for stability; if the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the IN pin to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

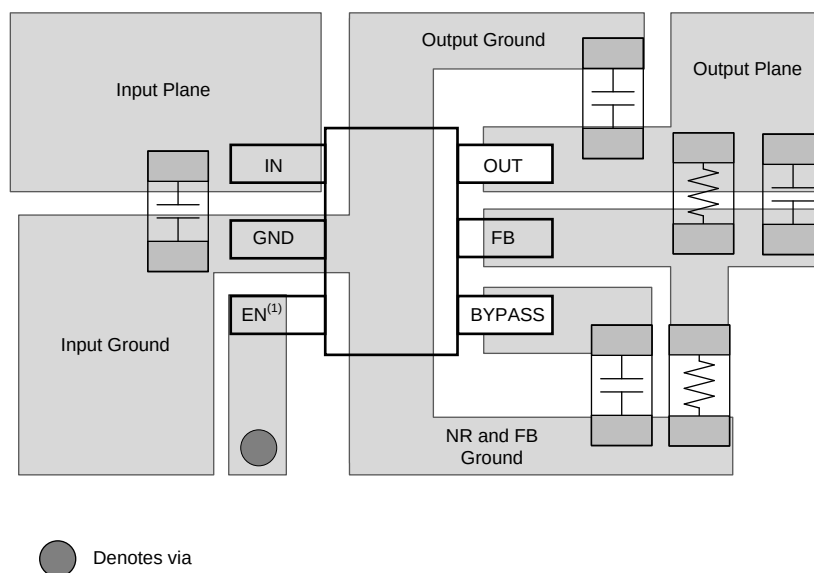
Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN} , C_{OUT} , C_{BYPASS} , and C_1) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits can impact system performance negatively, and even cause instability.

10.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements such as PSRR, output noise, and transient response, TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the ground pin of the device. In addition, connect the ground connection for the bypass capacitor directly to the ground pin of the device.

10.2 Layout Example



(1) The EN pin is active low.

Figure 38. Layout Example (6-Pin DBV Package)

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79101DBVR	NRND	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PEUI
TPS79101DBVR.A	NRND	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PEUI
TPS79101DBVRG4	NRND	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PEUI
TPS79101DBVT	Obsolete	Production	SOT-23 (DBV) 6	-	-	Call TI	Call TI	-40 to 125	PEUI
TPS79118DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PERI
TPS79118DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PERI
TPS79118DBVT	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 125	PERI
TPS79133DBVR	NRND	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PESI
TPS79133DBVR.A	NRND	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PESI
TPS79133DBVRG4	NRND	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PESI
TPS79147DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PETI
TPS79147DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PETI
TPS79147DBVT	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 125	PETI

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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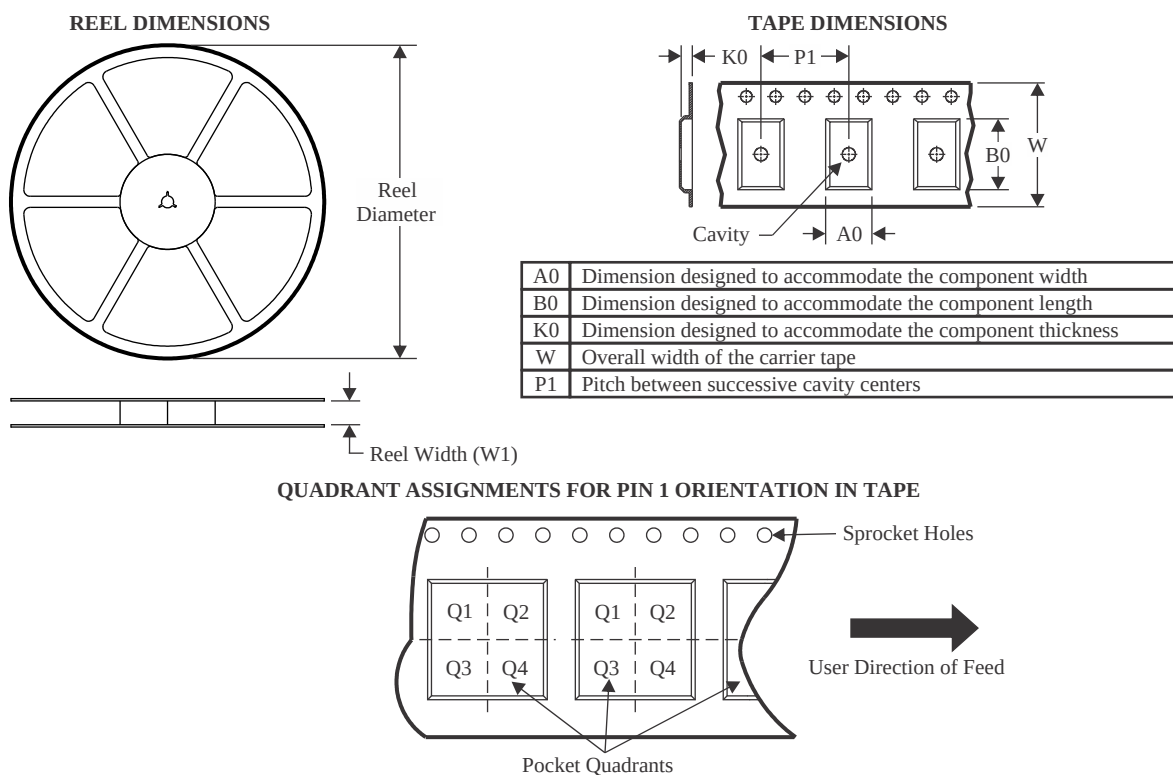
OTHER QUALIFIED VERSIONS OF TPS791 :

- Automotive : [TPS791-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

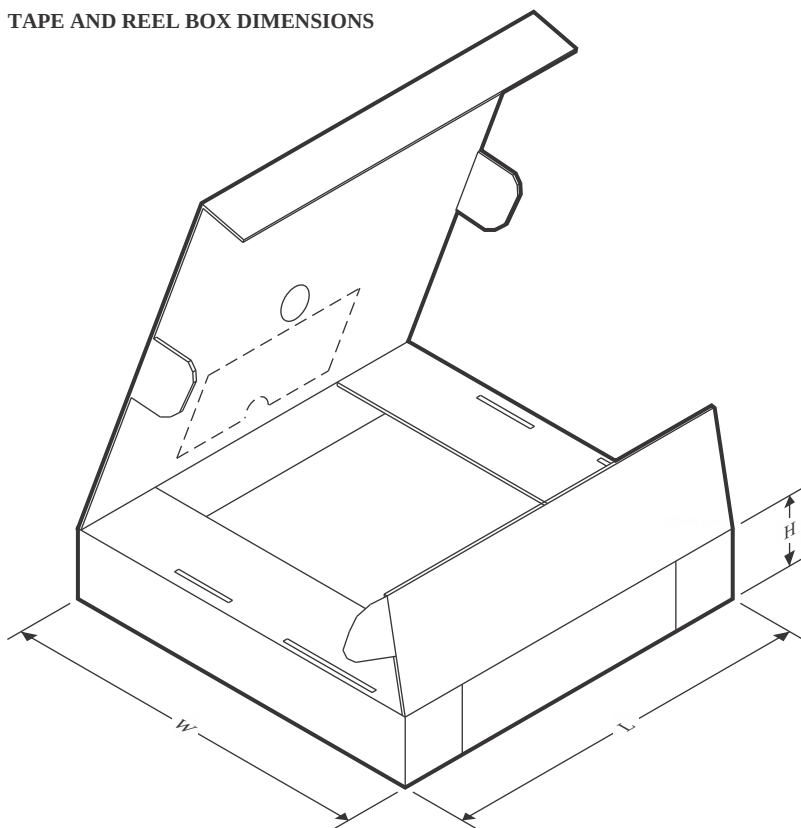
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79101DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79118DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79133DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79133DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79147DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

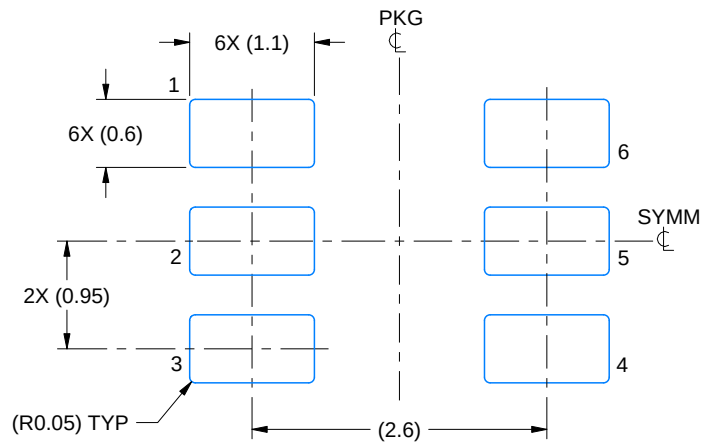
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79101DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS79118DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79133DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79133DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS79147DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

EXAMPLE BOARD LAYOUT

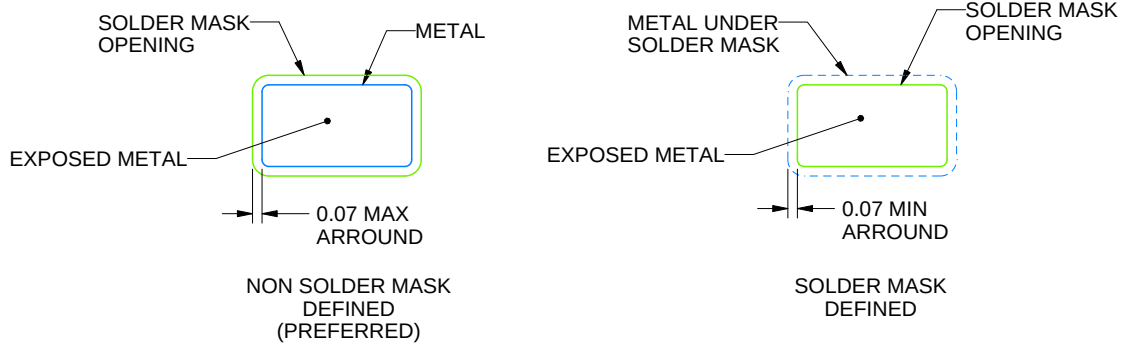
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

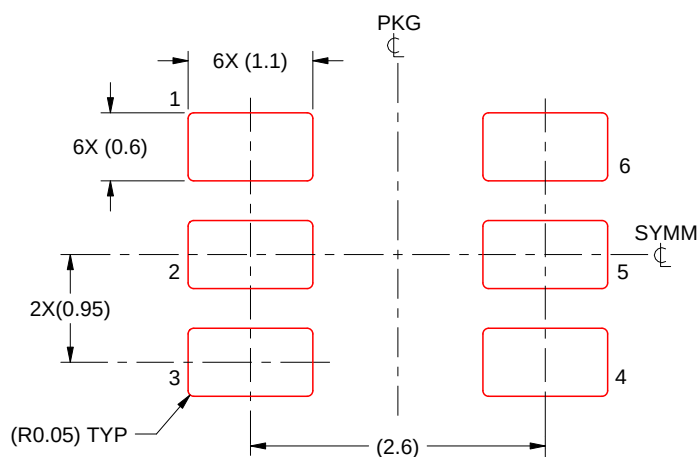
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

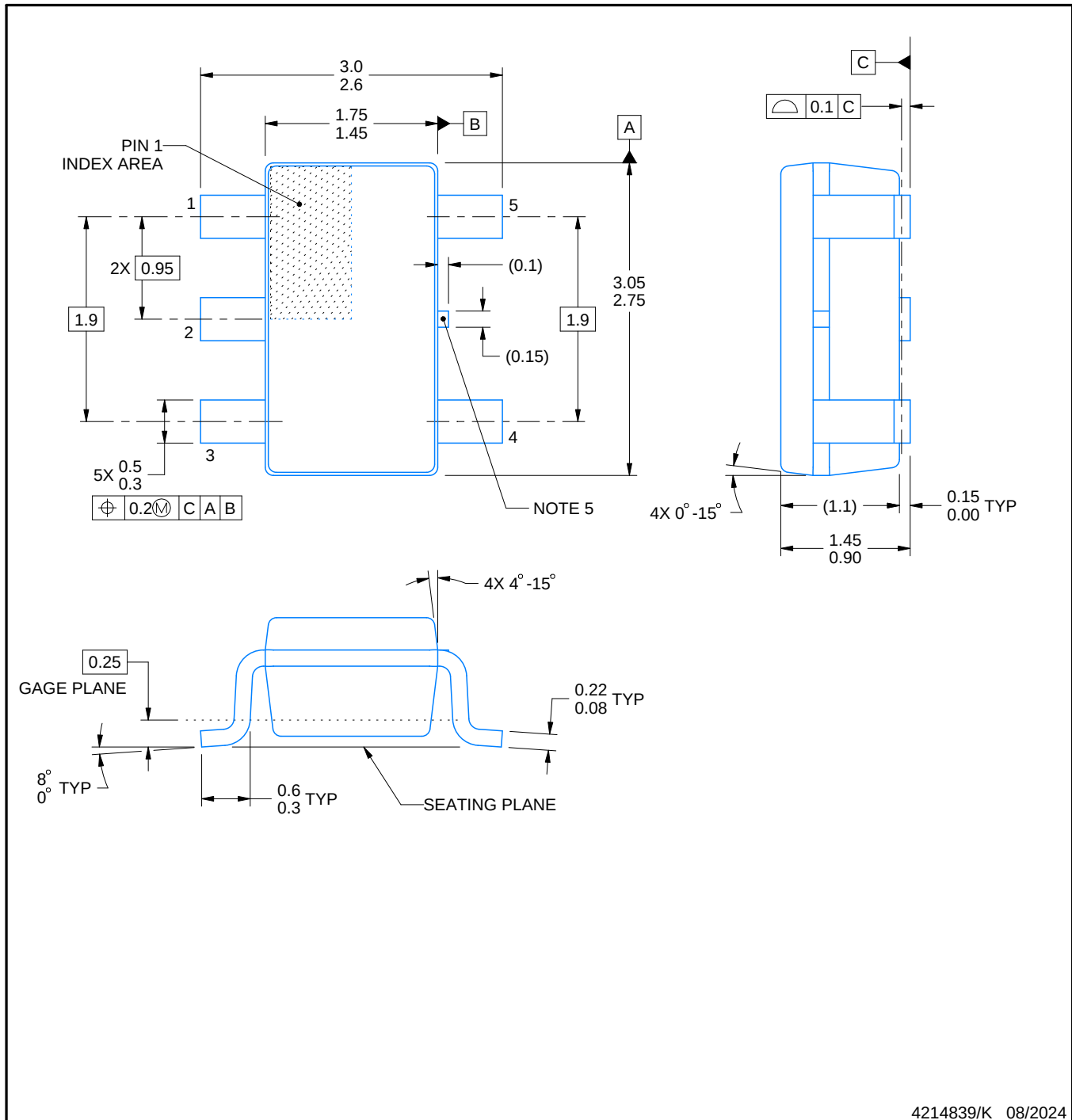
4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



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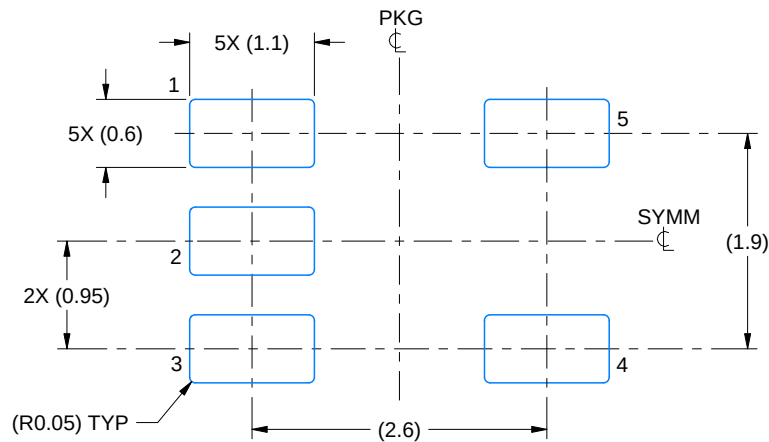
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

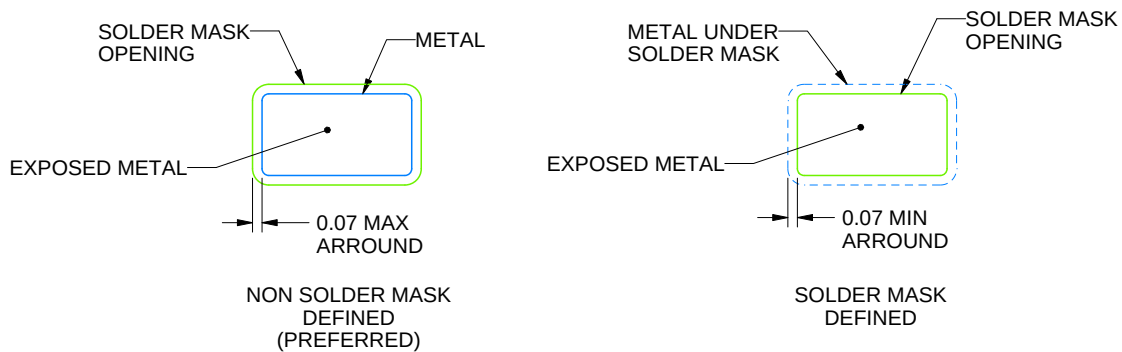
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

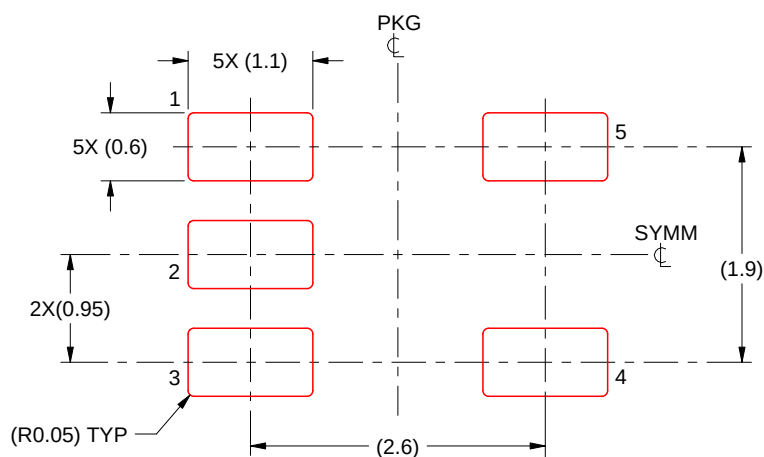
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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