

TL97x Output Rail-To-Rail Very-Low-Noise Operational Amplifiers

1 Features

- Rail-to-rail output voltage swing: $\pm 2.4V$ at $V_{CC} = \pm 2.5V$
- Very low noise level: $4nV/\sqrt{Hz}$
- Operating range: 2.7V to 12V

2 Applications

- Portable equipment:
 - Music players
 - Tablets
 - Cell phones
- Instrumentation and sensors
- Professional audio circuits

3 Description

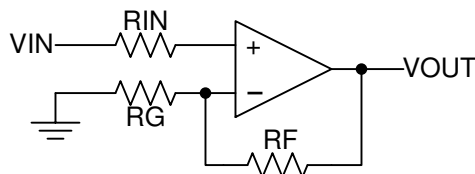
The TL97x family of single, dual, and quad operational amplifiers operates at voltages as low as $\pm 1.35V$ and features output rail-to-rail signal swing. The TL97x boast characteristics that make the devices practical for portable and battery-supplied equipment. Very low noise and low distortion characteristics makes the devices practical for audio preamplification.

The TL971 is housed in the space-saving 5-pin SOT-23 package, which simplifies board design because of the ability to be placed anywhere (outside dimensions are $2.9mm \times 1.6mm$).

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TL971	D (SOIC, 8)	4.90mm × 6.00mm
TL972	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.90mm × 6.00mm
	PW (TSSOP, 8)	3.00mm × 6.40mm
	DGK (VSSOP, 8)	3.00mm × 4.90mm
TL974	N (PDIP, 14)	19.30mm × 9.40mm
	D (SOIC, 14)	8.65mm × 6.00mm
	PW (TSSOP, 14)	5.00mm × 6.40mm

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



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4 Pin Configuration and Functions

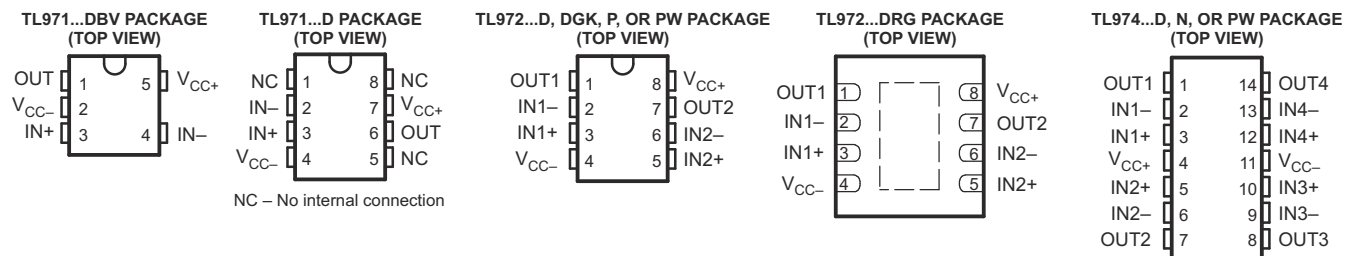


Table 4-1. Pin Functions

NAME	PIN					TYPE ⁽¹⁾	DESCRIPTION
	TL971	TL971	TL972		TL974		
	DBV	D	D, DGK, P, PW	DRG	D, N, PW		
IN+	3	3	—	—	—	I	Non-inverting input
IN–	4	2	—	—	—	I	Inverting input
IN1+	—	—	3	3	3	I	Non-inverting input
IN1–	—	—	2	2	2	I	Inverting input
IN2+	—	—	5	5	5	I	Non-inverting input
IN2–	—	—	6	6	6	I	Inverting input
IN3+	—	—	—	—	10	I	Non-inverting input
IN3–	—	—	—	—	9	I	Inverting input
IN4+	—	—	—	—	12	I	Non-inverting input
IN4–	—	—	—	—	13	I	Inverting input
NC	—	1	—	—	—	—	No Connect
		5					
		8					
OUT	1	6	—	—	—	O	Output
OUT1	—	—	1	1	1	O	Output
OUT2	—	—	7	7	7	O	Output
OUT3	—	—	—	—	8	O	Output
OUT4	—	—	—	—	14	O	Output
VCC+	5	7	8	8	4	—	Positive supply
VCC–	2	4	4	4	11	—	Negative supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	2.7	15	V
V _{ID}	Differential input voltage ⁽²⁾		±1V	V
V _{IN}	Input voltage range ⁽³⁾	V _{CC-} – 0.3	V _{CC+} + 0.3	V
T _J	Maximum junction temperature		150	°C
T _{stg}	Storage temperature range	–65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Differential voltages for the non-inverting input terminal are with respect to the inverting input terminal.
- (3) The input and output voltages must never exceed V_{CC} + 0.3V.

5.2 ESD Ratings Old Die

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	1500

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings New Die

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	12	V
V _{ICM}	Common-mode input voltage	V _{CC-} + 1.15	V _{CC+} – 1.15	V
T _A	Operating free-air temperature	–40	125	°C

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TL971		TL972					TL974			UNIT
		D ⁽²⁾	DBV ⁽²⁾	D ⁽²⁾	DGK ⁽³⁾	DRG ⁽³⁾	P ⁽²⁾	PW ⁽²⁾	D ⁽²⁾	N ⁽²⁾	PW ⁽²⁾	
		8 PINS	5 PINS	8 PINS					14 PINS			
R _{θ JA}	Package thermal impedance, junction to free air	97	206	97	172	44	85	149	86	80	113	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.
- (2) Package thermal impedance is calculated in accordance with JESD 51-7.

- (3) Package thermal impedance is calculated in accordance with JESD 51-5.

5.6 Electrical Characteristics

$V_{CC+} = 2.5V$, $V_{CC-} = -2.5V$, full-range $T_A = -40^{\circ}C$ to $125^{\circ}C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C	± 0.21		4	mV
			Full range			6	
αV_{IO}	Input offset voltage drift	$V_{ICM} = 0V$, $V_O = 0V$	25°C	± 0.25			$\mu V/^{\circ}C$
I_{IO}	Input offset current	$V_{ICM} = 0V$, $V_O = 0V$	25°C	± 0.01		150	nA
I_{IB}	Input bias current	$V_{ICM} = 0V$, $V_O = 0V$	25°C	± 0.01		750	nA
			Full range			1000	
V_{ICM}	Common-mode input voltage		25°C	-1.35		1.35	V
CMRR	Common-mode rejection ratio	$V_{ICM} = \pm 1.35V$	25°C	60	90		dB
SVR	Supply-voltage rejection ratio	$V_{CC} = \pm 2V$ to $\pm 3V$	25°C	60	70		dB
A_{VD}	Large-signal voltage gain	$R_L = 2k\Omega$	25°C	70	125		dB
V_{OH}	High-level output voltage	$R_L = 2k\Omega$	25°C	2	2.4		V
V_{OL}	Low-level output voltage	$R_L = 2k\Omega$	25°C		-2.4	-2	V
I_{source}	Output source current		25°C	1.2	65 ⁽¹⁾		mA
I_{sink}	Output sink current		25°C	50	-65 ⁽¹⁾		mA
I_{CC}	Supply current (per amplifier)	Unity gain, No load	25°C	2.48		2.8	mA
			Full range			3.2	
GBWP	Gain bandwidth product	$f = 100kHz$, $R_L = 2k\Omega$, $C_L = 100pF$	25°C	10.6			MHz
Φ_m	Phase margin at unity gain	$R_L = 2k\Omega$, $C_L = 100pF$	25°C	60			°
V_n	Equivalent input noise voltage	$f = 100kHz$	25°C	4.4			$nV/\sqrt{Hz}$
THD	Total harmonic distortion	$f = 1kHz$, $A_v = -1$, $R_L = 10k\Omega$	25°C	0.003			%

- (1) At high supply voltage, placing the TL97x in a sudden short to mid-supply or ground can lead to rapid thermal shutdown. Output current greater than I_{SC} can be achieved if rapid thermal shutdown is avoided as per [Figure 5-12](#) and [Figure 5-13](#).

5.7 Typical Characteristics

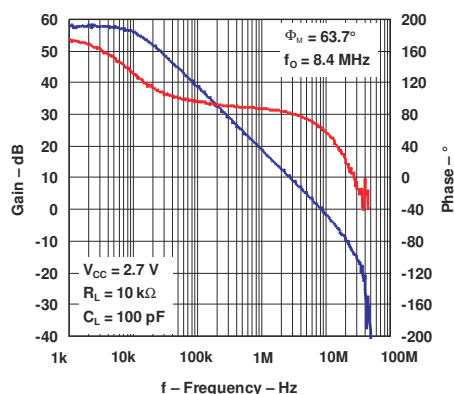


Figure 5-1. Gain And Phase vs Frequency, Old Die

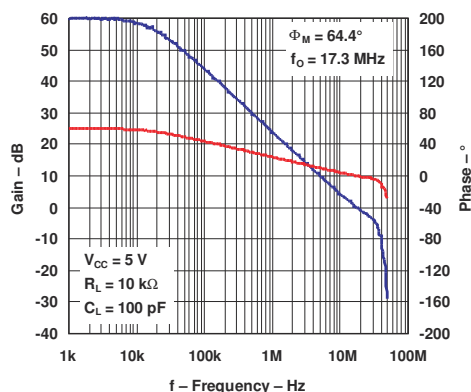


Figure 5-2. Gain And Phase vs Frequency, Old Die

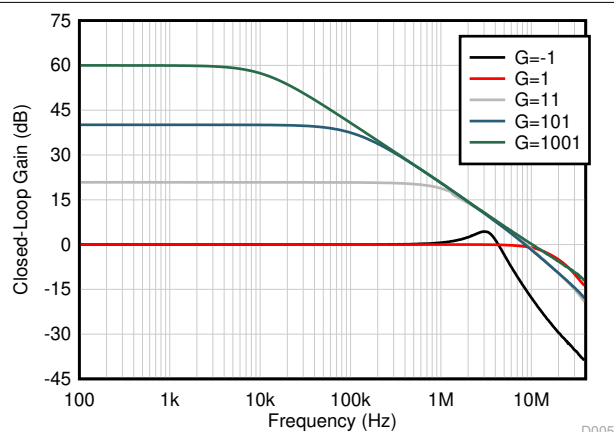


Figure 5-3. Closed-Loop Gain vs Frequency, New Die

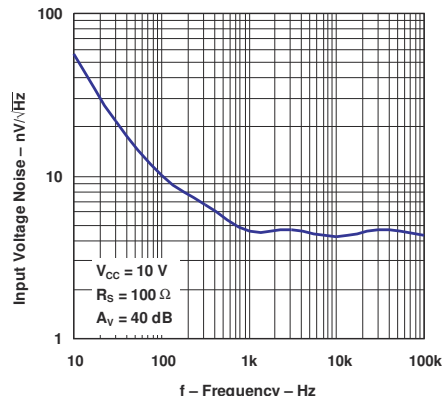


Figure 5-4. Input Voltage Noise vs Frequency, Old Die

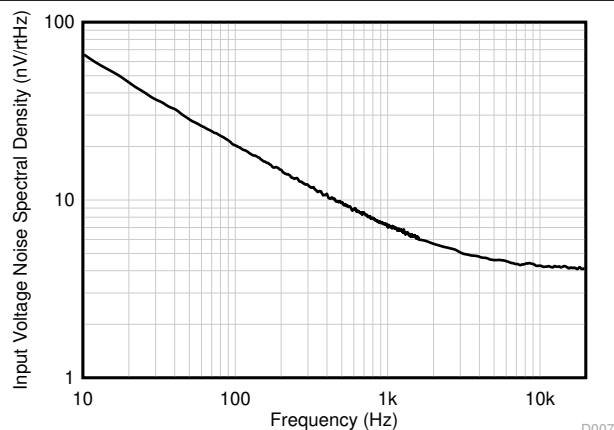


Figure 5-5. Input Voltage Noise Spectral Density vs Frequency, New Die

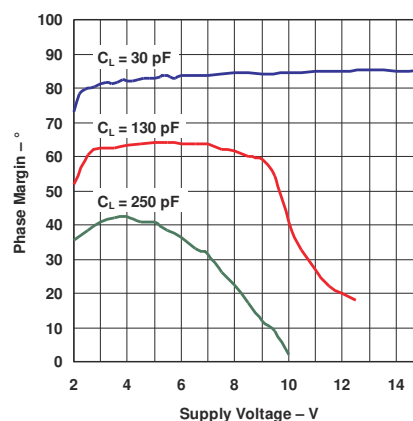


Figure 5-6. Phase Margin vs Supply Voltage, Old Die

5.7 Typical Characteristics (continued)

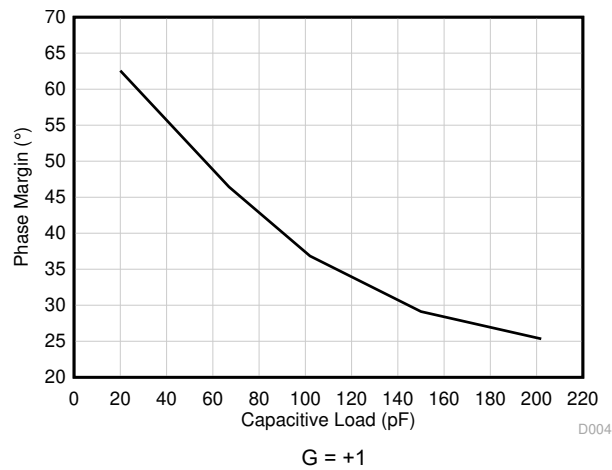


Figure 5-7. Phase Margin vs Capacitive Load, New Die

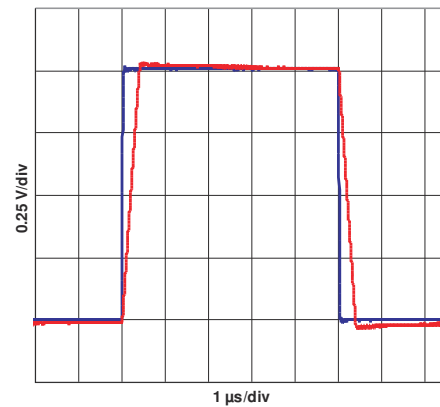


Figure 5-8. Input Response, Old Die

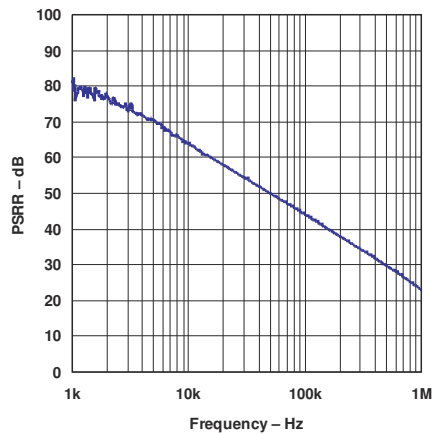


Figure 5-9. Power-Supply Ripple Rejection vs Frequency, Old Die

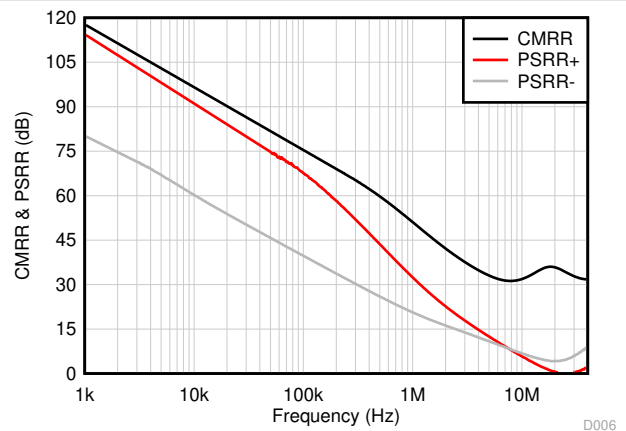


Figure 5-10. CMRR and PSRR vs Frequency, New Die

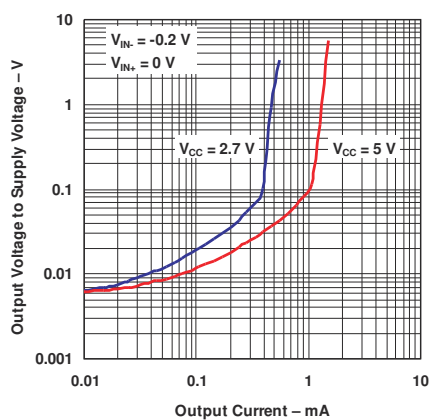


Figure 5-11. Output Voltage vs Output Current, Old Die

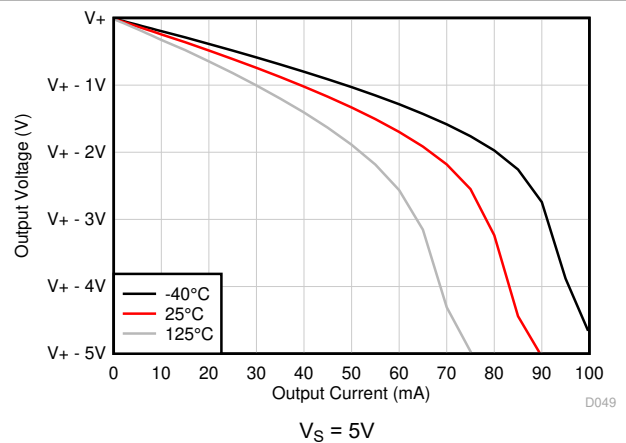


Figure 5-12. Output Voltage Swing vs Output Current (Sourcing), New Die

5.7 Typical Characteristics (continued)

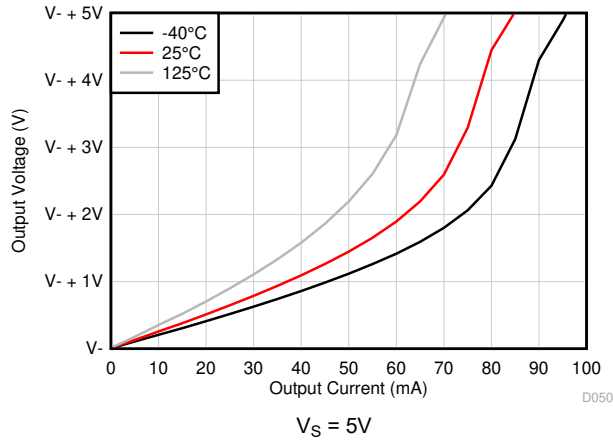


Figure 5-13. Output Voltage Swing vs Output Current (Sinking), New Die

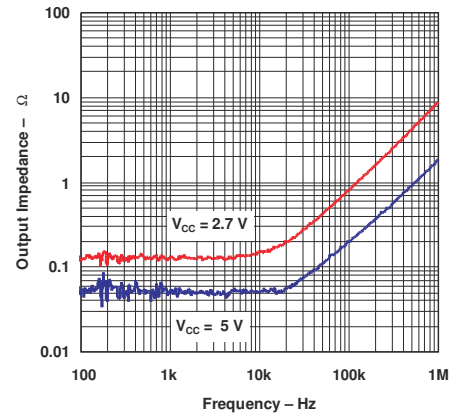


Figure 5-14. Output Impedance vs Frequency, Old Die

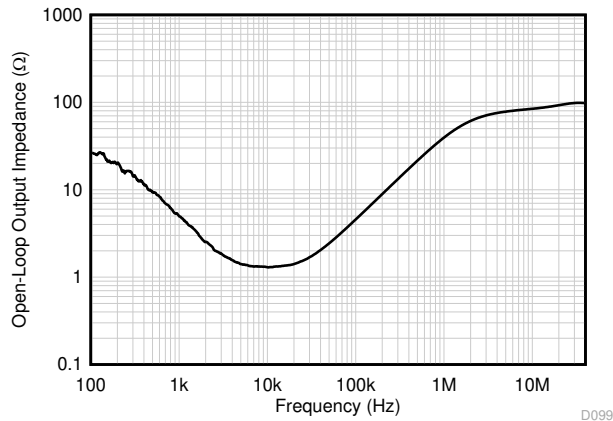


Figure 5-15. Open-Loop Output Impedance vs Frequency, New Die

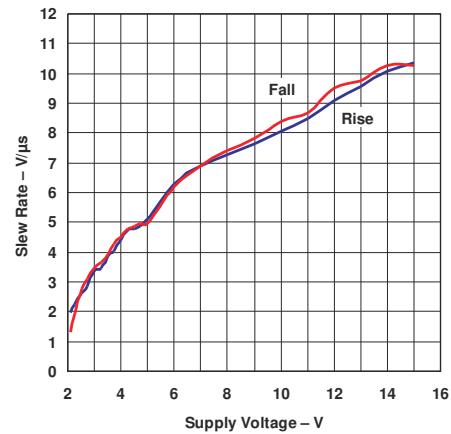


Figure 5-16. Slew Rate vs Supply Voltage, Old Die

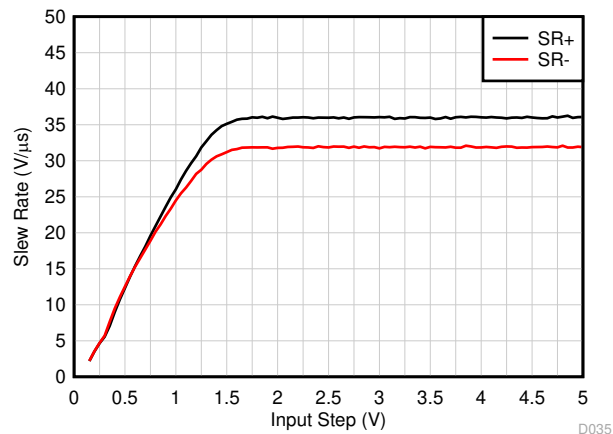


Figure 5-17. Slew Rate vs Input Step Voltage, New Die

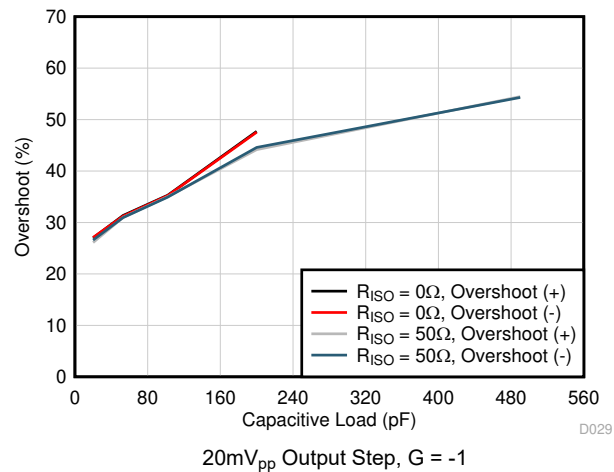


Figure 5-18. Small-Signal Overshoot vs Capacitive Load, New Die

5.7 Typical Characteristics (continued)

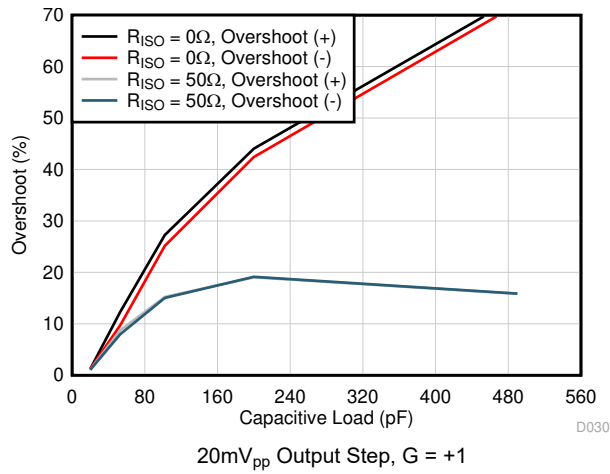


Figure 5-19. Small-Signal Overshoot vs Capacitive Load, New Die

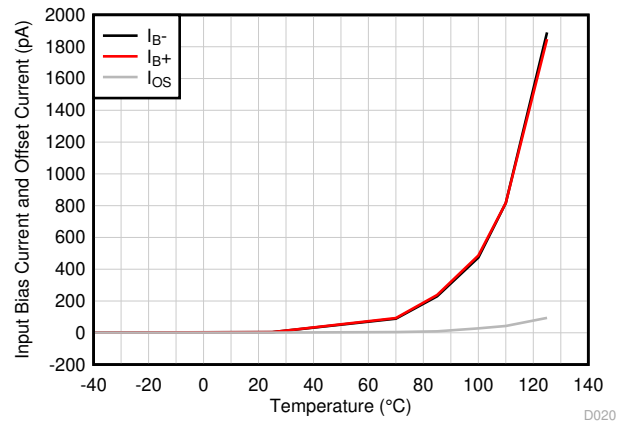


Figure 5-20. Input Bias Current and Offset Current vs Temperature, New Die

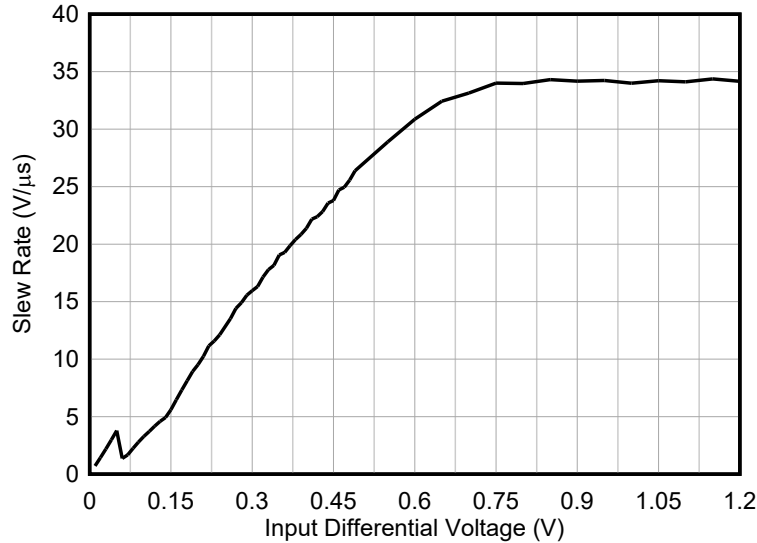


Figure 5-21. Slew Rate vs Input Differential Voltage, New Die

6 Detailed Description

6.1 Overview

The TL97x family of operational amplifiers operates at voltages as low as $\pm 1.35\text{V}$ and features output rail-to-rail signal swing. The TL97x boast characteristics that make the devices practical for portable and battery-supplied equipment. Very low noise and low distortion characteristics make the devices practical for audio preamplification. The TL97x family comes in single, dual, and quad operational amplifier packages of varying sizes.

The TL971 is housed in the space-saving 5-pin SOT-23 package, which simplifies board design because of the ability to be placed anywhere (outside dimensions are $2.9\text{mm} \times 1.6\text{mm}$).

6.2 Feature Description

6.2.1 Common-Mode Voltage Range

The OPA97x is a 12V, true rail-to-rail input operational amplifier with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in [Figure 6-1](#). The N-channel pair is active for input voltages close to the positive rail, typically from $(V+) - 1\text{V}$ to the positive supply. The P-channel pair is active for inputs from the negative supply to approximately $(V+) - 2\text{V}$. There is a small transition region, typically $(V+) - 2\text{V}$ to $(V+) - 1\text{V}$, in which both input pairs are on. This transition region can vary modestly with process variation. Within this region, PSRR, CMRR, offset voltage, offset drift, noise, and THD performance can be degraded compared to operation outside this region.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see the [Op Amps with Complementary-Pair Input Stages](#) analog design journal.

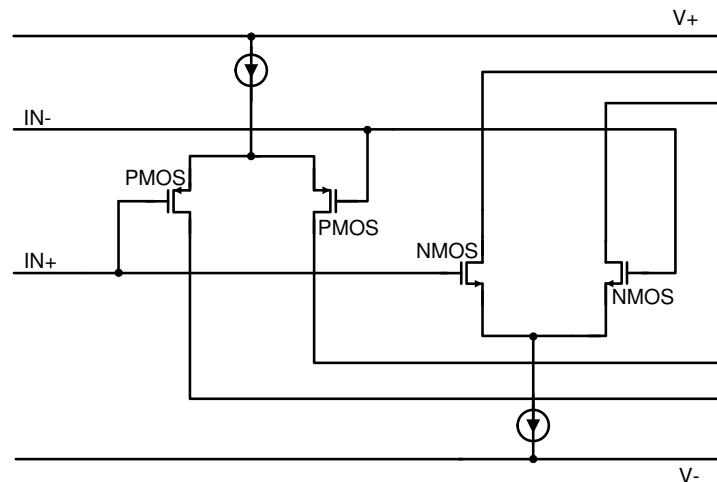


Figure 6-1. Rail-to-Rail Input Stage

6.2.2 Operating Voltage

The TL97x devices are fully specified for operation from 2.7V to 12V. In addition, many specifications apply from -40°C to 125°C .

6.3 Device Functional Modes

The TL97x devices are powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal is used to drive a relatively high current load. This circuit is also called a buffer amplifier or unity gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so the amplifier can provide as much current as necessary to the output load.

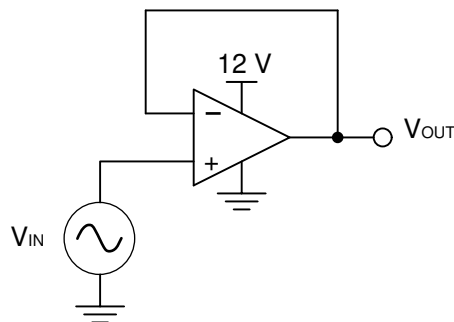


Figure 7-1. Voltage Follower Schematic

7.1.1 Design Requirements

- Input at positive Terminal
- Output range of 0V to 12V
- Input range of 0V to 12V
- Short-circuit feedback to negative input for unity gain

7.1.2 Detailed Design Procedure

7.1.2.1 Output Voltage Swing

The internal circuitry of an operational amplifier limits the output voltage to some level below the supply rails. For this amplifier, the output voltage must be within $\pm 12\text{V}$.

7.2 Power Supply Recommendations

The TL97x devices are specified for operation from 2.7V to 12V; many specifications apply from -40°C to 125°C .

CAUTION

Supply voltages larger than 15V can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1 μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout Guidelines](#).

7.3 Layout

7.3.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1 μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is a simple and effective method of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If keeping the input traces separate from the supply or output traces is not possible, cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

7.3.2 Layout Example

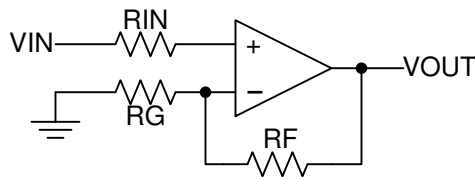


Figure 7-2. Operational Amplifier Schematic for Non-Inverting Configuration

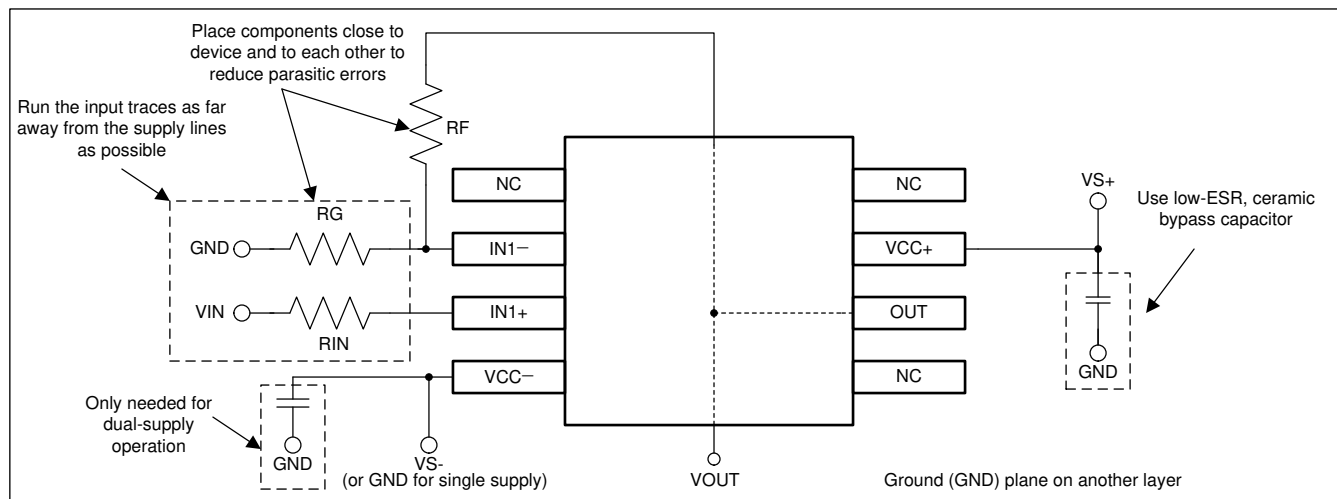


Figure 7-3. Operational Amplifier Board Layout for Non-Inverting Configuration

8 Device and Documentation Support

8.1 Third-Party Products Disclaimer

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8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision H (January 2015) to Revision I (July 2026)	Page
• Deleted Ultra-low Distortion and High Dynamic Features.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated Device Information table.....	1
• Updated package dimensions in text in Description to match updated Device Information table.....	1
• Added <i>ESD Ratings New Die</i> section.....	4
• Updated Input offset voltage typical value from 1mV to $\pm 0.21\text{mV}$	6
• Updated Input offset voltage drift typical value from $5\mu\text{V}/^\circ\text{C}$ to $\pm 0.25\mu\text{V}/^\circ\text{C}$	6
• Updated Input offset current typical value from 10nA to $\pm 0.01\text{nA}$	6
• Updated Input bias current typical value from 200nA to $\pm 0.01\text{nA}$	6
• Updated Common-mode rejection ratio typical value from 85dB to 90dB.....	6
• Updated Large-signal voltage gain typical value from 80dB to 125dB.....	6
• Removed Output source current Full Range values.....	6
• Removed Output sink current Full Range values.....	6
• Removed Gain bandwidth product minimum value.....	6
• Removed Slew Rate spec.....	6
• Removed Gain Margin spec.....	6
• Updated Equivalent input noise voltage typical value from $4\text{nV}/\sqrt{\text{Hz}}$ to $4.4\text{nV}/\sqrt{\text{Hz}}$	6
• Updated Output source current typical value from 1.4mA to 65mA.....	6
• Updated Output sink current typical value from 80mA to -65mA	6
• Updated <i>Typical Characteristics</i> as per New Die characteristics.....	7
• Updated package dimensions in text to match updated Device Information table in <i>Description</i> section.....	11
• Added <i>Common-Mode Voltage Range</i> section.....	11
• Removed <i>Slew Rate</i> section.....	11
• Removed <i>Unity-Gain Bandwidth</i> section.....	11
• Removed <i>Low Total Harmonic Distortion</i> section.....	11
• Removed <i>Application Information</i> section.....	12
• Removed <i>Supply and Input voltage</i> section.....	12

Changes from Revision G (May 2012) to Revision H (January 2015)	Page
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Deleted <i>Ordering Information</i> table.....	1

Changes from Revision F (December 2009) to Revision G (May 2012)	Page
• Changed slew rate MIN value.....	6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL971ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 125	Z971
TL971IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z971
TL971IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z971
TL971IDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	
TL972ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 125	Z972
TL972IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TSA
TL972IDGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TSA
TL972IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL972IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL972IDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL972IDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL972IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL972IP
TL972IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL972IP
TL972IPE4	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	Call TI	-40 to 125	
TL972IPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL972IPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL974ID	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I
TL974ID.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I
TL974IDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I
TL974IDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I
TL974IN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL974IN
TL974IN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL974IN
TL974INE4	Active	Production	PDIP (N) 14	25 TUBE	-	Call TI	Call TI	-40 to 125	
TL974IPW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974
TL974IPW.A	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974
TL974IPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	Z974
TL974IPWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974
TL974IPWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

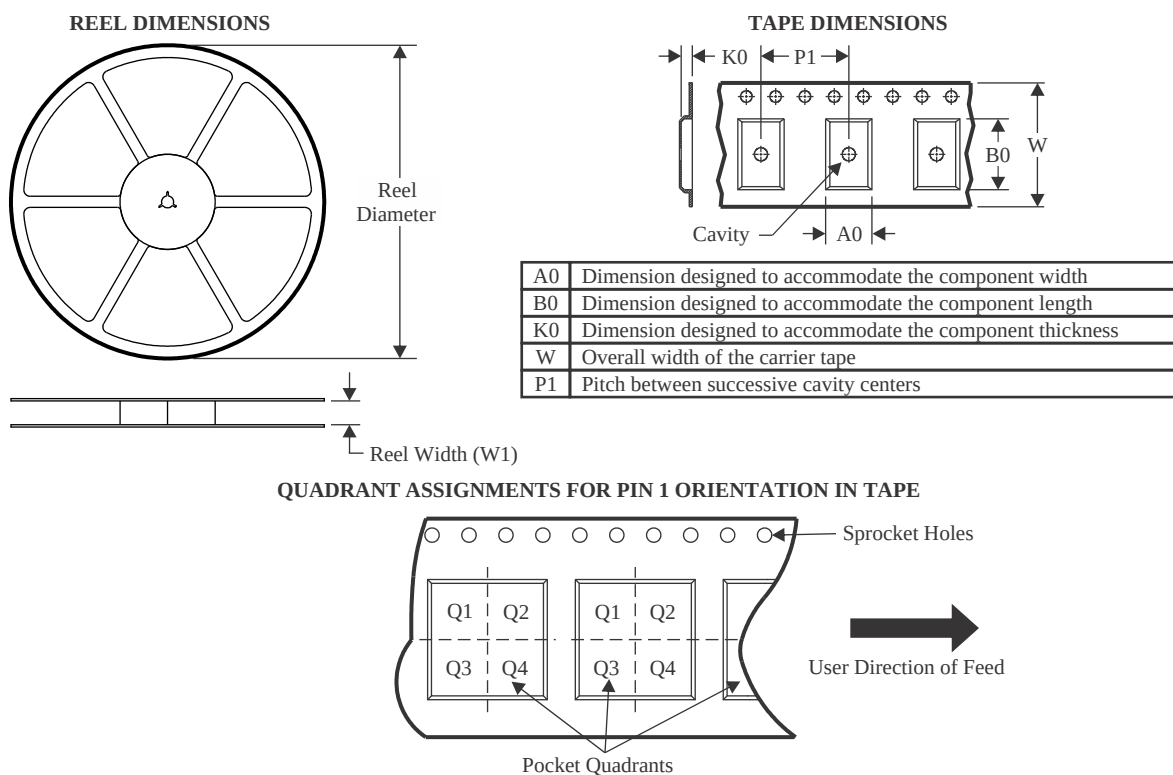
OTHER QUALIFIED VERSIONS OF TL971, TL972, TL974 :

- Automotive : [TL971-Q1](#), [TL972-Q1](#), [TL974-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

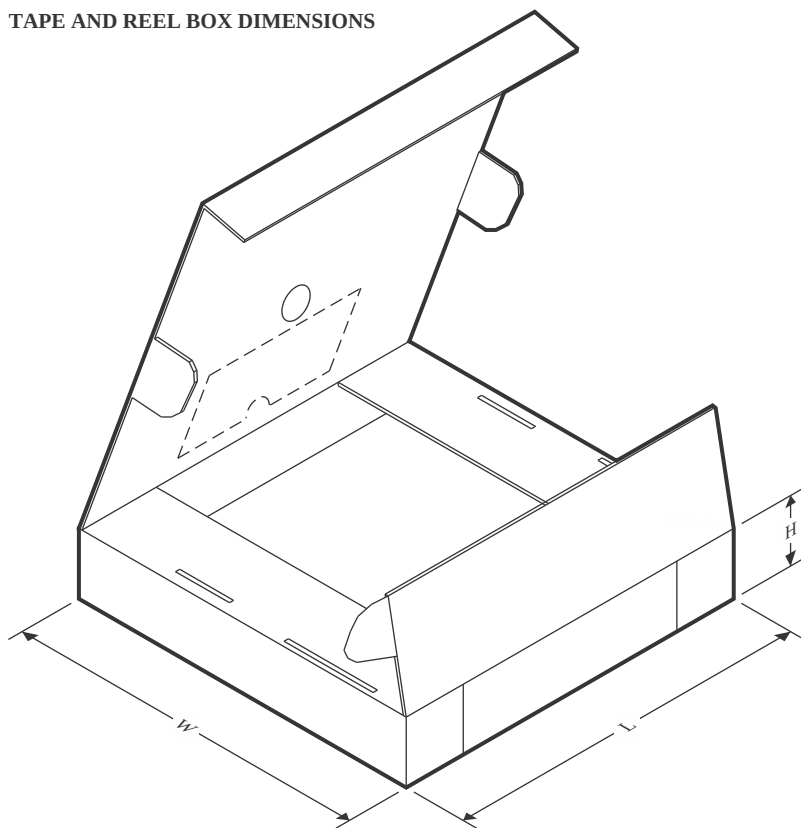
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL971IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL971IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL971IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TL972IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL974IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL974IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL974IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL974IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL974IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

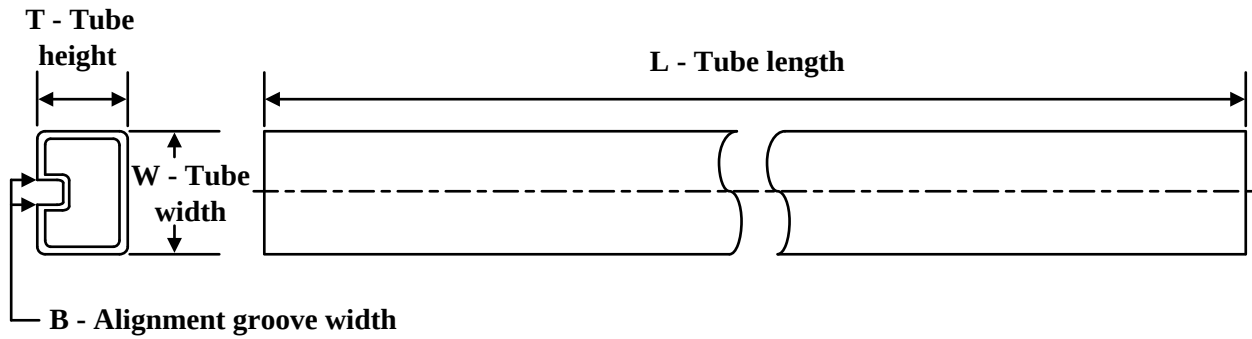
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

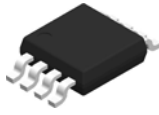
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL971IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL971IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL971IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL972IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TL972IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL972IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL972IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TL972IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL974IDR	SOIC	D	14	2500	353.0	353.0	32.0
TL974IDR	SOIC	D	14	2500	353.0	353.0	32.0
TL974IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL974IPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
TL974IPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE

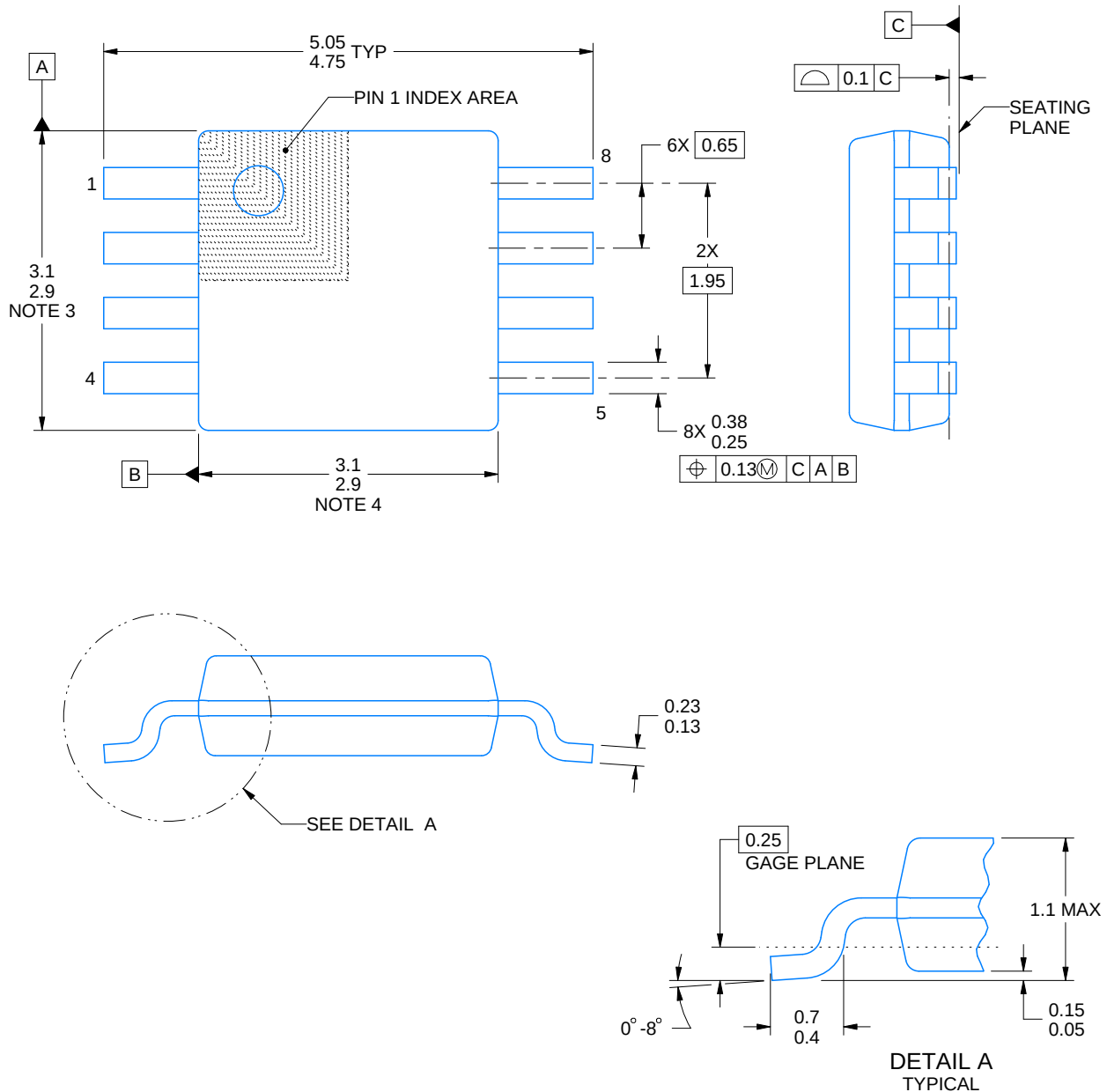


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TL972IP	P	PDIP	8	50	506	13.97	11230	4.32
TL972IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL974ID	D	SOIC	14	50	507	8	3940	4.32
TL974ID.A	D	SOIC	14	50	507	8	3940	4.32
TL974IN	N	PDIP	14	25	506	13.97	11230	4.32
TL974IN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL974IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TL974IPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

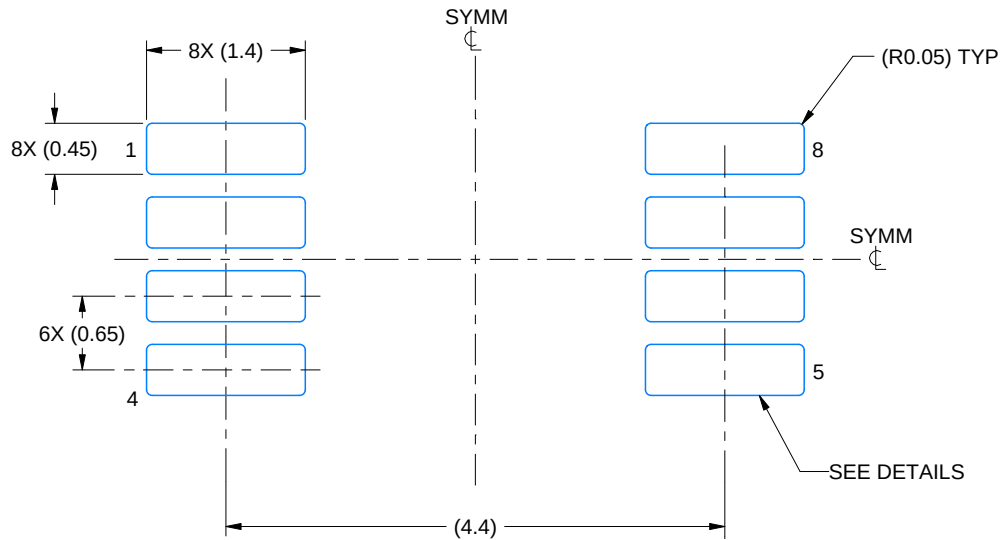
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

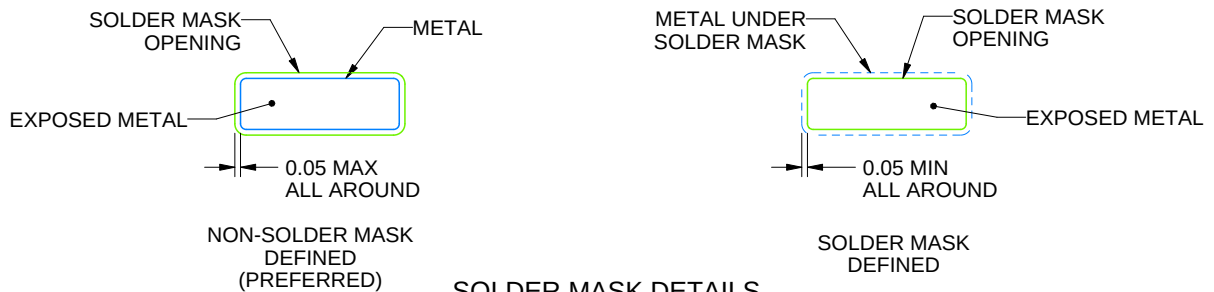
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

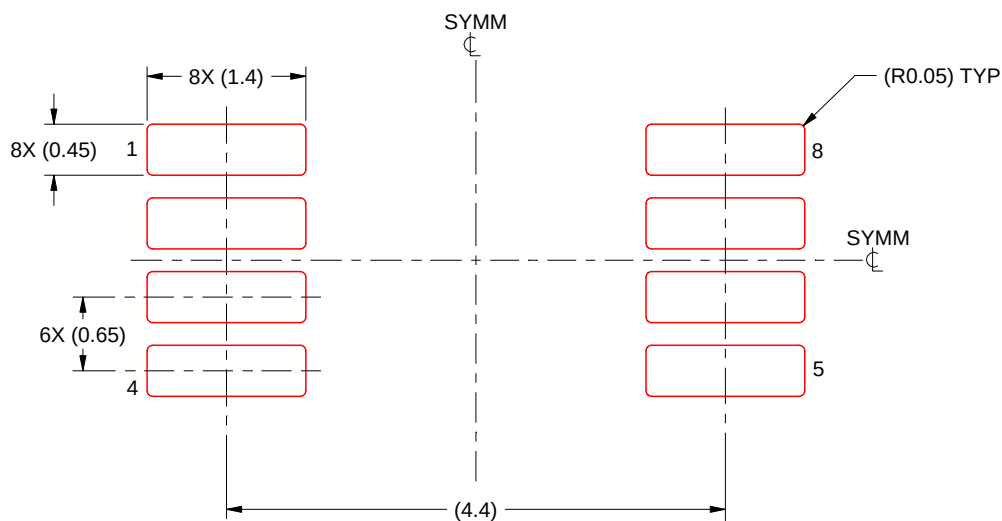
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

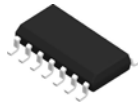


SOLDER PASTE EXAMPLE
SCALE: 15X

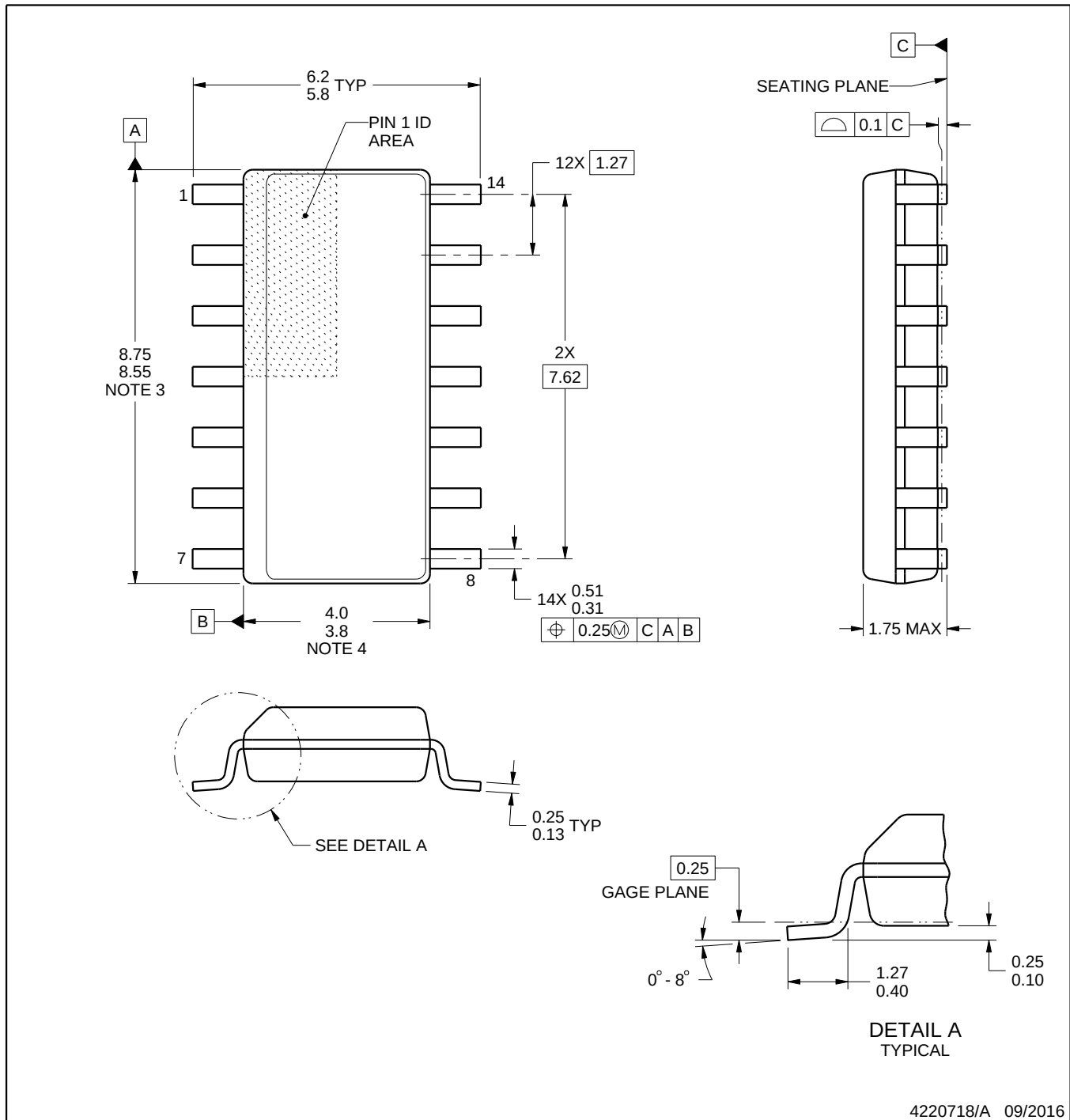
4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

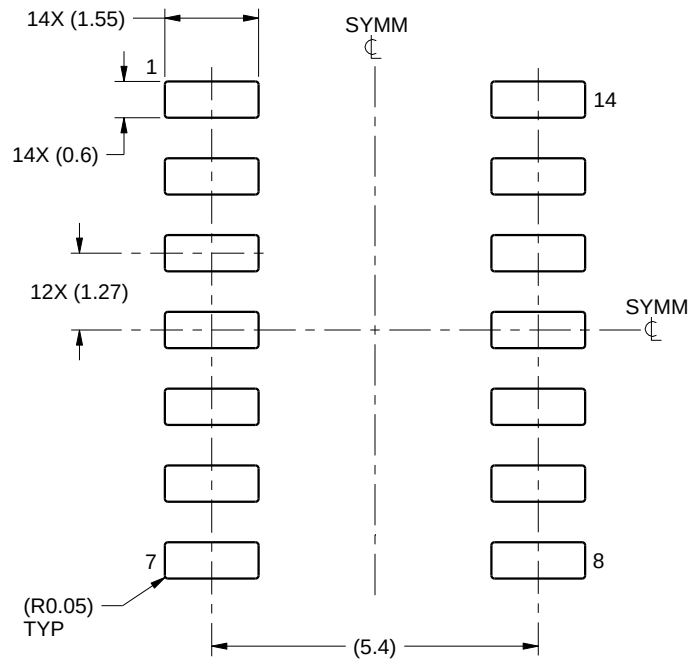


EXAMPLE BOARD LAYOUT

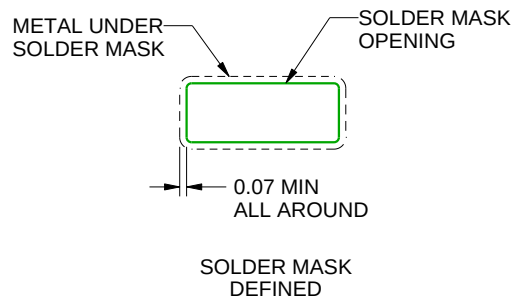
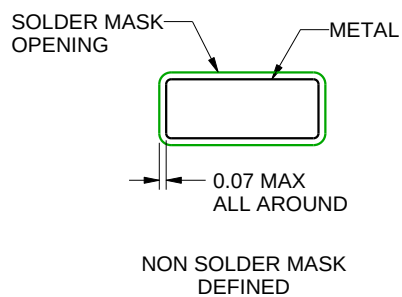
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

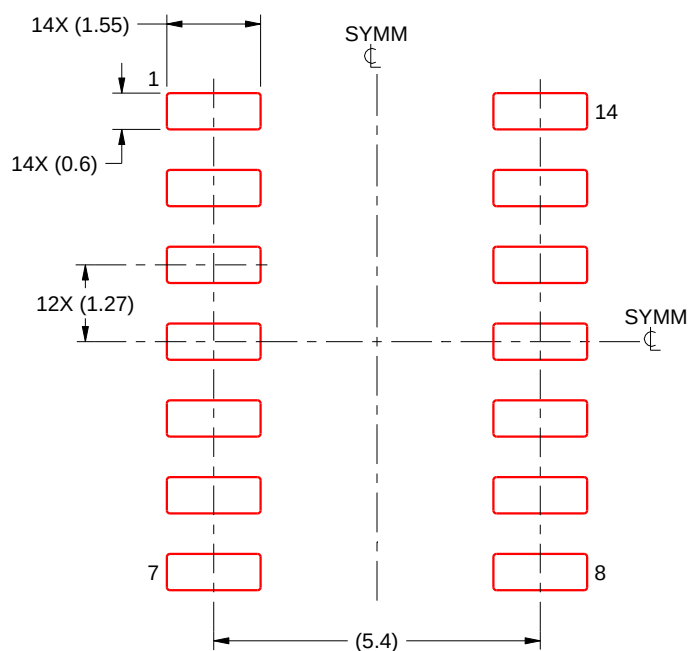
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



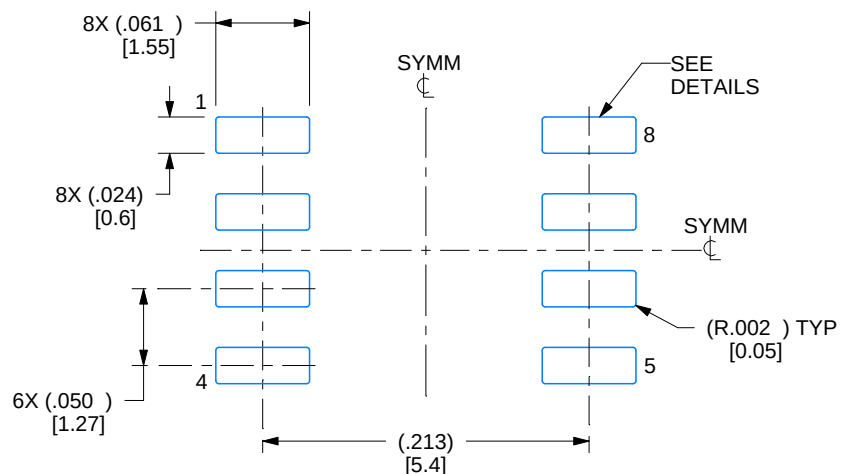
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

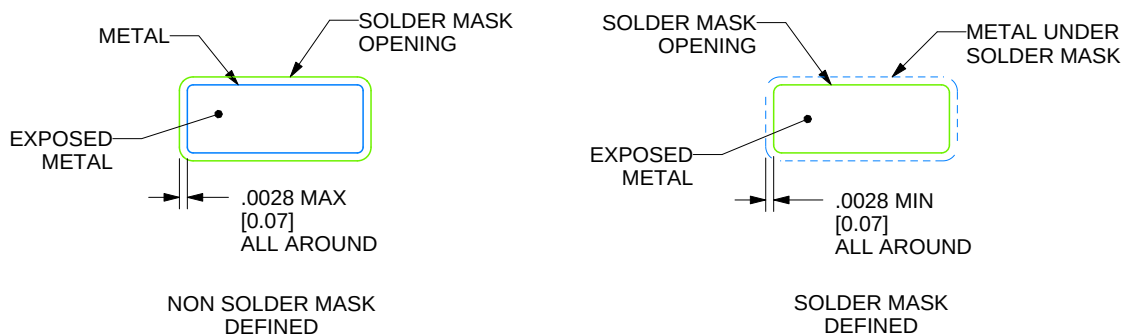
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

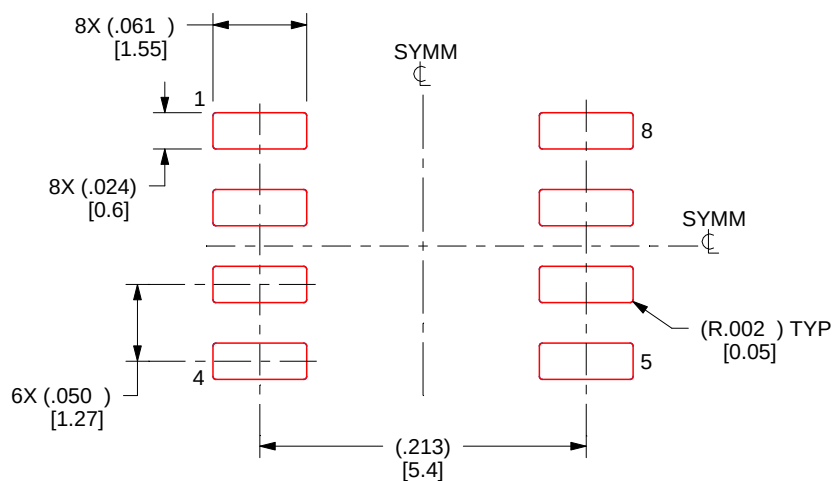
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

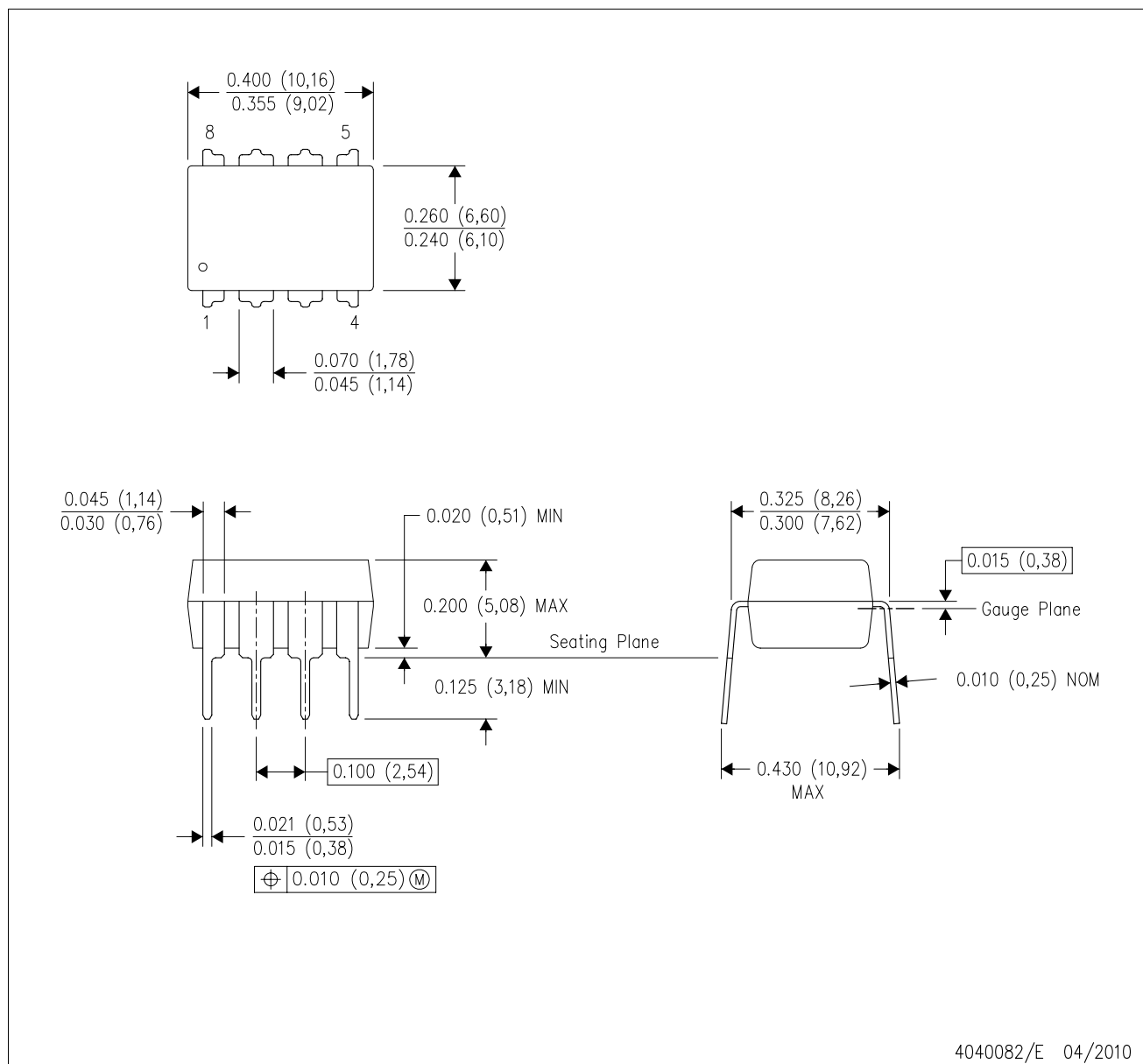
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

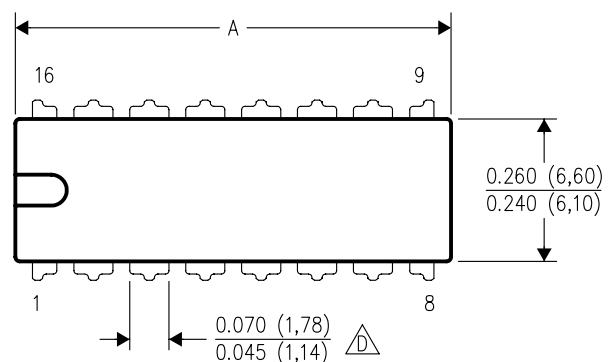


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

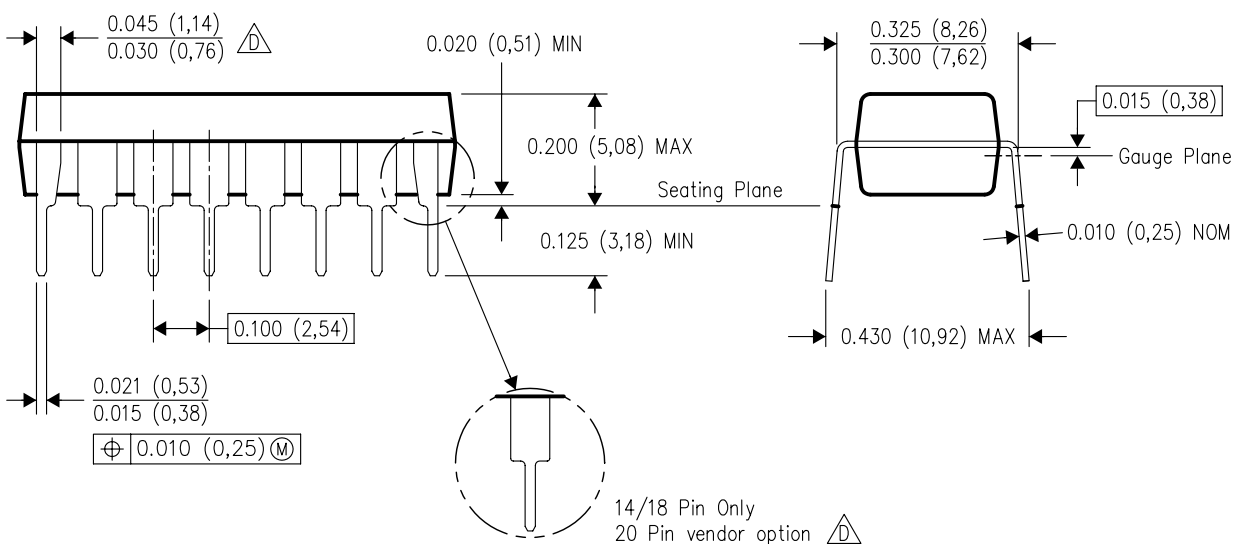
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

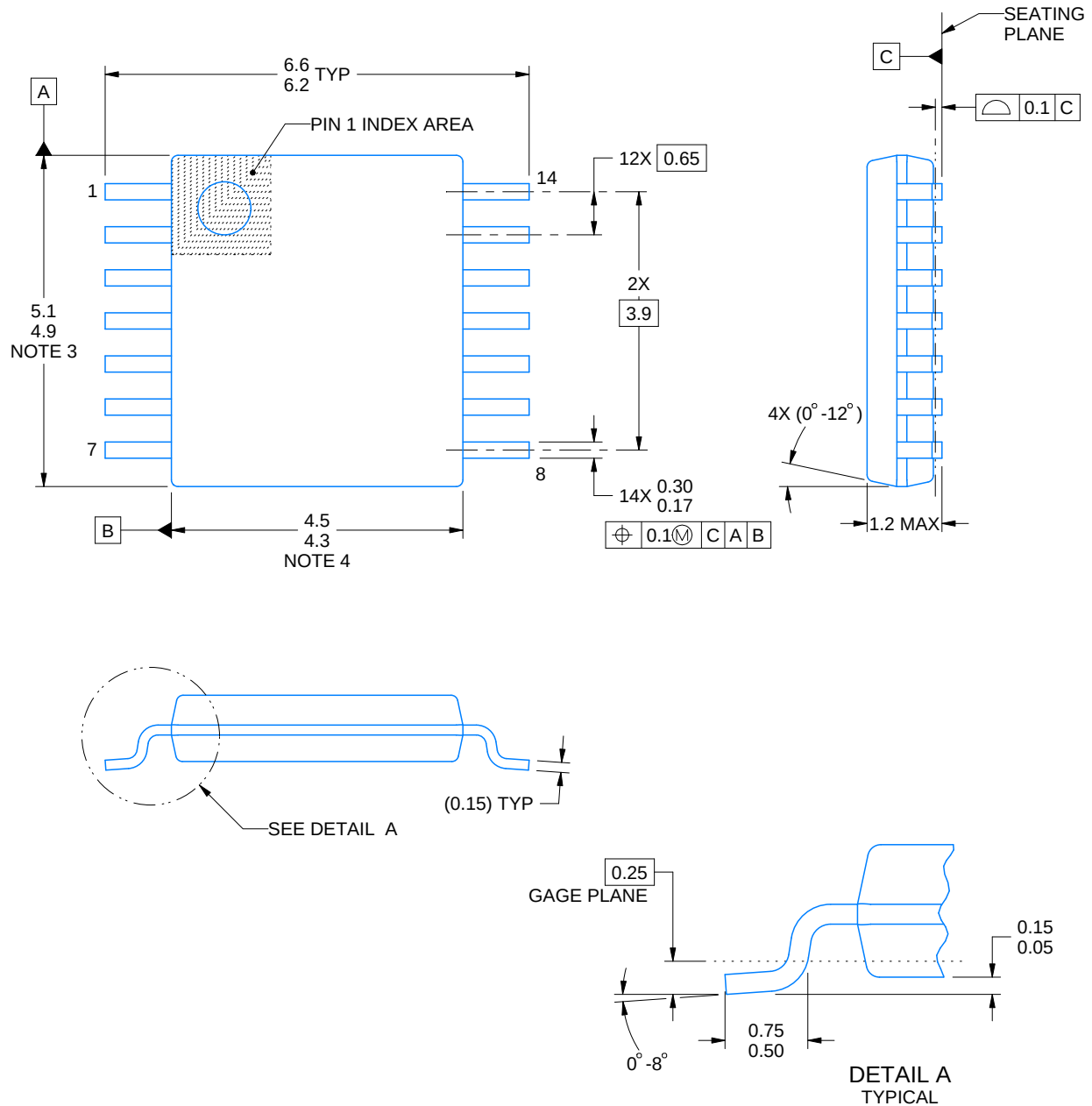
- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

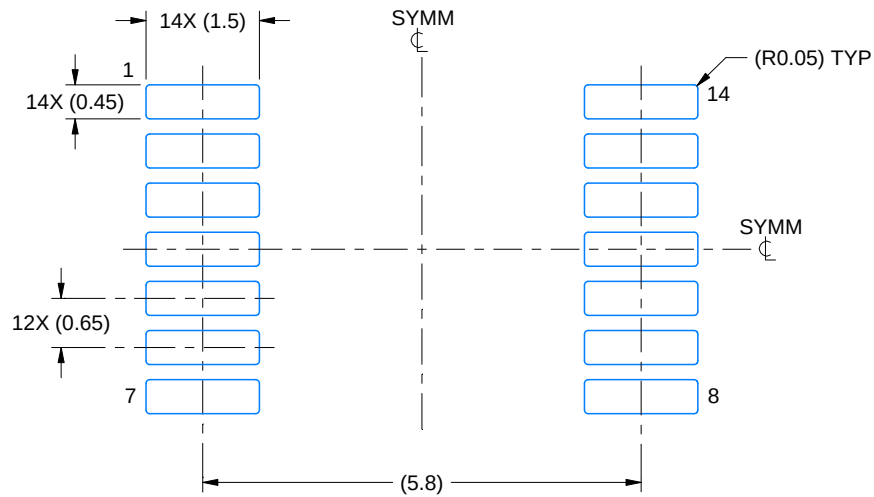
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

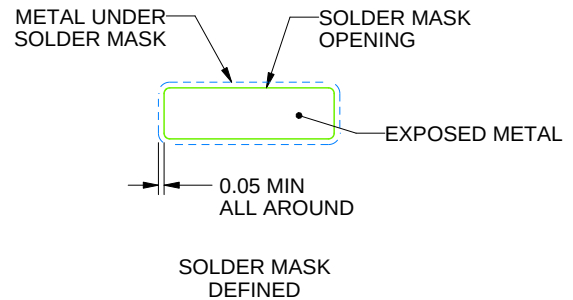
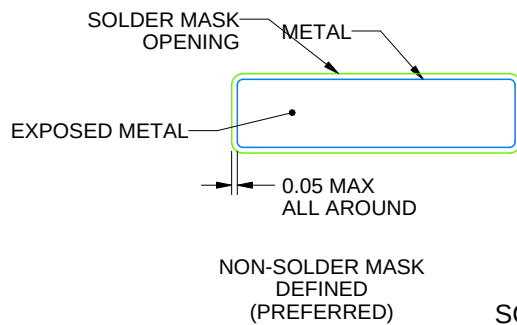
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

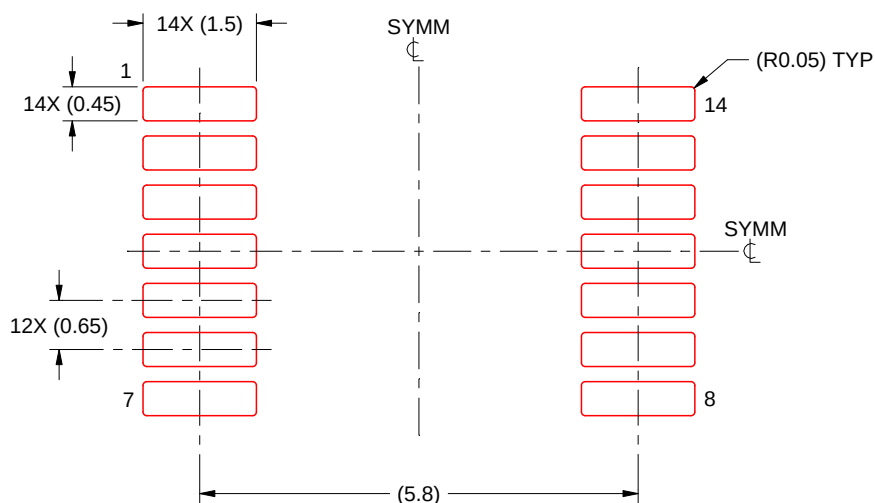
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

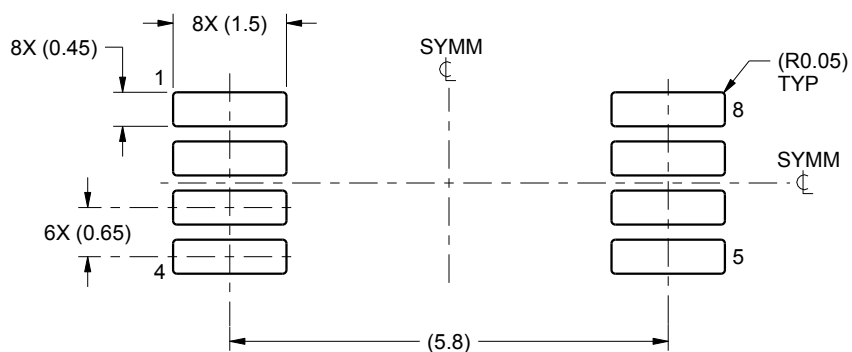
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

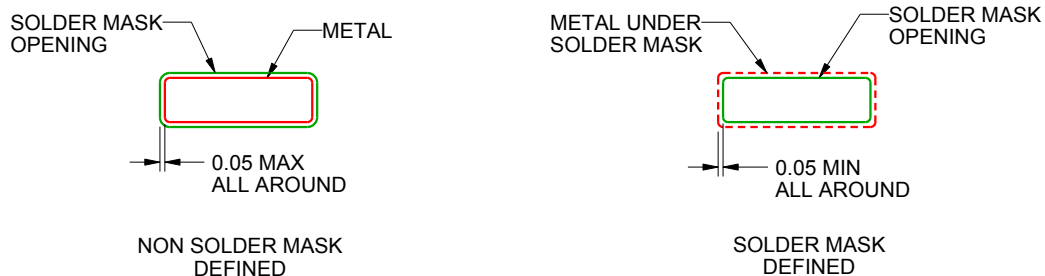
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

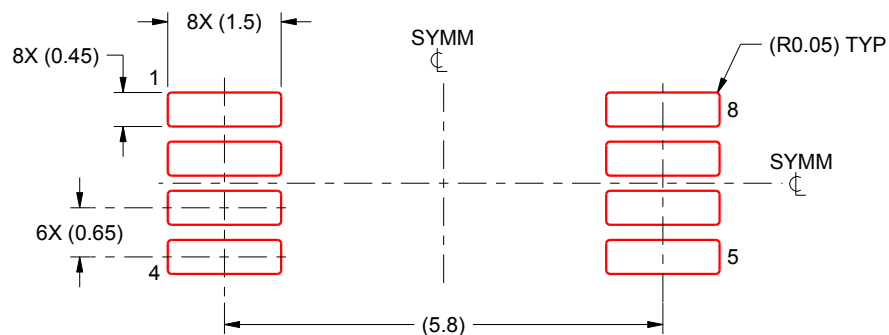
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025