Table 9. STM32F030x4/x6/x8/xC SPI implementation(1)

SPI features	SPI1	SPI2(2)
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
TI mode	X	X

1. X = supported.
2. Not available on STM32F030x4/6.

3.16 Serial wire debug port (SW-DP)

An Arm SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts and pin descriptions

Figure 4. LQFP64 64-pin package pinout (top view), for STM32F030x4/6/8 devices

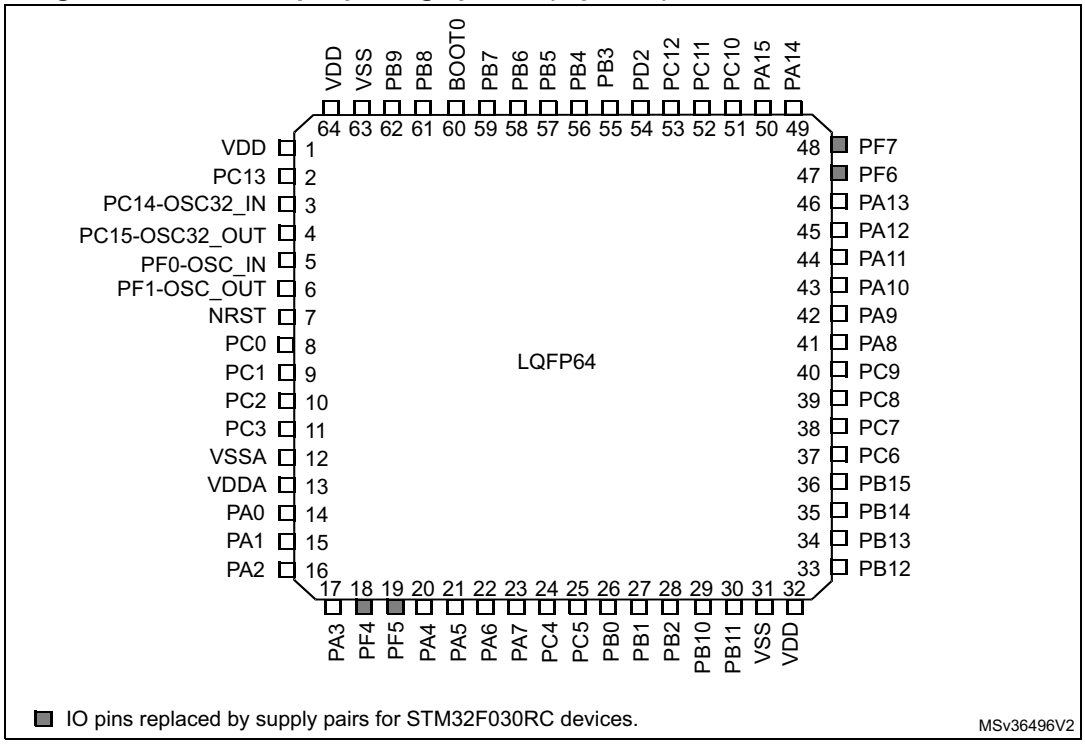


Figure 5. LQFP64 64-pin package pinout (top view), for STM32F030RC devices

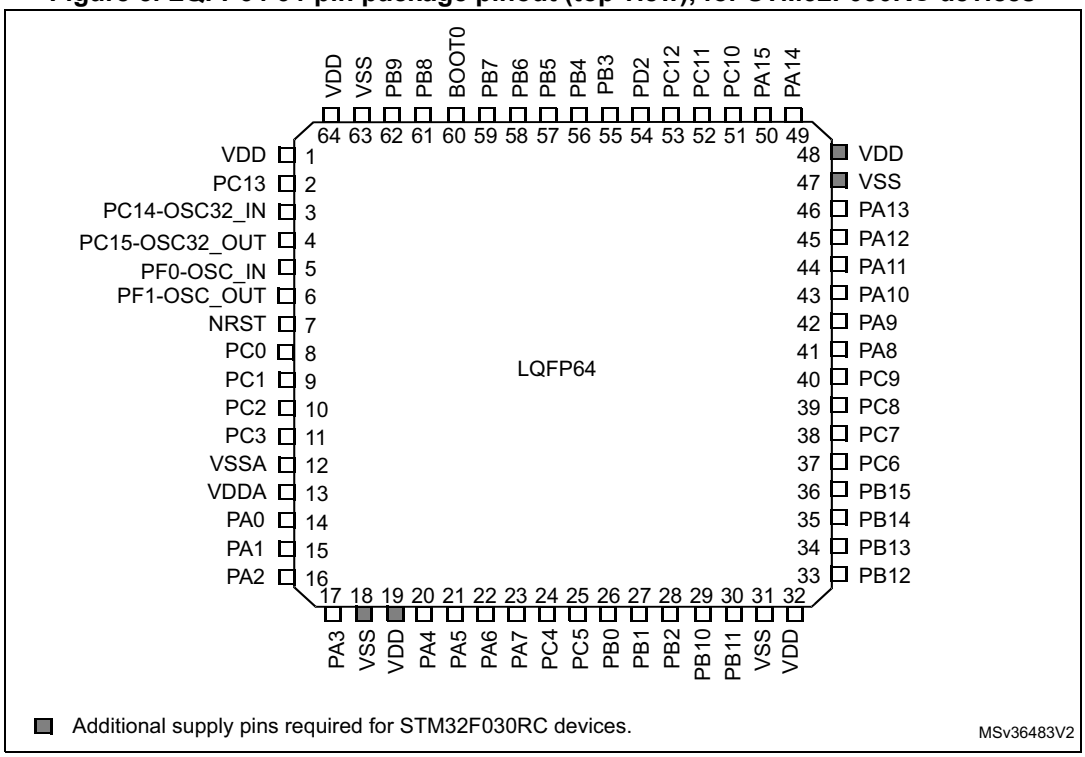


Figure 6. LQFP48 48-pin package pinout (top view), for STM32F030x4/6/8 devices

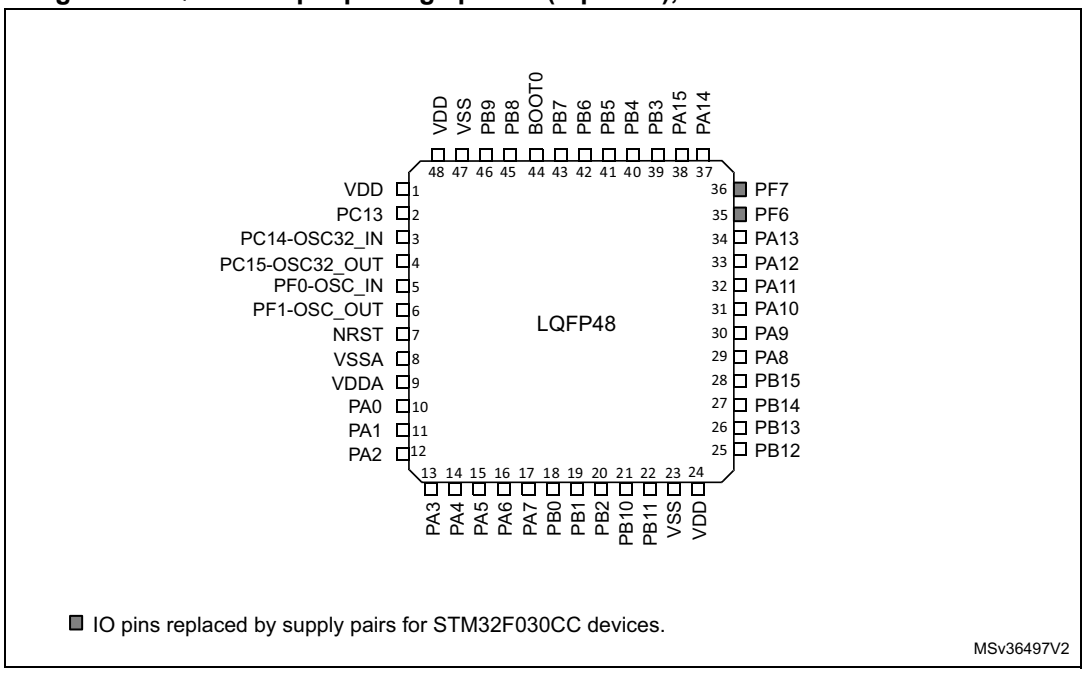


Figure 7. LQFP48 48-pin package pinout (top view), for STM32F030CC devices

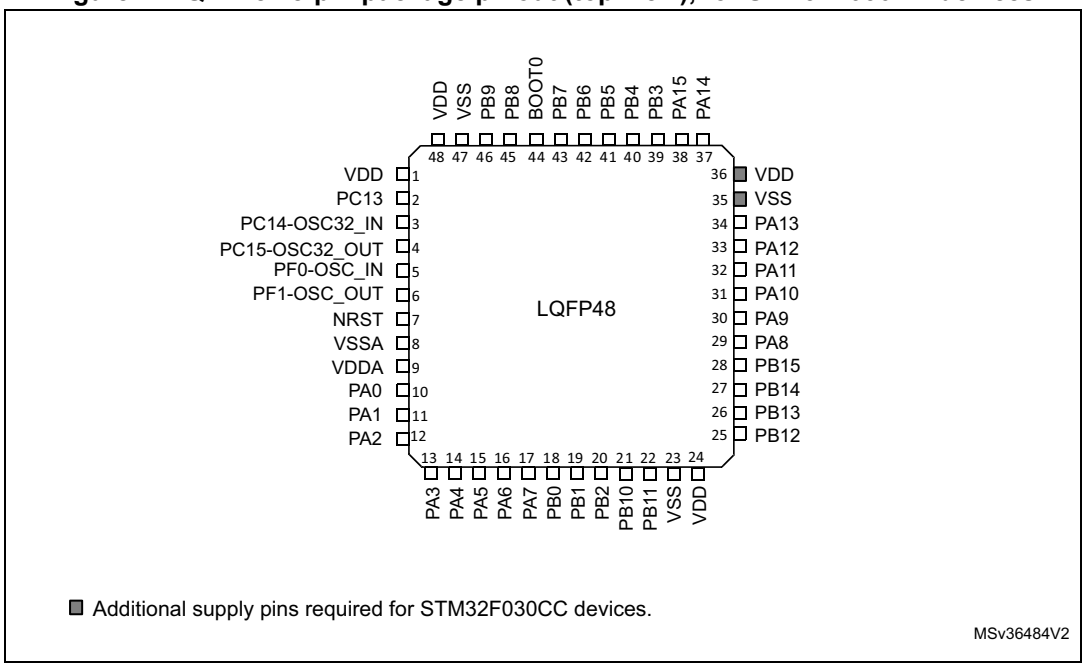


Figure 8. LQFP32 32-pin package pinout (top view)

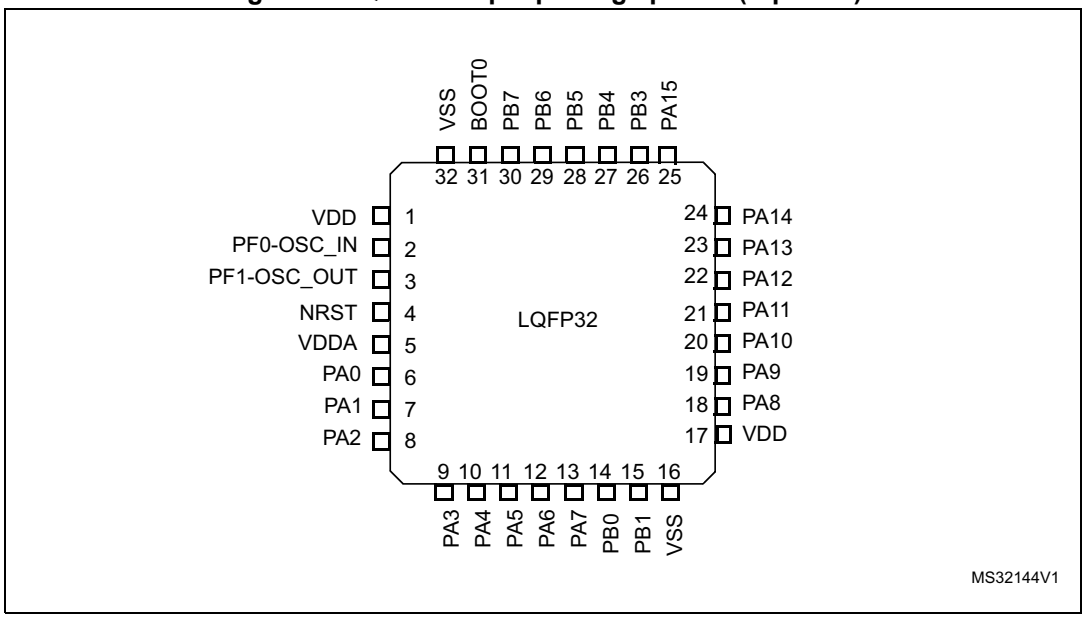


Figure 9. TSSOP20 20-pin package pinout (top view)

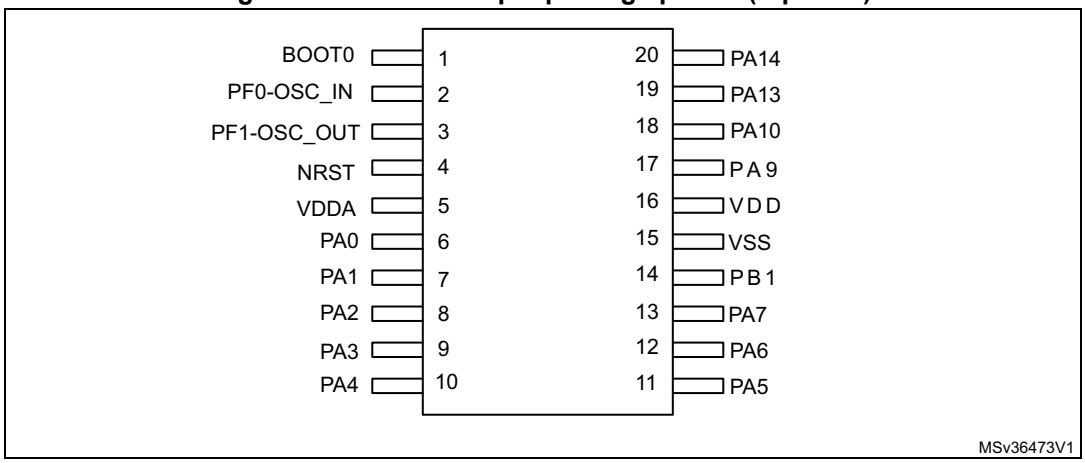


Table 10. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 11. STM32F030x4/6/8/C pin definitions

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
1	1	-	-	VDD	S	-	-	Complementary power supply	
2	2	-	-	PC13	I/O	TC	(1)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	3	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1)	-	OSC32_IN
4	4	-	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1)	-	OSC32_OUT
5	5	2	2	PF0-OSC_IN (PF0)	I/O	FT	-	I2C1_SDA(5)	OSC_IN
6	6	3	3	PF1-OSC_OUT (PF1)	I/O	FT	-	I2C1_SCL(5)	OSC_OUT
7	7	4	4	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	

Table 11. STM32F030x4/6/8/C pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
8	-	-	-	PC0	I/O	TTa	-	EVENTOUT, USART6_TX(5)	ADC_IN10
9	-	-	-	PC1	I/O	TTa	-	EVENTOUT, USART6_RX(5)	ADC_IN11
10	-	-	-	PC2	I/O	TTa	-	SPI2_MISO(5), EVENTOUT	ADC_IN12
11	-	-	-	PC3	I/O	TTa	-	SPI2_MOSI(5), EVENTOUT	ADC_IN13
12	8	-	-	VSSA	S	-	-	Analog ground	
13	9	5	5	VDDA	S	-	-	Analog power supply	
14	10	6	6	PA0	I/O	TTa	-	USART1_CTS(2), USART2_CTS(3)(5), USART4_TX(5)	ADC_IN0, RTC_TAMP2, WKUP1
15	11	7	7	PA1	I/O	TTa	-	USART1_RTS(2), USART2_RTS(3)(5), EVENTOUT, USART4_RX(5)	ADC_IN1
16	12	8	8	PA2	I/O	TTa	-	USART1_TX(2), USART2_TX(3)(5), TIM15_CH1(3)(5)	ADC_IN2, WKUP4(5)
17	13	9	9	PA3	I/O	TTa	-	USART1_RX(2), USART2_RX(3)(5), TIM15_CH2(3)(5)	ADC_IN3
18(4)	-	-	-	PF4	I/O	FT	(4)	EVENTOUT	-
18(5)	-	-	-	VSS	S	-	(5)	Ground	
19(4)	-	-	-	PF5	I/O	FT	(4)	EVENTOUT	-
19(5)	-	-	-	VDD	-	-	(5)	Complementary power supply	
20	14	10	10	PA4	I/O	TTa	-	SPI1_NSS, USART1_CK(2) USART2_CK(3)(5), TIM14_CH1, USART6_TX(5)	ADC_IN4
21	15	11	11	PA5	I/O	TTa	-	SPI1_SCK, USART6_RX(5)	ADC_IN5

Table 11. STM32F030x4/6/8/C pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
22	16	12	12	PA6	I/O	TTa	-	SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT USART3_CTS(5)	ADC_IN6
23	17	13	13	PA7	I/O	TTa	-	SPI1_MOSI, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT	ADC_IN7
24	-	-	-	PC4	I/O	TTa	-	EVENTOUT, USART3_TX(5)	ADC_IN14
25	-	-	-	PC5	I/O	TTa	-	USART3_RX(5)	ADC_IN15, WKUP5(5)
26	18	14	-	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, EVENTOUT, USART3_CK(5)	ADC_IN8
27	19	15	14	PB1	I/O	TTa	-	TIM3_CH4, TIM14_CH1, TIM1_CH3N, USART3_RTS(5)	ADC_IN9
28	20	-	-	PB2	I/O	FT	(6)	-	-
29	21	-	-	PB10	I/O	FT	-	SPI2_SCK(5), I2C1_SCL(2), I2C2_SCL(3)(5), USART3_TX(5)	-
30	22	-	-	PB11	I/O	FT	-	I2C1_SDA(2), I2C2_SDA(3)(5), EVENTOUT, USART3_RX(5)	-
31	23	16	-	VSS	S	-	-	Ground	
32	24	17	16	VDD	S	-	-	Digital power supply	
33	25	-	-	PB12	I/O	FT	-	SPI1_NSS(2), SPI2_NSS(3)(5), TIM1_BKIN, EVENTOUT, USART3_CK(5)	-

Table 11. STM32F030x4/6/8/C pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
34	26	-	-	PB13	I/O	FT	-	SPI1_SCK(2), SPI2_SCK(3)(5), I2C2_SCL(5), TIM1_CH1N, USART3_CTS(5)	-
35	27	-	-	PB14	I/O	FT	-	SPI1_MISO(2), SPI2_MISO(3)(5), I2C2_SDA(5), TIM1_CH2N, TIM15_CH1(3)(5), USART3_RTS(5)	-
36	28	-	-	PB15	I/O	FT	-	SPI1_MOSI(2), SPI2_MOSI(3)(5), TIM1_CH3N, TIM15_CH1N(3)(5), TIM15_CH2(3)(5)	RTC_REFIN, WKUP7(5)
37	-	-	-	PC6	I/O	FT	-	TIM3_CH1	-
38	-	-	-	PC7	I/O	FT	-	TIM3_CH2	-
39	-	-	-	PC8	I/O	FT	-	TIM3_CH3	-
40	-	-	-	PC9	I/O	FT	-	TIM3_CH4	-
41	29	18	-	PA8	I/O	FT	-	USART1_CK, TIM1_CH1, EVENTOUT, MCO	-
42	30	19	17	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, TIM15_BKIN(3)(5) I2C1_SCL(2)(5)	-
43	31	20	18	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, TIM17_BKIN I2C1_SDA(2)(5)	-
44	32	21	-	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, EVENTOUT, I2C2_SCL(5)	-
45	33	22	-	PA12	I/O	FT	-	USART1_RTS, TIM1_ETR, EVENTOUT, I2C2_SDA(5)	-

Table 11. STM32F030x4/6/8/C pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
46	34	23	19	PA13 (SWDIO)	I/O	FT	(7)	IR_OUT, SWDIO	-
47(4)	35(4)	-	-	PF6	I/O	FT	(4)	I2C1_SCL(2), I2C2_SCL(3)	-
47(5)	35(5)	-	-	VSS	S	-	(5)	Ground	
48(4)	36(4)	-	-	PF7	I/O	FT	(4)	I2C1_SDA(2), I2C2_SDA(3)	-
48(5)	36(5)	-	-	VDD	S	-	(5)	Complementary power supply	
49	37	24	20	PA14 (SWCLK)	I/O	FT	(7)	USART1_TX(2), USART2_TX(3)(5), SWCLK	-
50	38	25	-	PA15	I/O	FT	-	SPI1_NSS, USART1_RX(2), USART2_RX(3)(5), USART4_RTS(5), EVENTOUT	-
51	-	-	-	PC10	I/O	FT	-	USART3_TX(5), USART4_TX(5)	-
52	-	-	-	PC11	I/O	FT	-	USART3_RX(5), USART4_RX(5)	-
53	-	-	-	PC12	I/O	FT	-	USART3_CK(5), USART4_CK(5), USART5_TX(5)	-
54	-	-	-	PD2	I/O	FT	-	TIM3_ETR, USART3_RTS(5), USART5_RX(5)	-
55	39	26	-	PB3	I/O	FT	-	SPI1_SCK, EVENTOUT, USART5_TX(5)	-
56	40	27	-	PB4	I/O	FT	-	SPI1_MISO, TIM3_CH1, EVENTOUT, TIM17_BKIN(5), USART5_RX(5)	-
57	41	28	-	PB5	I/O	FT	-	SPI1_MOSI, I2C1_SMBA, TIM16_BKIN, TIM3_CH2, USART5_CK_RTS(5)	WKUP6(5)

Table 11. STM32F030x4/6/8/C pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
58	42	29	-	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N	-
59	43	30	-	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N, USART4_CTS(5)	-
60	44	31	1	BOOT0	I	B	-	Boot memory selection	
61	45	-	-	PB8	I/O	FTf	(6)	I2C1_SCL, TIM16_CH1	-
62	46	-	-	PB9	I/O	FTf	-	I2C1_SDA, IR_OUT, SPI2_NSS(5), TIM17_CH1, EVENTOUT	-
63	47	32	15	VSS	S	-	-	Ground	
64	48	1	16	VDD	S	-	-	Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. This feature is available on STM32F030x6 and STM32F030x4 devices only.
3. This feature is available on STM32F030x8 devices only.
4. For STM32F030x4/6/8 devices only.
5. For STM32F030xC devices only.
6. On LQFP32 package, PB2 and PB8 should be treated as unconnected pins (even when they are not available on the package, they are not forced to a defined level by hardware).
7. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on SWDIO pin and internal pull-down on SWCLK pin are activated.

Table 12. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA0	-	USART1_CTS(2) / USART2_CTS(1)(3)	-	-	USART4_TX(1)	-	-
PA1	EVENTOUT	USART1_RTS(2) / USART2_RTS(1)(3)	-	-	USART4_RX(1)	TIM15_CH1N(1)	-
PA2	TIM15_CH1(1)(3)	USART1_TX(2) / USART2_TX(1)(3)	-	-	-	-	-
PA3	TIM15_CH2(1)(3)	USART1_RX(2) / USART2_RX(1)(3)	-	-	-	-	-
PA4	SPI1_NSS	USART1_CK(2) / USART2_CK(1)(3)	-	-	TIM14_CH1	USART6_TX(1)	-
PA5	SPI1_SCK	-	-	-	-	USART6_RX(1)	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	USART3_CTS(1)	TIM16_CH1	EVENTOUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	-
PA9	TIM15_BKIN(1)(3)	USART1_TX	TIM1_CH2	-	I2C1_SCL(1)(2)	MCO(1)	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	I2C1_SDA(1)(2)	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	-	SCL	-

Table 12. Alternate functions selected through GPIOA_AFR registers for port A (continued)

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	-	-	SDA	-
PA13	SWDIO	IR_OUT	-	-	-	-	-
PA14	SWCLK	USART1_TX(2)	-	-	-	-	-
		USART2_TX(1)(3)					
PA15	SPI1_NSS	USART1_RX(2)	-	EVENTOUT	USART4_RTS(1)	-	-
		USART2_RX(1)(3)					

1. This feature is available on STM32F030xC devices.
2. This feature is available on STM32F030x4 and STM32F030x6 devices.
3. This feature is available on STM32F030x8 devices.

Table 13. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-	USART3_CK(1)	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	USART3_RTS(1)	-
PB2	-	-	-	-	-	-
PB3	SPI1_SCK	EVENTOUT	-	-	USART5_TX(1)	-
PB4	SPI1_MISO	TIM3_CH1	EVENTOUT	-	USART5_RX(1)	TIM17_BKIN(1)
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	USART5_CK_RTS(1)	-
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	-	-	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	-	USART4_CTS(1)	-

Table 13. Alternate functions selected through GPIOB_AFR registers for port B (continued)

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB8	-	I2C1_SCL	TIM16_CH1	-	-	-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	-	SPI2_NSS(1)
PB10	-	I2C1_SCL(2) / I2C2_SCL(1)(3)	-	-	USART3_TX(1)	SPI2_SCK(1)
PB11	EVENTOUT	I2C1_SDA(2) / I2C2_SDA(1)(3)	-	-	USART3_RX(1)	-
PB12	SPI1_NSS(2) / SPI2_NSS(1)(3)	EVENTOUT	TIM1_BKIN	-	USART3_RTS(1)	TIM15(1)
PB13	SPI1_SCK(2) / SPI2_SCK(1)(3)	-	TIM1_CH1N	-	USART3_CTS(1)	I2C2_SCL(1)
PB14	SPI1_MISO(2) / SPI2_MISO(1)(3)	TIM15_CH1(1)(3)	TIM1_CH2N	-	USART3_RTS(1)	I2C2_SDA(1)
PB15	SPI1_MOSI(2) / SPI2_MOSI(1)(3)	TIM15_CH2(1)(3)	TIM1_CH3N	TIM15_CH1N(1)(3)	-	-

1. This feature is available on STM32F030xC devices.
2. This feature is available on STM32F030x4 and STM32F030x6 devices.
3. This feature is available on STM32F030x8 devices.

Table 14. Alternate functions selected through GPIOC_AFR(1) registers for port C

Pin name	AF0(2)	AF1(1)	AF2(1)
PC0	EVENTOUT	-	USART6_TX
PC1	EVENTOUT	-	USART6_RX
PC2	EVENTOUT	SPI2_MISO	-
PC3	EVENTOUT	SPI2_MOSI	-
PC4	EVENTOUT	USART3_TX	-
PC5	-	USART3_RX	-
PC6	TIM3_CH1	-	-
PC7	TIM3_CH2	-	-
PC8	TIM3_CH3	-	-
PC9	TIM3_CH4	-	-
PC10	USART4_TX(1)	USART3_TX	-
PC11	USART4_RX(1)	USART3_RX	-
PC12	USART4_CK(1)	USART3_CK	USART5_TX
PC13	-	-	-
PC14	-	-	-
PC15	-	-	-

1. Available on STM32F030xC devices only.
2. Default alternate functions for STM32F030x4/x6/x8 devices (they do not have the GPIOC_AFR registers).

Table 15. Alternate functions selected through GPIOD_AFR(1) registers for port D

Pin name	AF0(2)	AF1(1)	AF2(1)
PD2	TIM3_ETR	USART3_RTS	USART5_RX

1. Available on STM32F030xC devices only.
2. Default alternate functions for STM32F030x4/x6/x8 devices (they do not have the GPIOD_AFR registers).

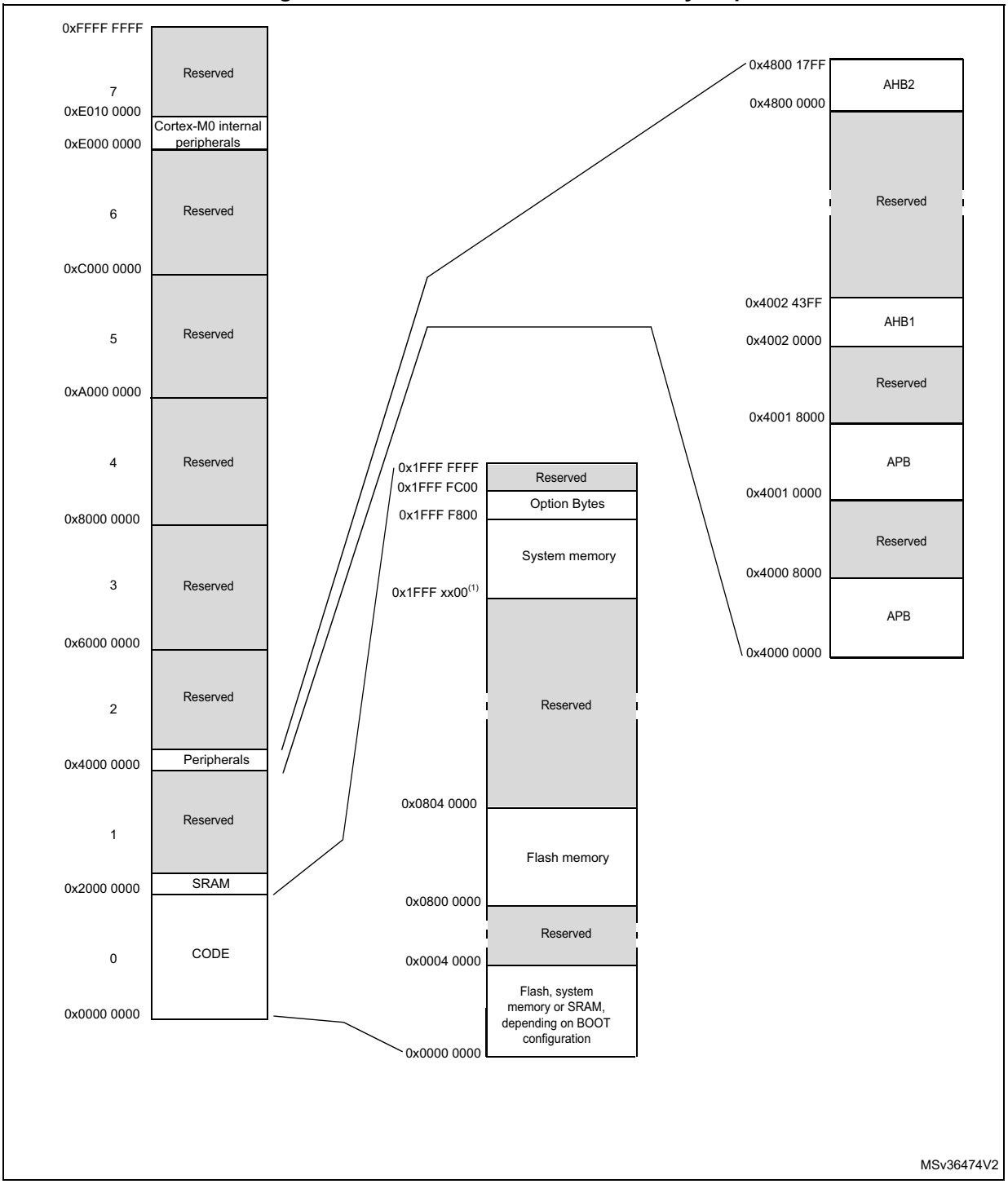
Table 16. Alternate functions selected through GPIOF_AFR(1) registers for port F

Pin name	AF0(2)	AF1(1)
PF0	-	I2C1_SDA
PF1	-	I2C1_SCL
PF4	EVENTOUT(1)	
PF5	EVENTOUT(1)	
PF6	I2C1_SCL(3), I2C2_SCL(4)	
PF7	I2C1_SDA(3), I2C2_SDA(4)	

1. Available on STM32F030xC devices only.
2. Default alternate functions for STM32F030x4/x6/x8 devices (they do not have the GPIOF_AFR registers).
3. Applies to STM32F030x4/x6
4. Applies to STM32F030x8

5 Memory mapping

Figure 10. STM32F030x4/x6/x8/xC memory map



1. The start address of the system memory is 0x1FFF EC00 for STM32F030x4, STM32F030x6 and STM32F030x8 devices, and 0x1FFF D800 for STM32F030xC devices.

Table 17. STM32F030x4/x6/x8/xC peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
-	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 3400 - 0x4002 43FF	4 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
-	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15(1)
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 1800 - 0x4001 23FF	3 KB	Reserved
	0x4001 1400 - 0x4001 17FF	1 KB	USART6(2)
	0x4001 0800 - 0x4001 13FF	3 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG

Table 17. STM32F030x4/x6/x8/xC peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
-	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved
APB	0x4000 7400 - 0x4000 7FFF	3 KB	Reserved
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 5C00 - 0x4000 6FFF	5 KB	Reserved
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2(1)
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	USART5(2)
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4(2)
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3(2)
	0x4000 4400 - 0x4000 47FF	1 KB	USART2(1)
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2(1)
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	2 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7(2)
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6(1)
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	Reserved

1. This feature is available on STM32F030x8 and STM32F030xC devices only. For STM32F030x6 and STM32F060x4, the area is Reserved.
2. This feature is available on STM32F030xC devices only. This area is reserved for STM32F030x4/6/8 devices.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions

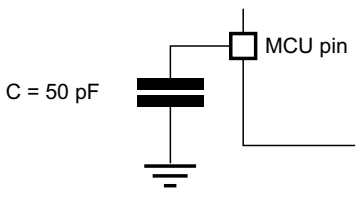
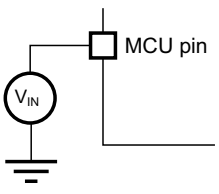
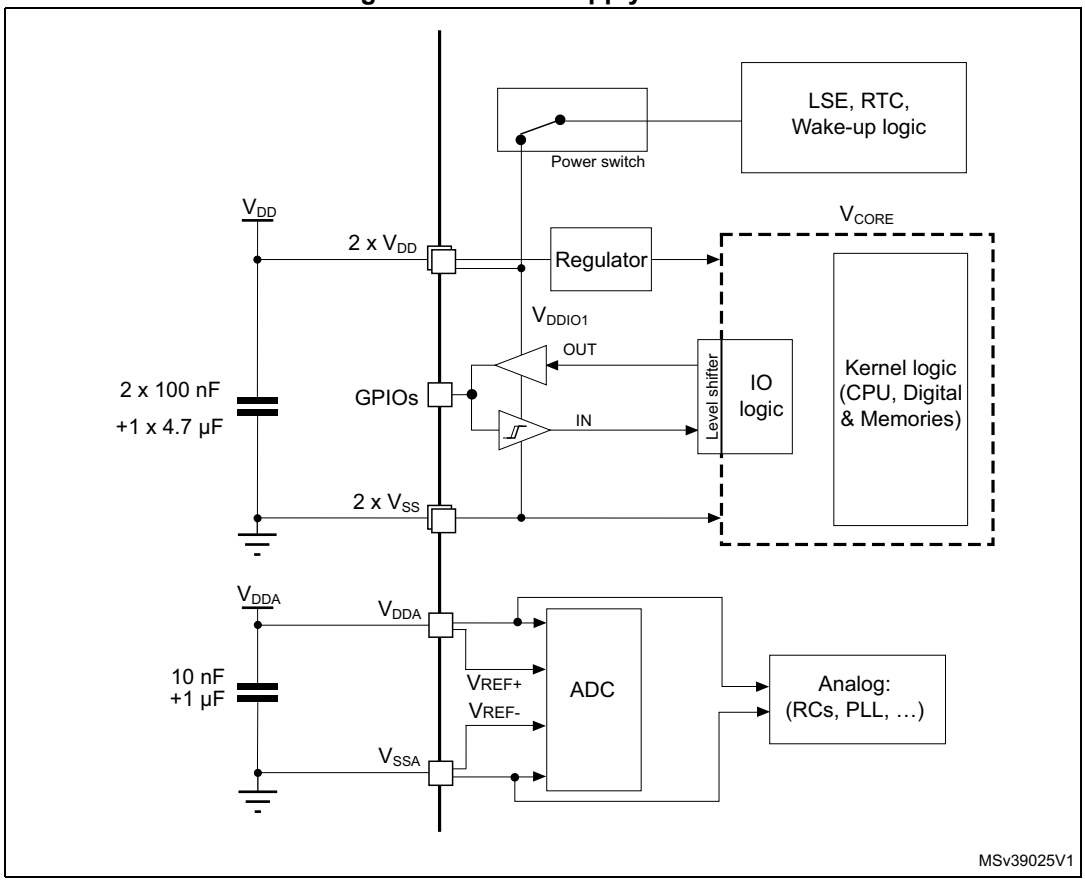


Figure 12. Pin input voltage



6.1.6 Power supply scheme

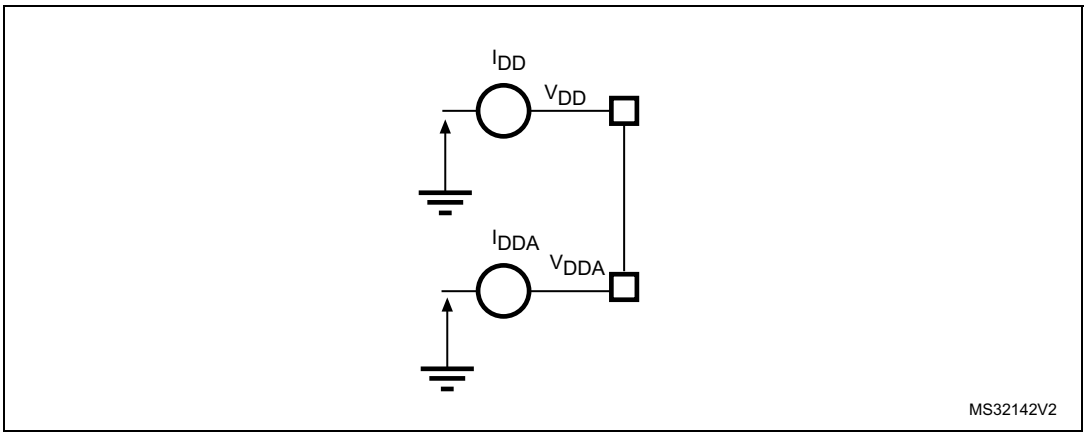
Figure 13. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18: Voltage characteristics*, *Table 19: Current characteristics* and *Table 20: Thermal characteristics* may cause permanent damage to the device. These are stress *ratings* only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 18. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage	-0.3	4.0	V
V_{DDA}–V_{SS}	External analog supply voltage	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} – 0.3	V_{DDIOx} + 4.0 (3)	V
	Input voltage on TTa pins	V_{SS} – 0.3	4.0	V
	BOOT0	0	V_{DDIOx} + 4.0 (3)	V
	Input voltage on any other pin	V_{SS} – 0.3	4.0	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 19: Current characteristics* for the maximum allowed injected current values.
3. V_{DDIOx} is internally connected with VDD pin.

Table 19. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$I_{INJ(PIN)}$(3)	Injected current on FT and FTf pins	-5/+0(4)	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 18: Voltage characteristics* for the maximum allowed input voltage values.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device. See note (2) below *Table 52: ADC accuracy*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	2.4	3.6	V

Table 21. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	Analog operating voltage	Must have a potential equal to or higher than V_{DD}	2.4	3.6	V
V_{IN}	I/O input voltage	TC and RST I/O	-0.3	V_{DDIOx}+0.3	V
		TTa I/O	-0.3	V_{DDA}+0.3(2)	
		FT and FTf I/O	-0.3	5.5(2)	
		BOOT0	0	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 (1)	LQFP64	-	455	mW
		LQFP48	-	364	
		LQFP32	-	357	
		TSSOP20	-	263	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	°C
		Low power dissipation(2)	-40	105	
T_J	Junction temperature range	Suffix 6 version	-40	105	°C

1. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
2. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.5: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 22* are derived from tests performed under the ambient temperature condition summarized in *Table 21*.

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge(2)	1.80	1.88	1.96(3)	V
		Rising edge	1.84(3)	1.92	2.00	V

Table 23. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$ (4)	Reset temporization	-	1.50	2.50	4.50	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 24* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 24. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40°C < T_A < +85°C	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10(1)	µs
$t_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4 (1)	-	-	µs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3 V	-	-	10(1)	mV
T_{Coeff}	Temperature coefficient	-	-100(1)	-	100(1)	ppm/°C

1. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 25* to *Table 27* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 25. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V(1)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled		Unit
				Typ	Max @ T_A(2) 85 °C	
I_{DD}	Supply current in Run mode, code executing from Flash	HSI or HSE clock, PLL on	48 MHz	22.0	22.8	mA
			48 MHz	26.8	30.2	
			24 MHz	12.2	13.2	
			24 MHz	14.1	16.2	
		HSI or HSE clock, PLL off	8 MHz	4.4	5.2	
			8 MHz	4.9	5.6	
I_{DD}	Supply current in Run mode, code executing from RAM	HSI or HSE clock, PLL on	48 MHz	22.2	23.2	mA
			48 MHz	26.1	29.3	
			24 MHz	11.2	12.2	
			24 MHz	13.3	15.7	
		HSI or HSE clock, PLL off	8 MHz	4.0	4.5	
			8 MHz	4.6	5.2	
I_{DD}	Supply current in Sleep mode, code executing from Flash or RAM	HSI or HSE clock, PLL on	48 MHz	14	15.3	mA
			48 MHz	17.0	19.0	
			24 MHz	7.3	7.8	
			24 MHz	8.7	10.1	
		HSI or HSE clock, PLL off	8 MHz	2.6	2.9	
			8 MHz	3.0	3.5	

1. The gray shading is used to distinguish the values for STM32F030xC devices.
2. Data based on characterization results, not tested in production unless otherwise specified.

Table 26. Typical and maximum current consumption from the V_{DDA} supply(1)

Symbol	Parameter	Conditions(2)	f_{HCLK}	V_{DDA} = 3.6 V		Unit
				Typ	Max @ T_A(3)	
					85 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSE bypass, PLL on	48 MHz	175	215	µA
			48 MHz	160	192	
		HSE bypass, PLL off	8 MHz	3.9	4.9	
			8 MHz	3.7	4.6	
			1 MHz	3.9	4.1	
			1 MHz	3.3	4.4	
		HSI clock, PLL on	48 MHz	244	275	
			48 MHz	235	275	
		HSI clock, PLL off	8 MHz	85	105	
			8 MHz	77	92	

1. The gray shading is used to distinguish the values for STM32F030xC devices.
2. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash or RAM. Furthermore, when the PLL is off, I_{DDA} is independent of the frequency.
3. Data based on characterization results, not tested in production.