SN74CBTLV3253 Low-Voltage Dual 1-of-4 FET Multiplexer/Demultiplexer

1 Features

- Functionally Equivalent to QS3253
- 5Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100mA Per JESD 78, Class II

2 Applications

- Datacenter and enterprise computing
- Broadband fixed line access
- Building automation
- Wired networking
- Motor drives
- Video Broadcasting: IP-Based Multi-Format Transcoders
- Video Communications Systems

3 Description

The SN74CBTLV3253 device is a dual 1-of-4 high-speed FET multiplexer and demultiplexer. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

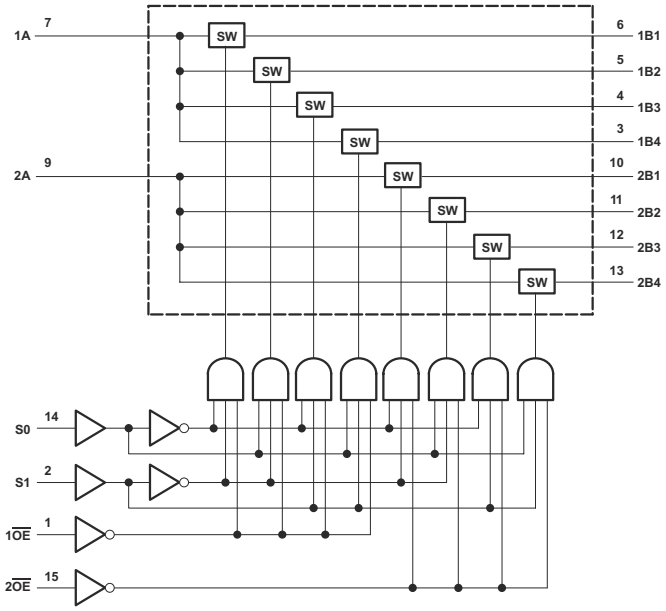
The select (S0, S1) inputs control the data flow. The FET multiplexers/demultiplexers are disabled when the associated output-enable ($\overline{OE}$) input is high.

The SN74CBTLV3253 device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current cannot backflow through the device when it is powered down. The device has isolation during power off.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE
SN74CBTLV3253D	SOIC (16)	9.90mm × 3.90mm
SN74CBTLV3253DBQ	SSOP (16)	4.90mm × 3.90mm
SN74CBTLV3253DGV	TVSOP (16)	3.60mm × 4.40mm
SN74CBTLV3253RGY	VQFN (16)	4.00mm × 3.50mm
SN74CBTLV3253PW	TSSOP (16)	5.00mm × 4.40mm
SN74CBTLV3253DYY	SOT (16)	4.20mm × 2.00mm
SN74CBTLV3253BQB	WQFN (16)	3.50mm × 2.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

Table of Contents

4 Pin Configuration and Functions

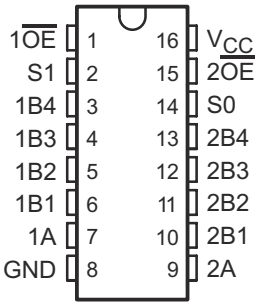


Figure 4-1. D, DBQ, DGV, PW or DYY Package 16-Pin SOIC, SSOP, TVSOP, TSSOP or SOT Top View

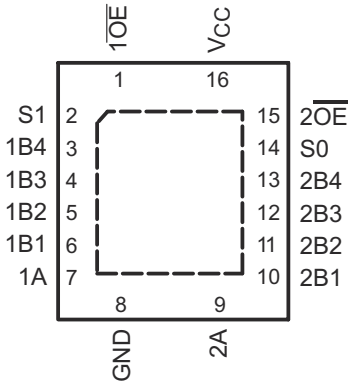


Figure 4-2. RGY or BQB Package 16-Pin VQFN Top View

Table 4-1. Pin Functions

PIN		Type	DESCRIPTION
NAME	NO.		
1 $\overline{OE}$	1	I	Output Enable 1 Active-Low
S1	2	I	Select Pin 1
1B4	3	I/O	Channel 1 I/O 4
1B3	4	I/O	Channel 1 I/O 3
1B2	5	I/O	Channel 1 I/O 2
1B1	6	I/O	Channel 1 I/O 1
1A	7	I/O	Channel 1 common
GND	8	—	Ground
2A	9	I/O	Channel 2 common
2B1	10	I/O	Channel 2 I/O 1
2B2	11	I/O	Channel 2 I/O 2
2B3	12	I/O	Channel 2 I/O 3
2B4	13	I/O	Channel 2 I/O 4
S0	14	I	Select Pin 0
2 $\overline{OE}$	15	I	Output Enable 2 Active-Low
V_{CC}	16	—	Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_{IN}	Control input voltage(2)		–0.5	4.6	V
$V_{I/O}$	Switch I/O voltage(2)		–0.5	4.6	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
	Continuous current through V_{CC} or GND			±128	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	+2000	V
		Charged-Device Model (CDM), per JEDEC specification JESD22-C101, all pins(2)	+1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3V to 2.7V	1.7		V
		V_{CC} = 2.7V to 3.6V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3V to 2.7V		0.7	V
		V_{CC} = 2.7V to 3.6V		0.8	
T_A	Operating free-air temperature	PKG = RGY, DBQ, D, PW, DGV	–40	85	°C
T_A	Operating free-air temperature	PKG = BQB, DYY	-40	125	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the *Implications of Slow or Floating CMOS Inputs* application note.

5.4 Thermal Information

THERMAL METRIC[1]		SN74CBTLV3253							UNIT
		D (SOIC)	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	DYY (SOT)	BQB (WQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.5	116.6	123.1	129.1	78.4	129.9	88.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.4	70	48.7	67	52.5	78.4	58.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.2	75	54.9	87.1	21.74	73.3	17.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.5	17	5.2	14.5	52.5	17.2	58.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.6	74.1	54.3	86.3	76.6	72.4	85.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	37.3	n/a	37.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics - D, DBQ, DGV, PW and RGY only

over recommended operating free-air temperature range -40 to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IK}		V_{CC} = 3V,	I_I = –18mA				–1.2	V
I_I		V_{CC} = 3.6V,	V_I = V_{CC} or GND				±1	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6V				15	µA
I_{CC}		V_{CC} = 3.6V,	I_O = 0,	V_I = V_{CC} or GND			10	µA
ΔI_{CC} [2]	Control inputs	V_{CC} = 3.6V,	One input at 3V,	Other inputs at V_{CC} or GND			300	µA
C_i	Control inputs	V_I = 3V or 0				3		pF
$C_{io(OFF)}$	A port	V_O = 3V or 0,	$\overline{OE}$ = V_{CC}			20.5		pF
	B port					5.5		
r_{on} [3]		V_{CC} = 2.3V, TYP at V_{CC} = 2.5V	V_I = 0	I_I = 64mA		5	8	Ω
				I_I = 24mA		5	8	
			V_I = 1.7V,	I_I = 15mA		27	40	
		V_{CC} = 3V	V_I = 0	I_I = 64mA		5	7	
				I_I = 24mA		5	7	
			V_I = 2.4V,	I_I = 15mA		10	15	

(1) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(2) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
(3) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

5.6 Electrical Characteristics - DYY and BQB Package only

over recommended operating free-air temperature range -40 to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IK}		V_{CC} = 3V,	I_I = –18mA				-1.2	V
I_I		V_{CC} = 3.6V,	V_I = V_{CC} or GND				±1	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6V				20	µA
I_{CC}		V_{CC} = 3.6V,	I_O = 0,	V_I = V_{CC} or GND			10	µA
ΔI_{CC} [2]	Control inputs	V_{CC} = 3.6V,	One input at 3V,	Other inputs at V_{CC} or GND			300	µA
C_i	Control inputs	V_I = 3V or 0				3		pF
$C_{io(OFF)}$	A port	V_O = 3V or 0,	$\overline{OE}$ = V_{CC}			20.5		pF
	B port					5.5		
r_{on} [3]		V_{CC} = 2.3V, TYP at V_{CC} = 2.5V	V_I = 0	I_I = 64mA		5	10	Ω
				I_I = 24mA		5	10	
			V_I = 1.7V,	I_I = 15mA		27	40	
		V_{CC} = 3V	V_I = 0	I_I = 64mA		5	9	
				I_I = 24mA		5	9	
			V_I = 2.4V,	I_I = 15mA		10	20	

(1) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(2) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
(3) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

5.7 Switching Characteristics - D, DBQ, DGV, PW and RGY only

over recommended operating free-air temperature range -40 to 85°C (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B[1]	B or A		0.15		0.25	ns
	S	A or B	1	6.8	1	5.5	
t_{en}	S	A or B	1	4.3	1	4	ns
t_{dis}	S	A or B	1	5.1	1	5.5	ns
t_{en}	$\overline{OE}$	A or B	1	5	1	4.8	ns
t_{dis}	$\overline{OE}$	A or B	1	5.5	1	5.4	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

5.8 Switching Characteristics - DYY and BQB Package only

over recommended operating free-air temperature range -40 to 125°C (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B[1]	B or A		3.1		1.7	ns
	S	A or B	1	6.8	1	5.5	
t_{en}	S	A or B	1	6.8	1	6.8	ns
t_{dis}	S	A or B	1	7	1	7	ns
t_{en}	$\overline{OE}$	A or B	1	6.5	1	6	ns
t_{dis}	$\overline{OE}$	A or B	1	6.5	1	6	ns

5.9 Typical Characteristics

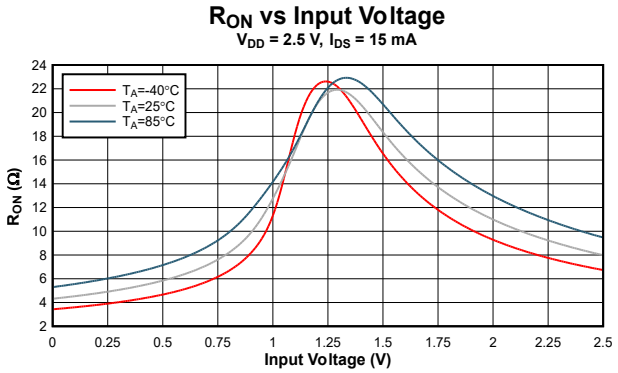


Figure 5-1. V_{DD} = 2.5V, I_{DS} = 15mA

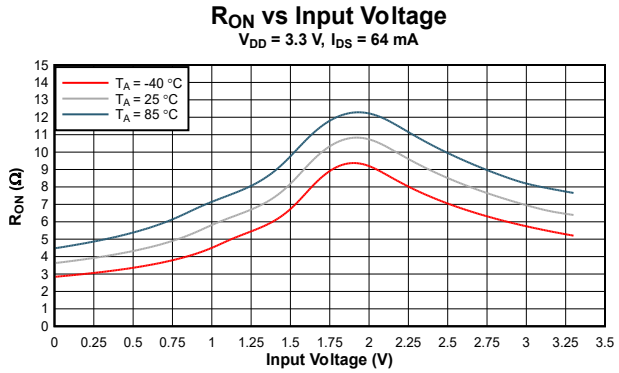


Figure 5-2. V_{DD} = 3.3V, I_{DS} = 64mA

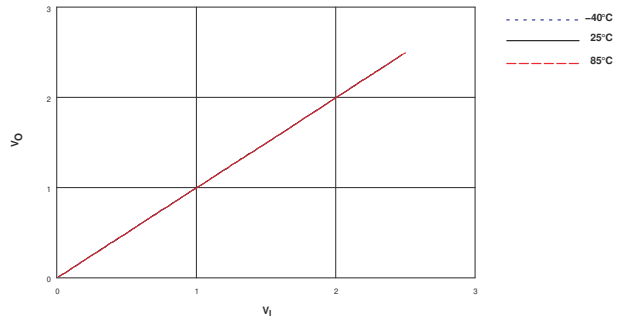
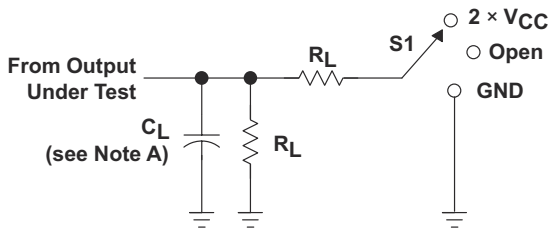


Figure 5-3. V_O vs V_I, V_{CC} = 2.5V

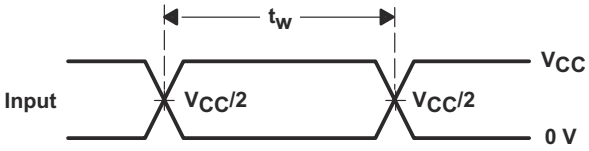
6 Parameter Measurement Information



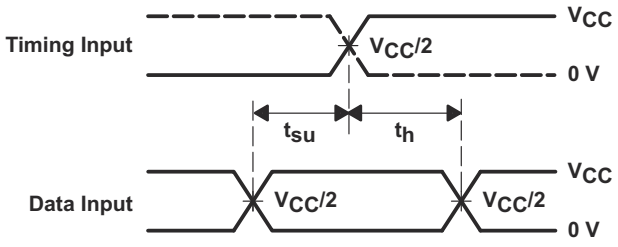
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

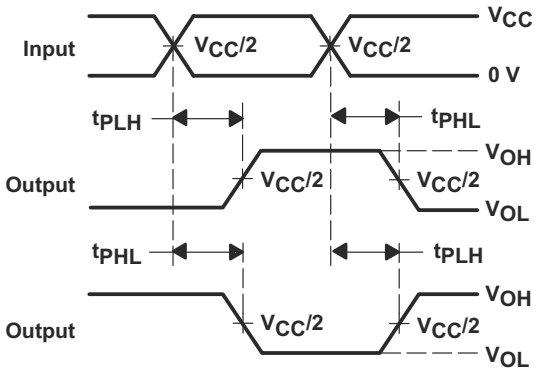
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V



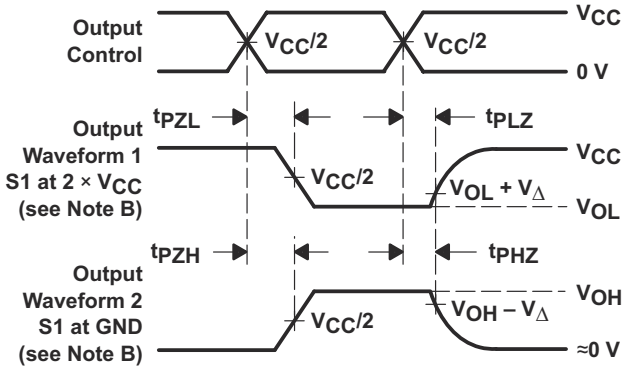
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

Figure 6-1. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

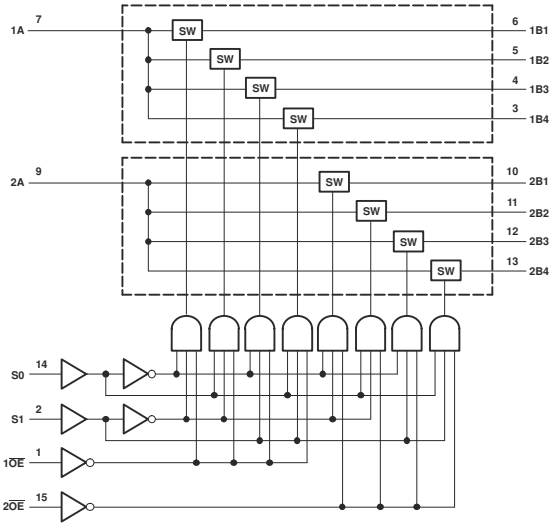
The SN74CBTLV3253 device is a dual 1-of-4 high-speed FET multiplexer/demultiplexer. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

The select (S0, S1) inputs control the data flow. The FET multiplexers and demultiplexers are disabled when the associated output-enable ($\overline{OE}$) input is high.

The SN74CBTLV3253 device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Feature Description

The SN74CBTLV3253 device is functionally equivalent to the QS3253 and has a 5Ω switch connection between two ports. The device also has rail-to-rail switching on data I/O ports as well as I_{off} supporting partial-power-down mode operation.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74CBTLV3253.

Table 7-1. Function Table (Each Multiplexer/Demultiplexer)

INPUTS			FUNCTION
$\overline{OE}$	S1	S0	
L	L	L	A port = B1 port
L	L	H	A port = B2 port
L	H	L	A port = B3 port
L	H	H	A port = B4 port
H	X	X	Disconnect

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74CBTLV3253 can be used to multiplex and demultiplex up to 2 channels simultaneously in a 4:1 configuration. The application shown here is a 2-bit bus being multiplexed between two devices. the $\overline{OE}$ and S pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations.

8.2 Typical Application

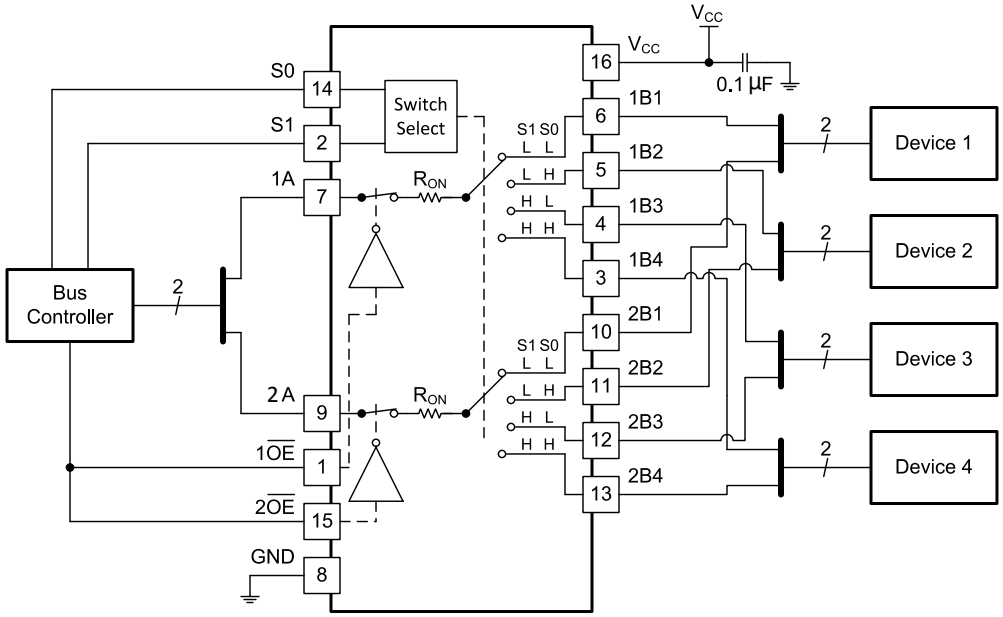


Figure 8-1. Typical Application of the SN74CBTLV3253

8.2.1 Design Requirements

The 0.1µF capacitor should be placed as close as possible to the device.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in Section 5.3.
   - Inputs and outputs are overvoltage tolerant slowing them to go as high as 4.6V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents must not exceed ±128mA per channel.
3. Frequency Selection Criterion:
   - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in Section 10.

8.2.3 Application Curve

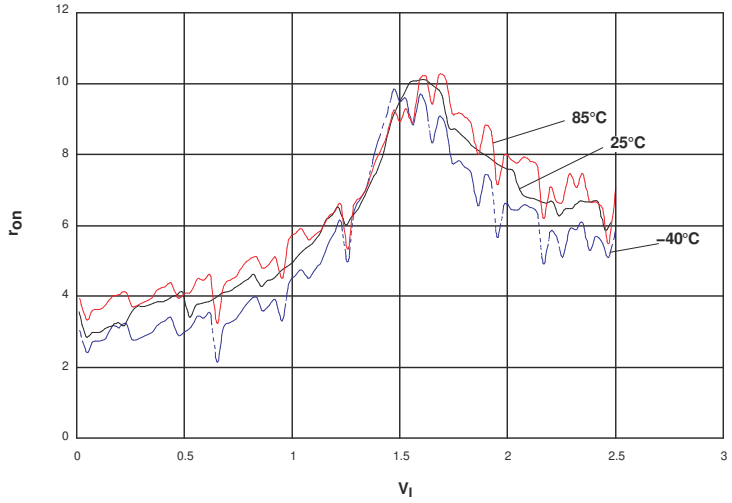


Figure 8-2. r_{on} vs V_I, V_{CC} = 2.5V

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the Section 5.3 table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

10 Layout

10.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 10-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

10.2 Layout Example

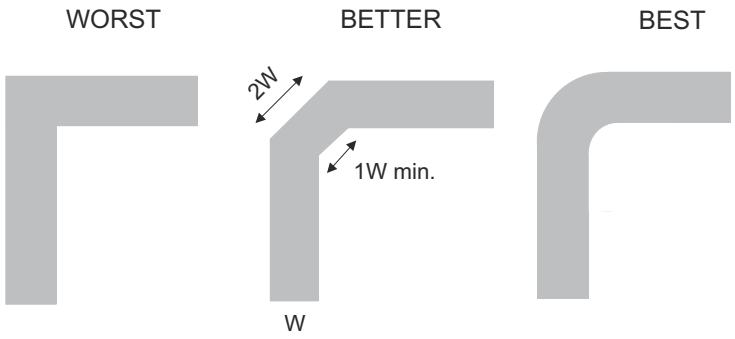


Figure 10-1. Trace Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- Texas Instruments, Implications of Slow or Floating CMOS Inputs

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (January 2018) to Revision K (July 2026)	Page
• Added New Packages with 125°C capability	4
• Updated Thermal ratings	5
• Added Electrical Specification section for new package	6
• Added Switching Specification section for new package	7
• Added Typical Curves	7

Changes from Revision I (February 2014) to Revision J (January 2018)	Page
• Changed the *Thermal Information* table	5

Changes from Revision H (February 2014) to Revision I (September 2015)	Page
• Added *Applications* section, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision G (February 2014) to Revision H (February 2014)	Page
• Updated data sheet – no specific changes	1

Changes from Revision F (July 2012) to Revision G (February 2014)	Page
• Deleted *Ordering Information* table	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74CBTLV3253DGVRG4	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
74CBTLV3253DGVRG4.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
74CBTLV3253RGYRG4	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
74CBTLV3253RGYRG4.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
74CBTLV3253RGYRG4.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253DBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253DBQR.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253DBQR.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253DGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253DGVR.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3253
SN74CBTLV3253DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3253
SN74CBTLV3253DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3253
SN74CBTLV3253DYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	CL253
SN74CBTLV3253PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL253
SN74CBTLV3253RGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253RGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253
SN74CBTLV3253RGYR.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL253

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

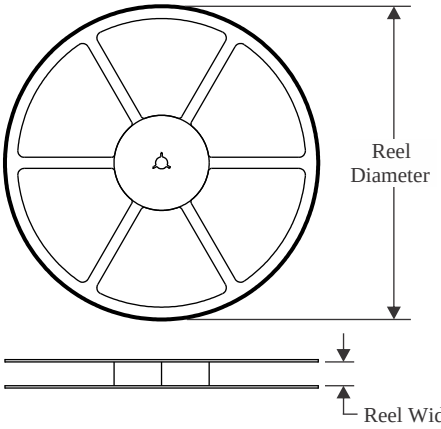
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

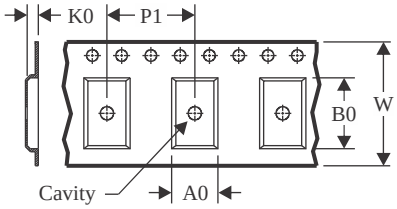
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

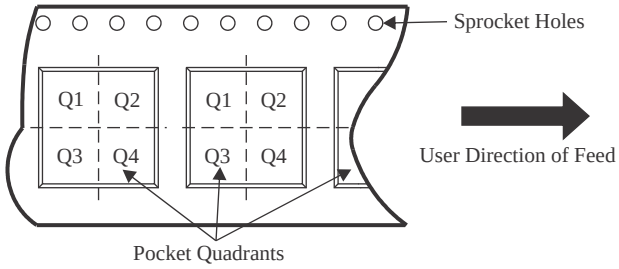


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

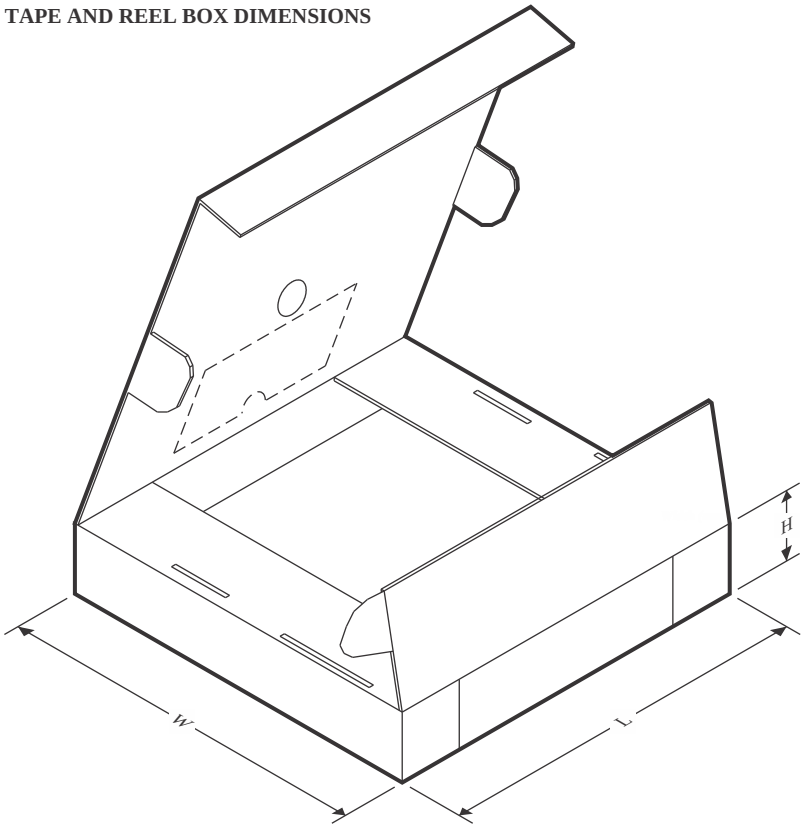
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBTLV3253DGVRG4	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
74CBTLV3253RGYRG4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74CBTLV3253BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74CBTLV3253DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBTLV3253DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CBTLV3253DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74CBTLV3253DYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.5	3.56	1.35	8.0	12.0	Q3
SN74CBTLV3253PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3253RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

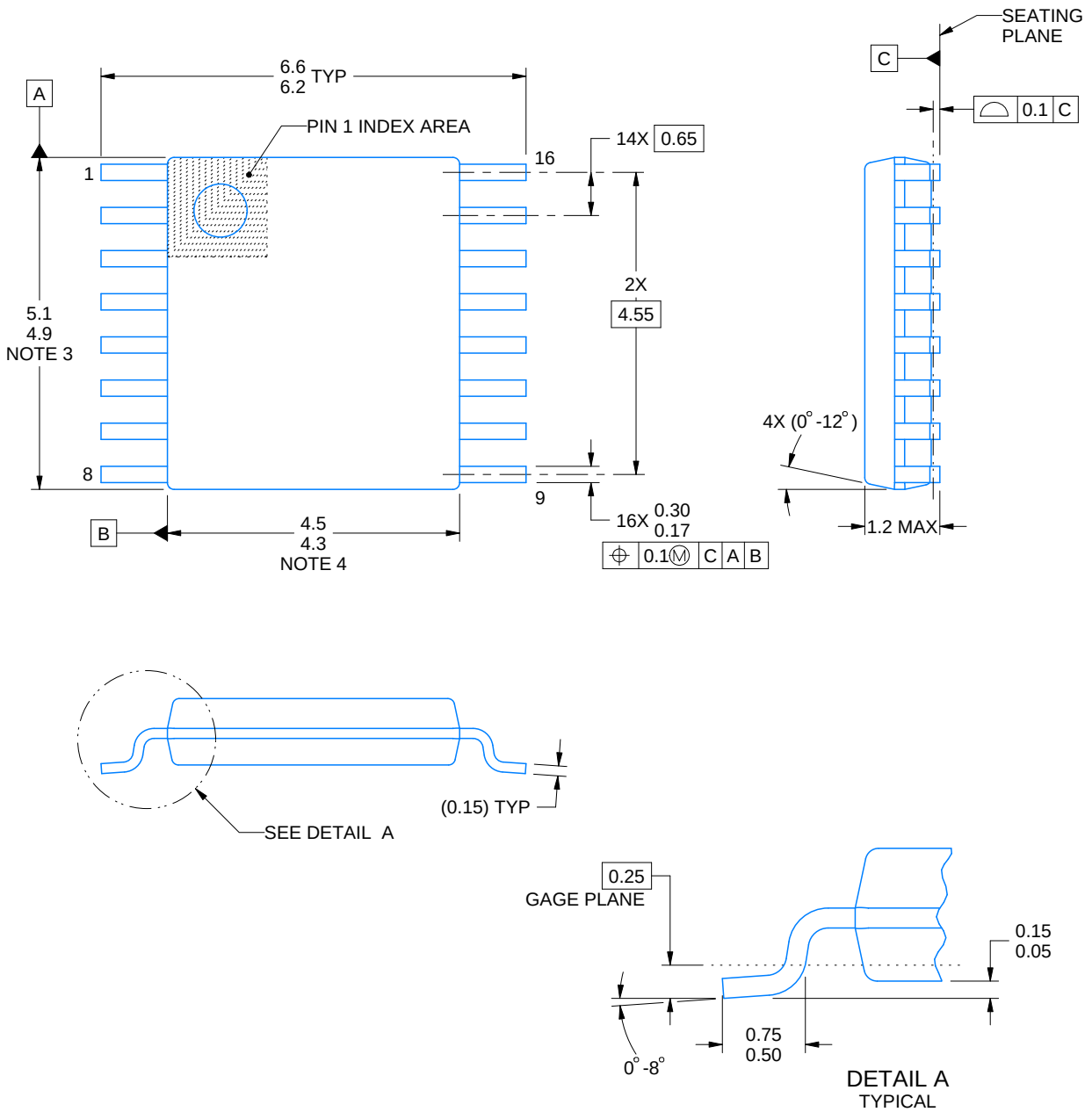
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CBTLV3253DGVRG4	TVSOP	DGV	16	2000	353.0	353.0	32.0
74CBTLV3253RGYRG4	VQFN	RGY	16	3000	353.0	353.0	32.0
SN74CBTLV3253BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74CBTLV3253DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
SN74CBTLV3253DGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74CBTLV3253DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74CBTLV3253DYYR	SOT-23-THIN	DYY	16	3000	360.0	360.0	36.0
SN74CBTLV3253PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74CBTLV3253RGYR	VQFN	RGY	16	3000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

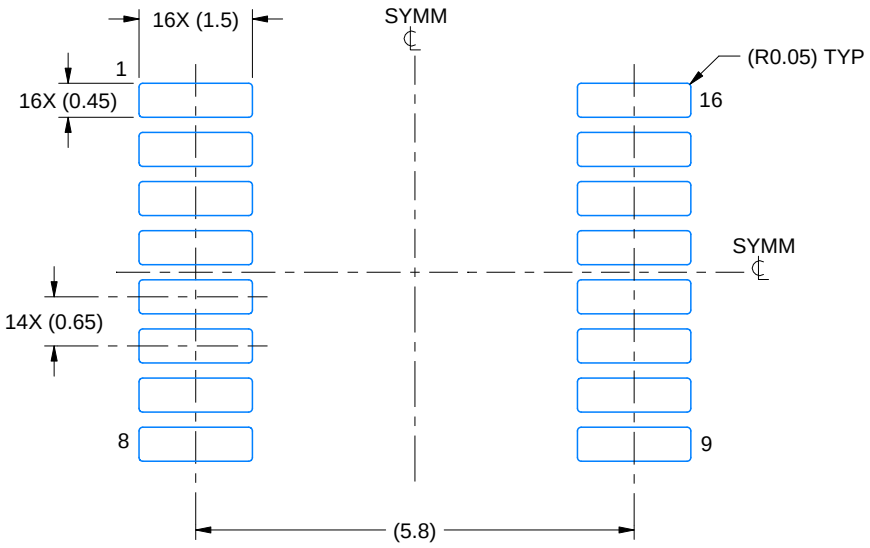
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



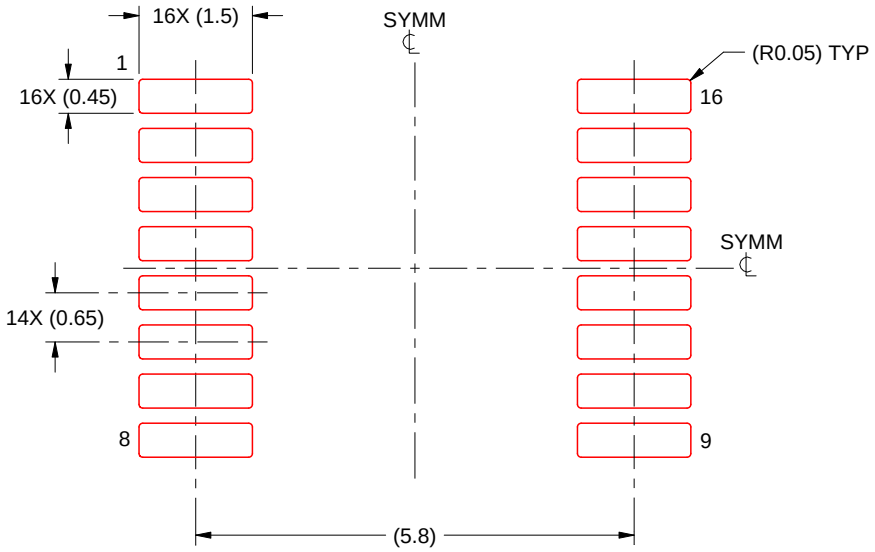
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

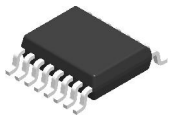


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

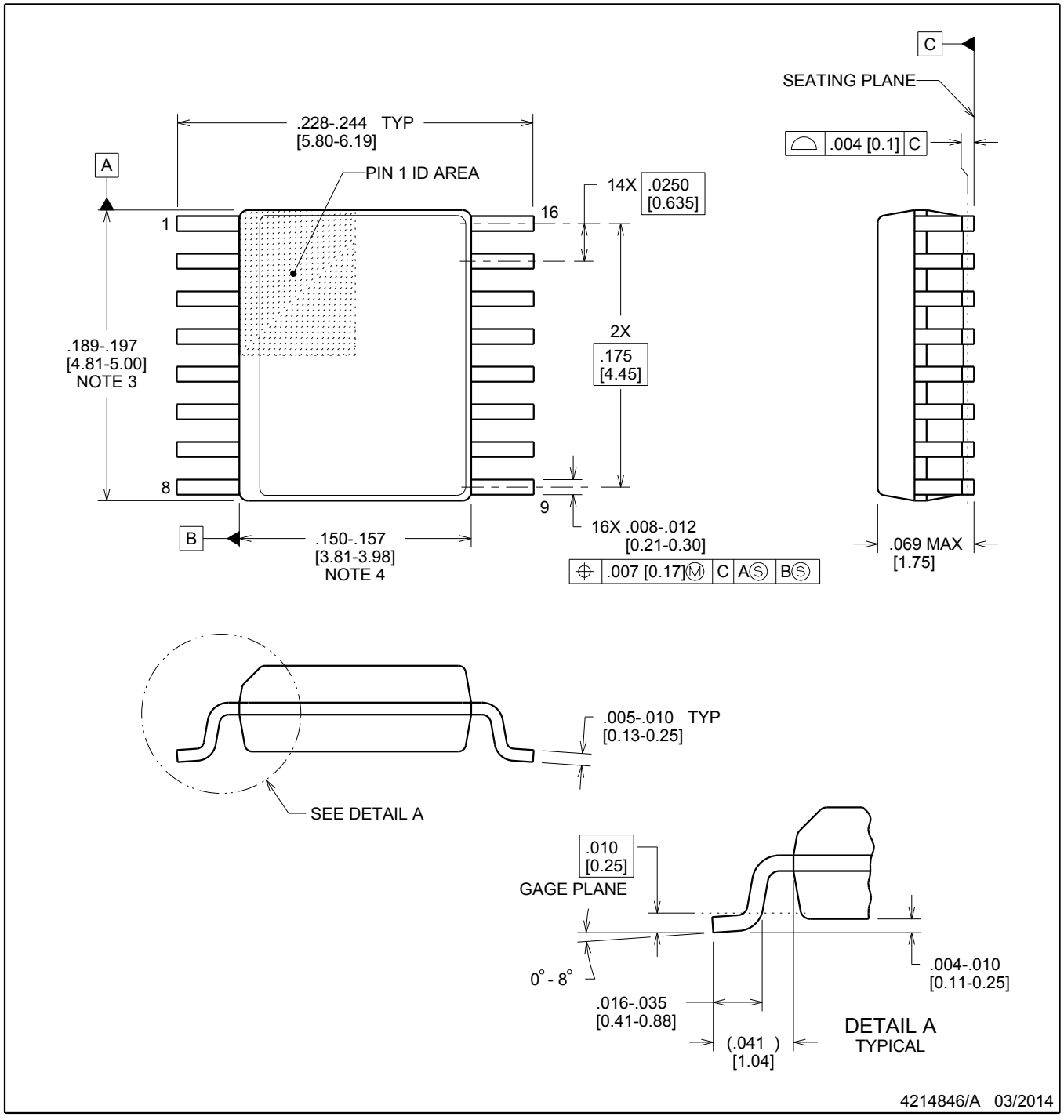


PACKAGE OUTLINE

DBQ0016A

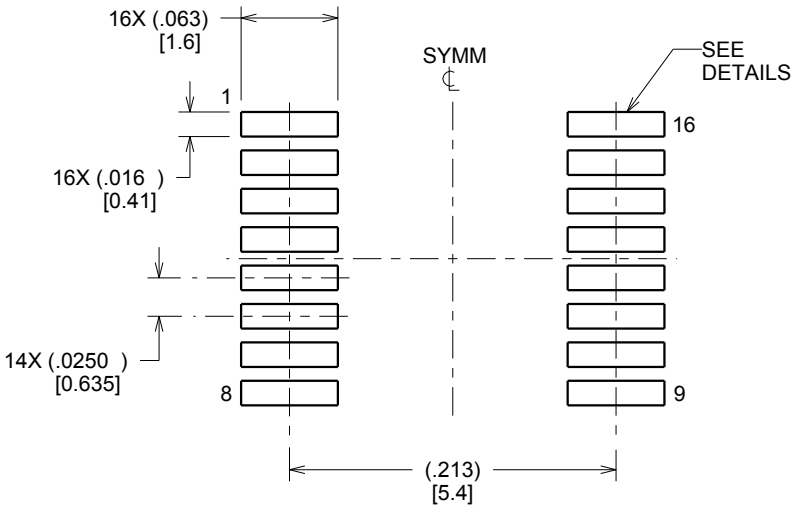
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

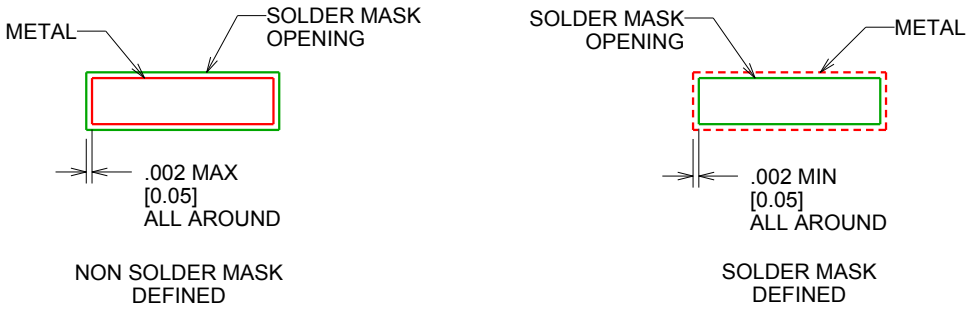


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

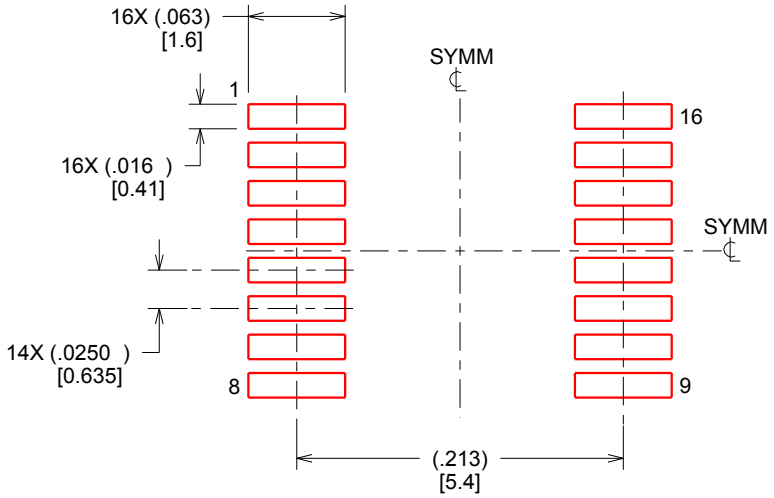
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



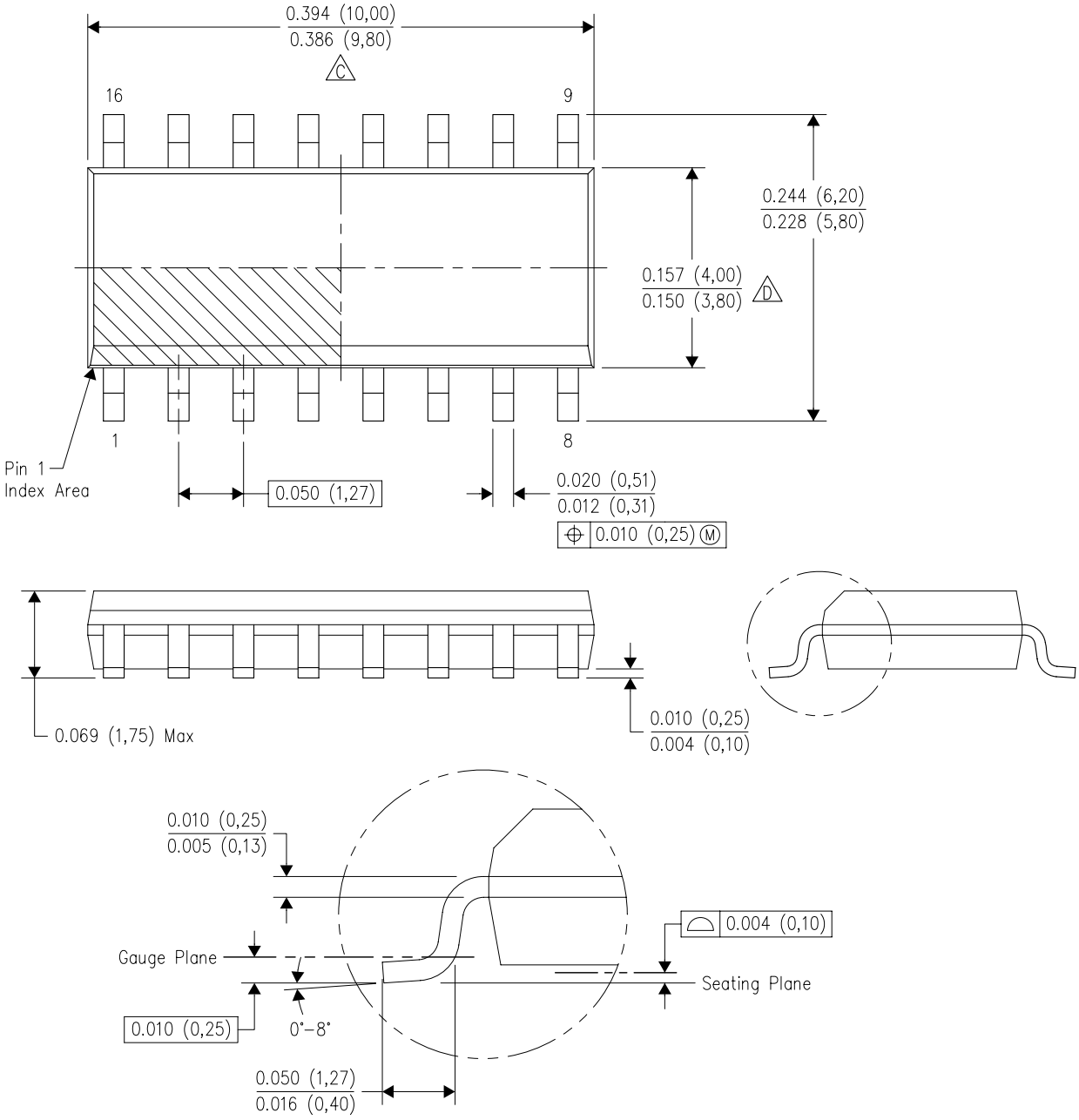
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

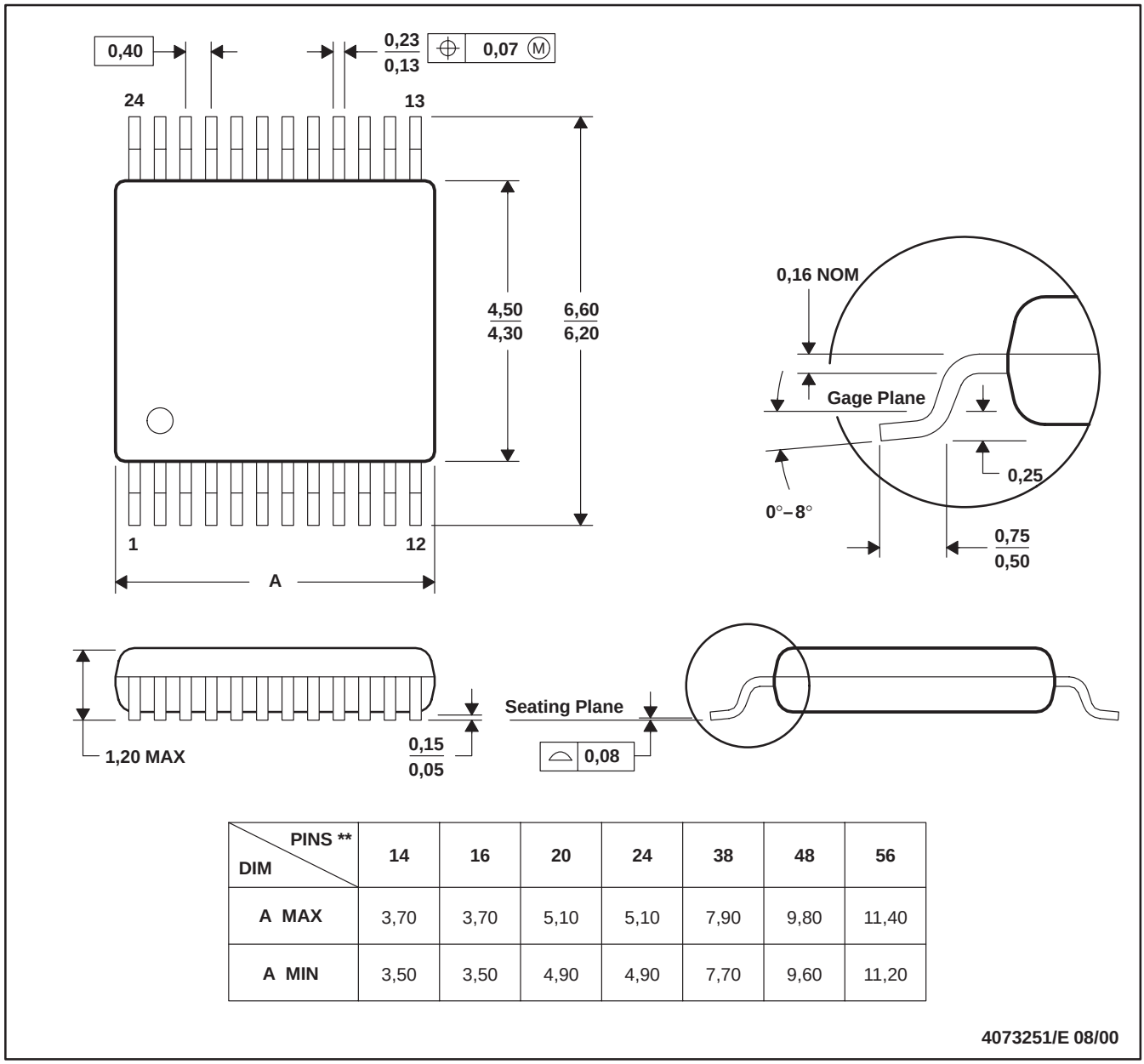
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

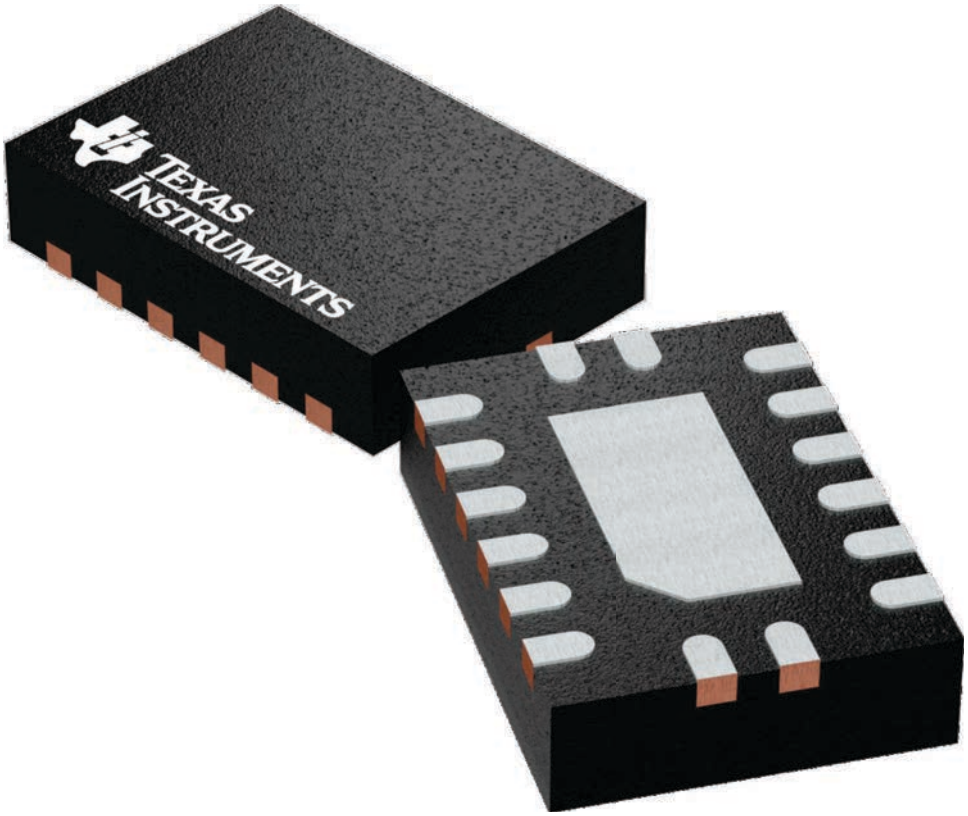
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



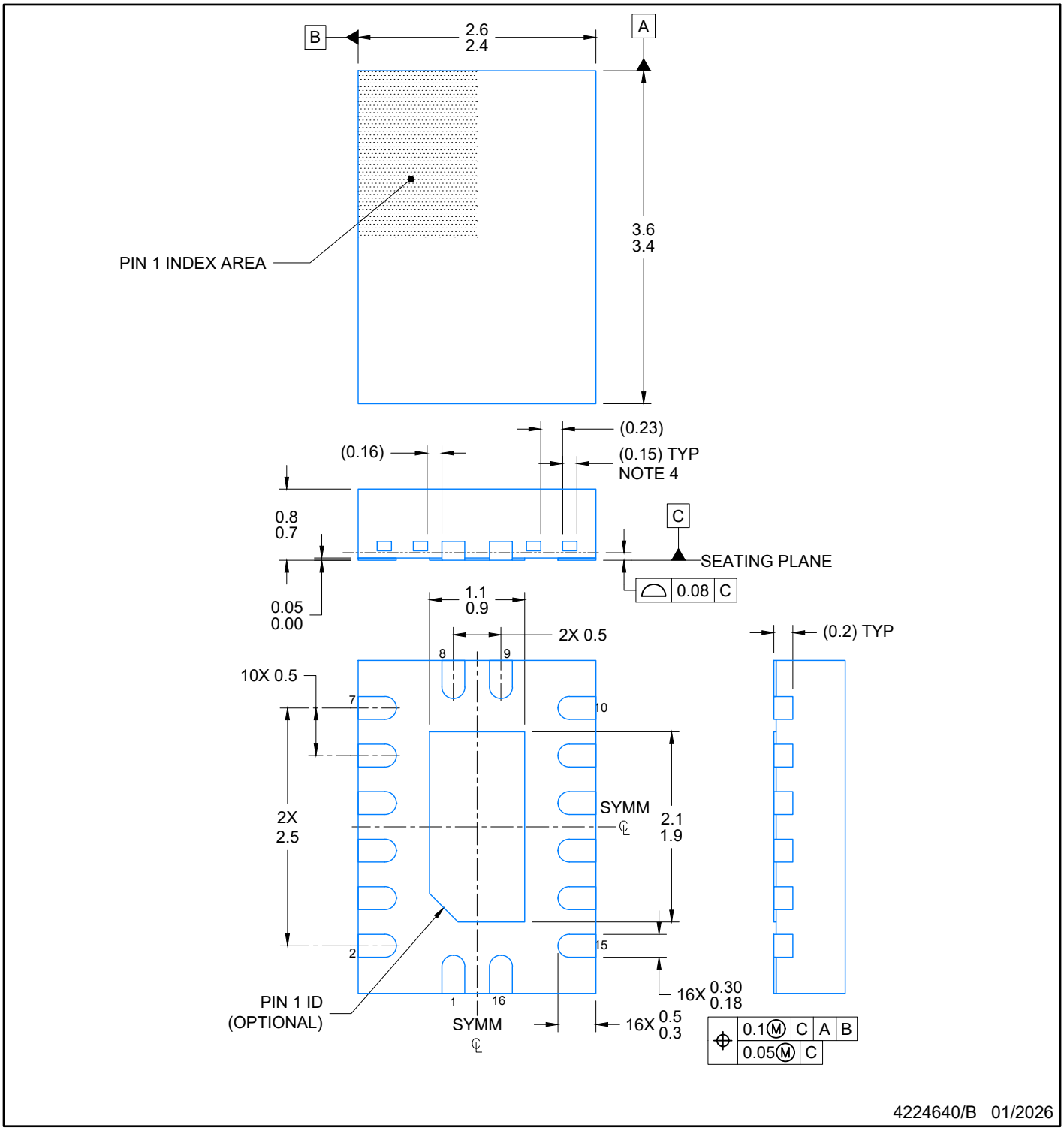
4226161/A

PACKAGE OUTLINE

BQB0016A

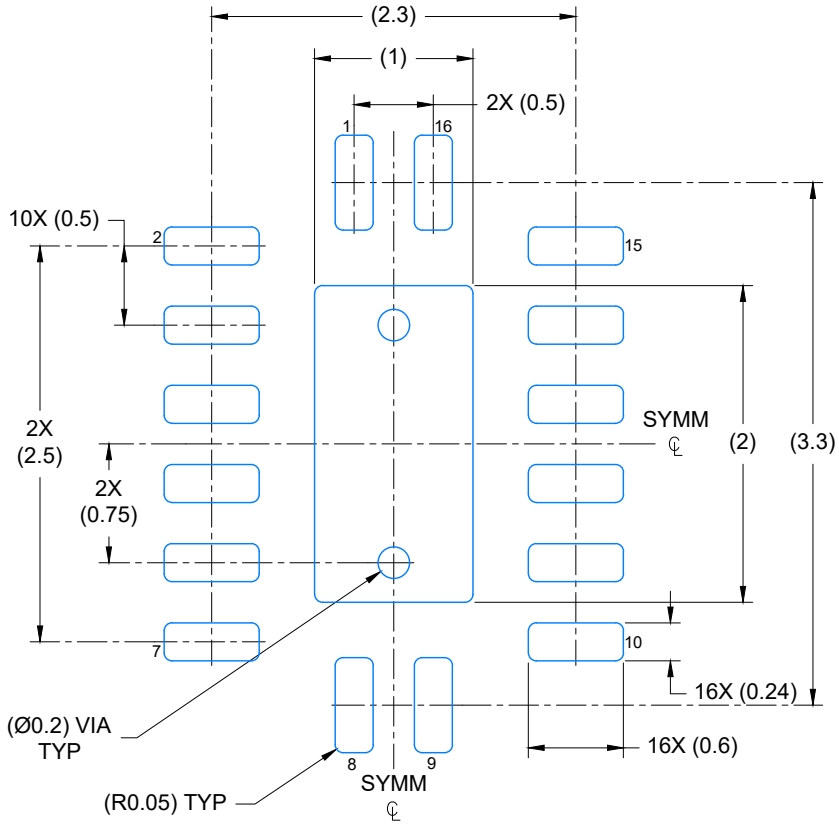
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

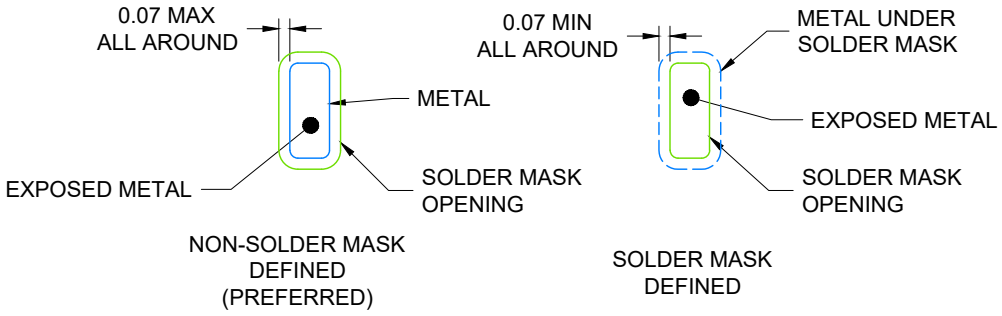


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

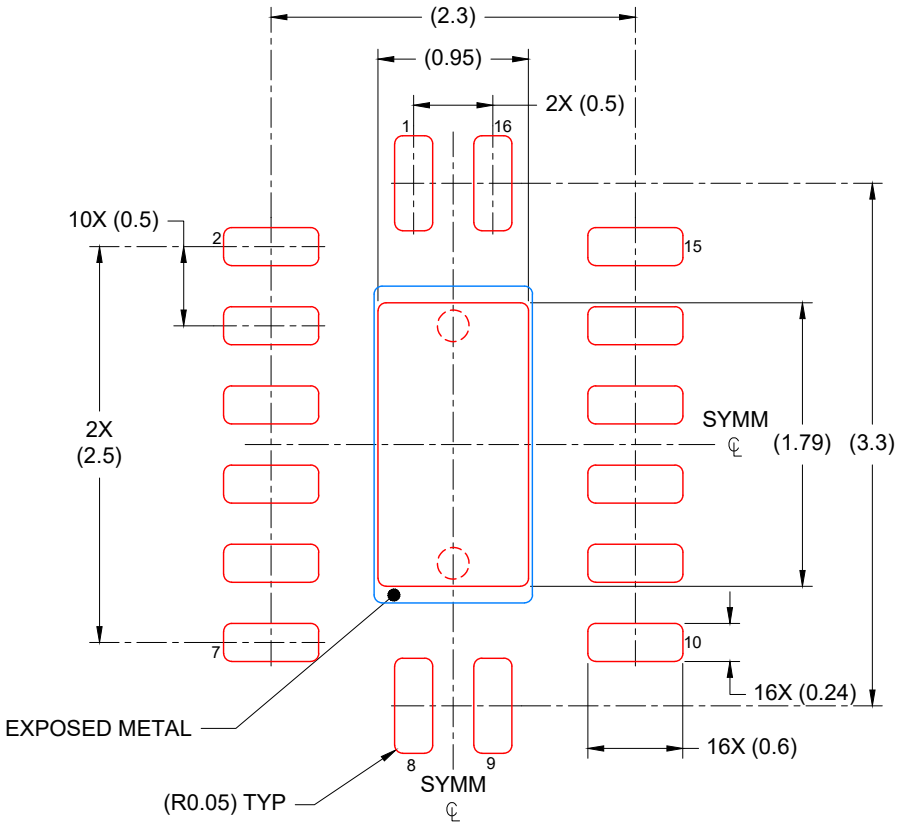


4224640/B 01/2026

1. NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/B 01/2026

NOTES: (continued)

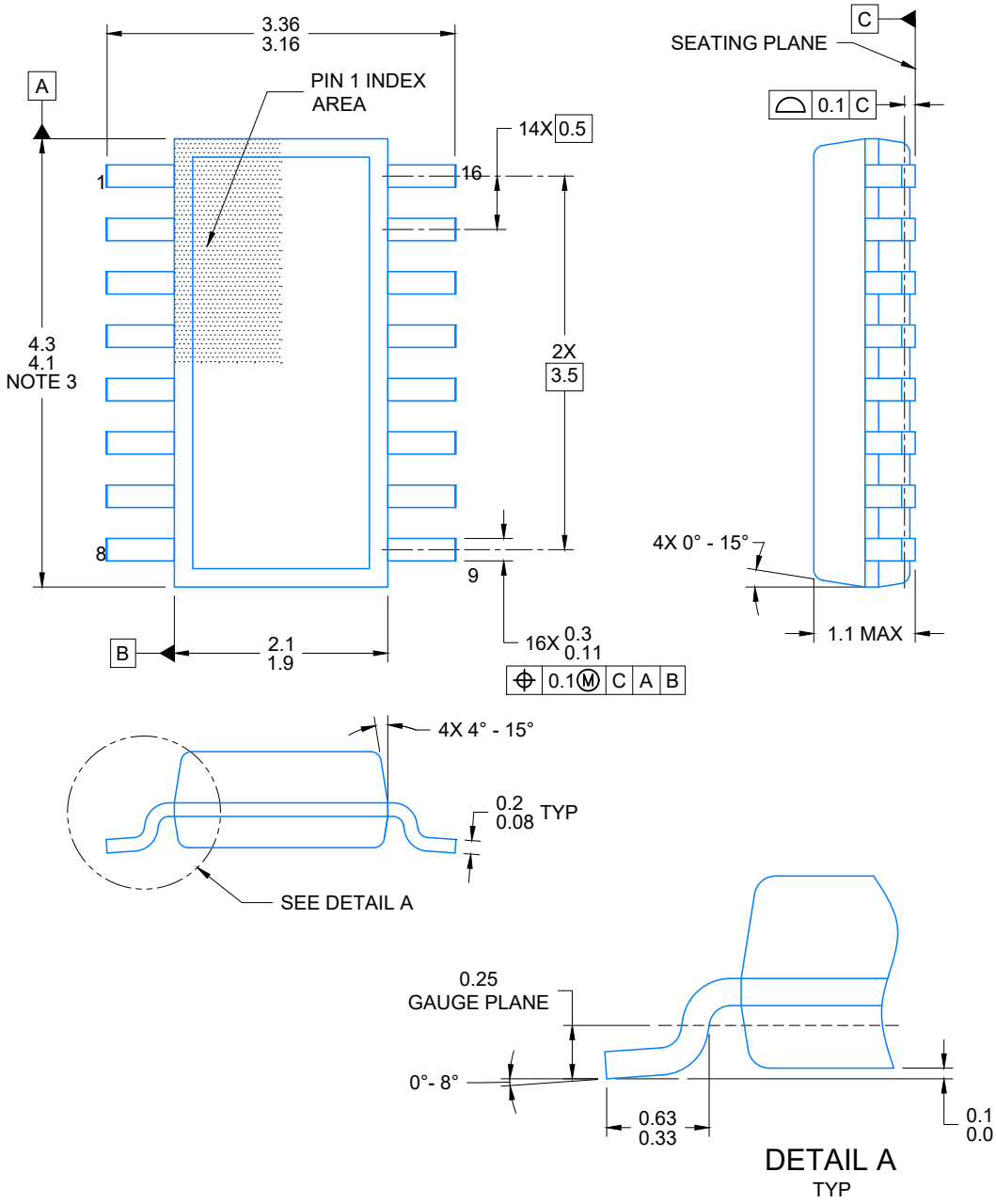
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0016A

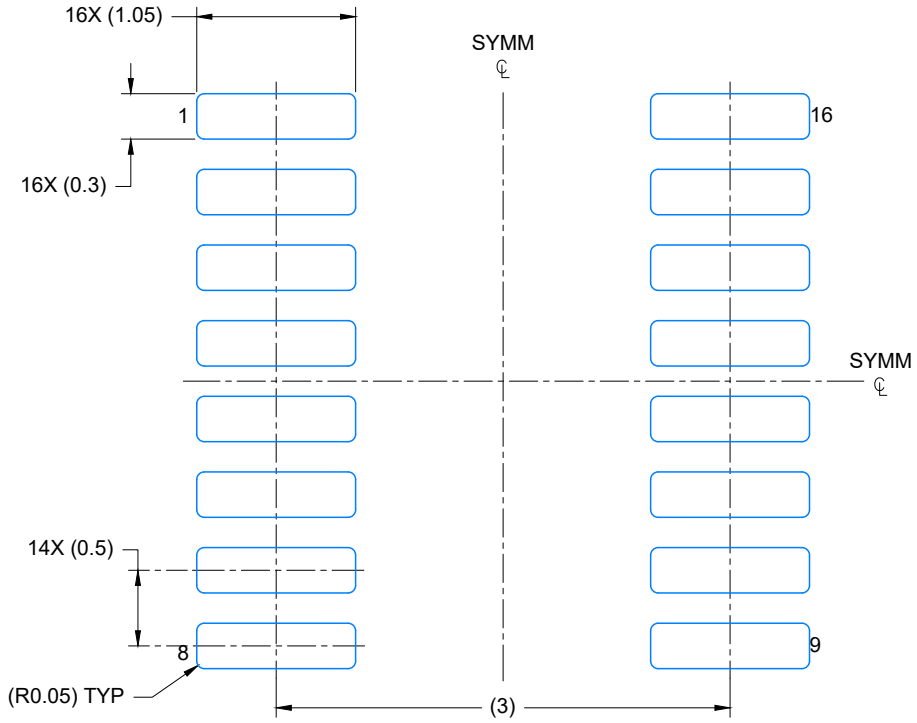
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

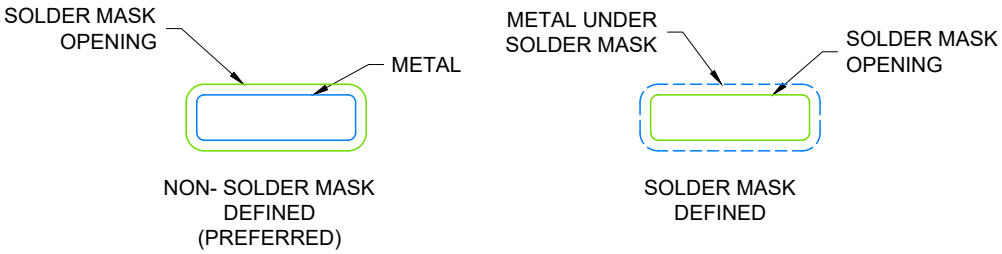


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

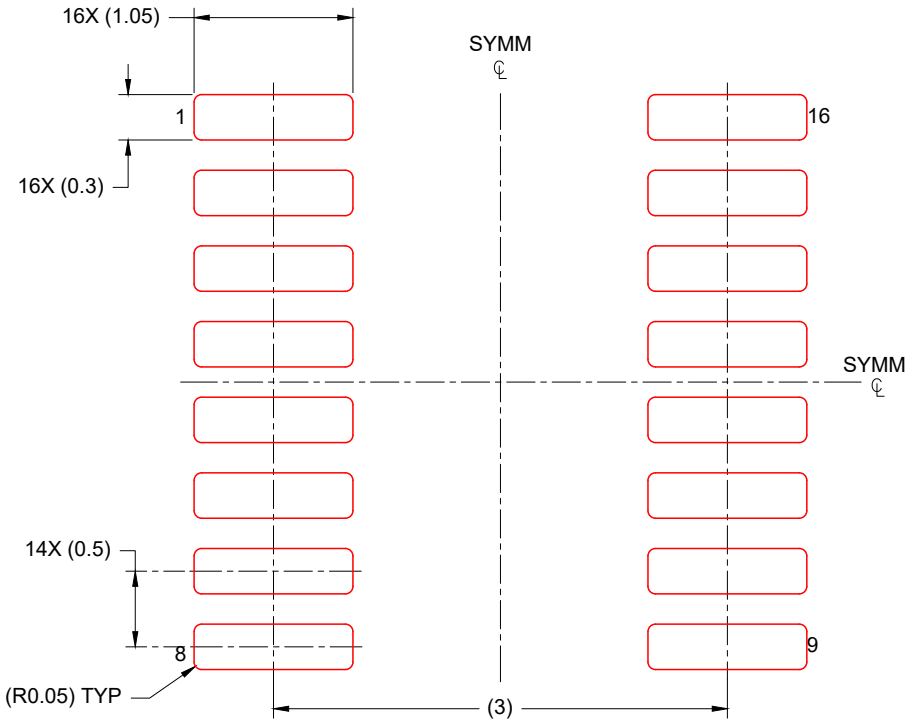
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

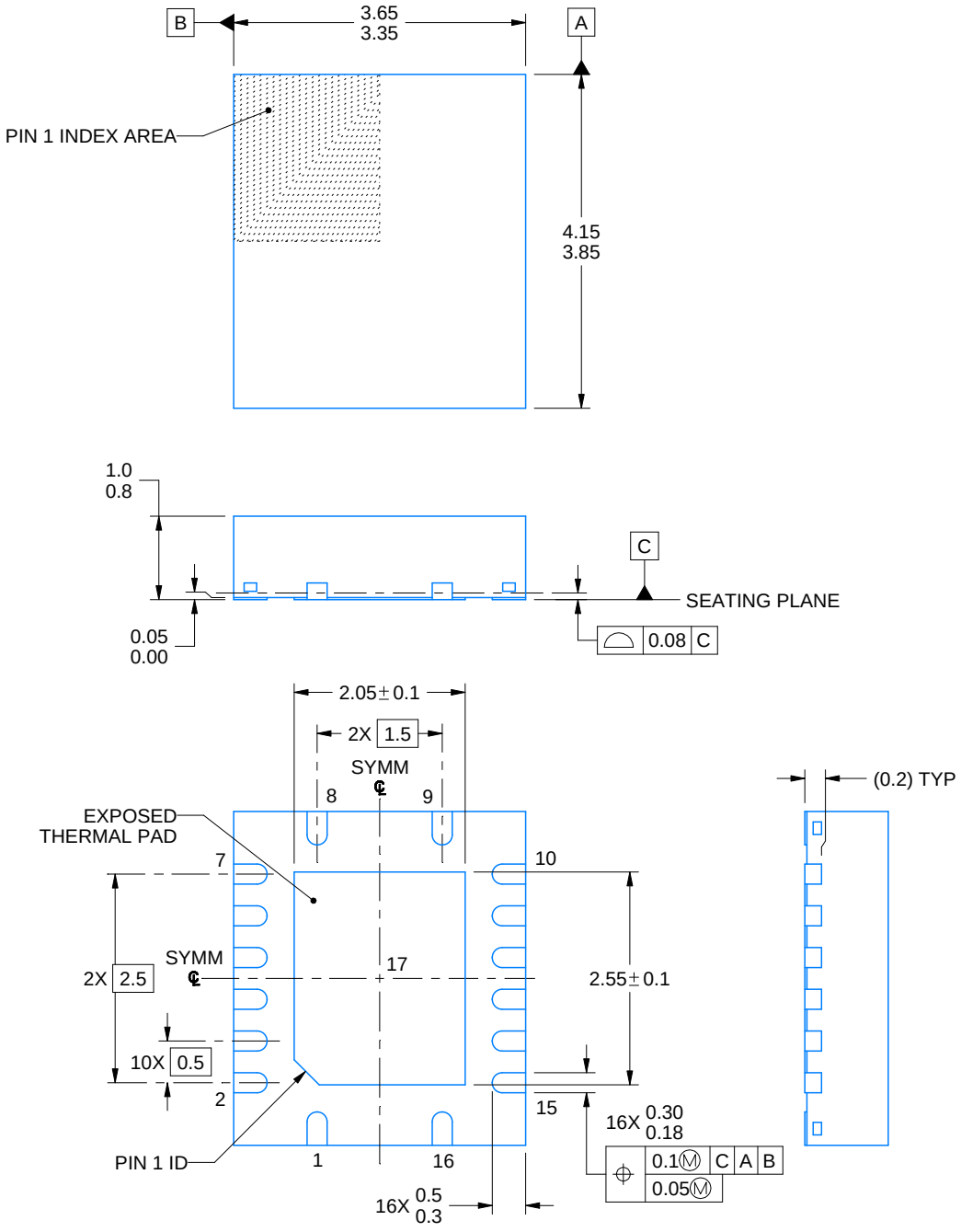
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY0016A

PACKAGE OUTLINE

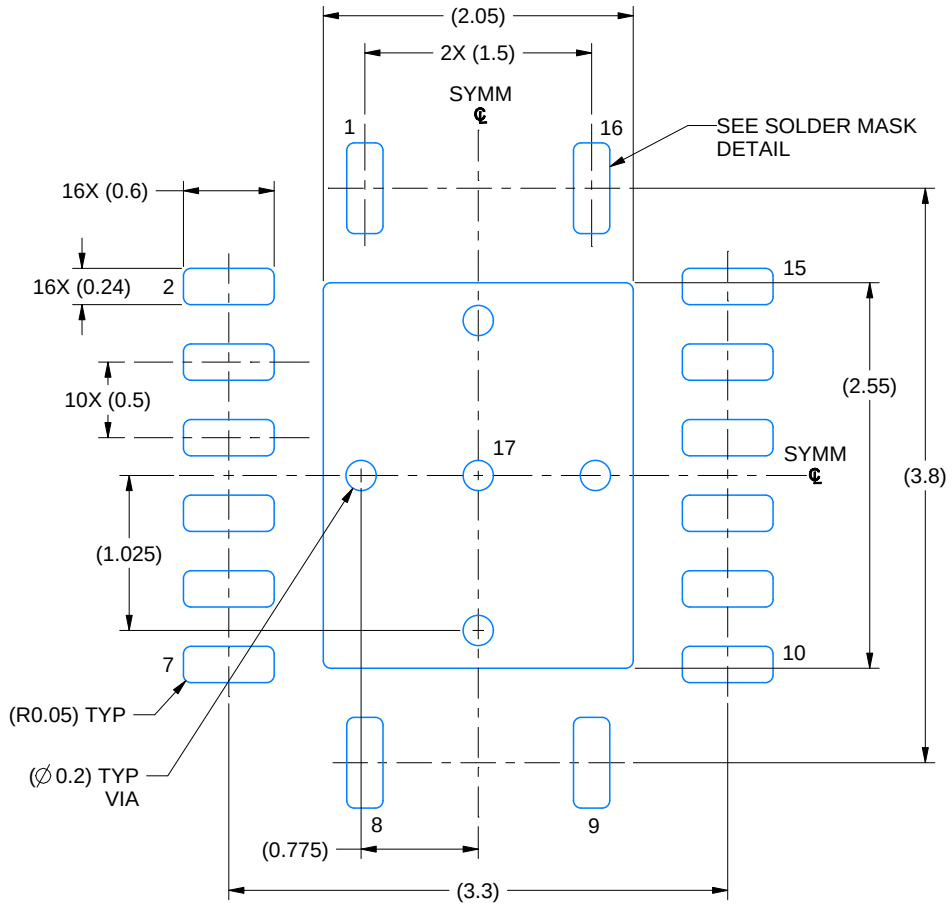
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

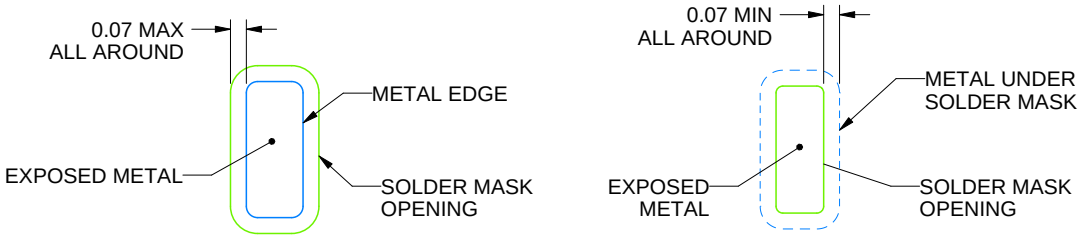


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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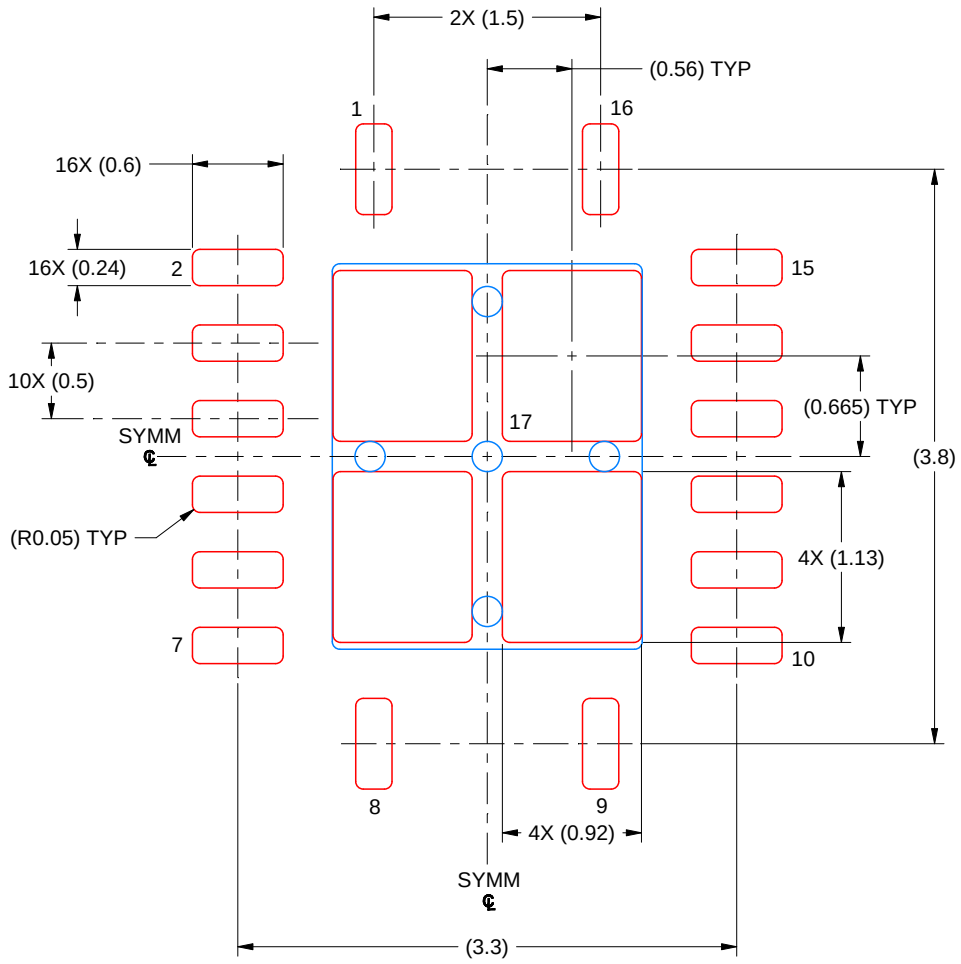
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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