SN74AHCT1G00 单通道双输入正与非门

1 特性

- 工作电压范围为 4.5 V 至 5.5V
- 5V 时 t_{pd} 最大值为 7.1ns
- 低功耗，I_{CC} 最大值为 10μA
- 电压为 5V 时，输出驱动为 ±8mA
- 输入兼容 TTL 电压
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- IP 电话
- 笔记本电脑
- 打印机
- 门禁与安防
- 太阳能逆变器

3 说明

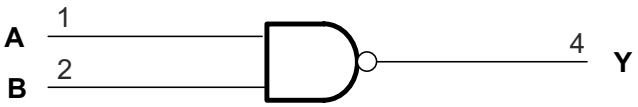
SN74AHCT1G00 器件以正逻辑执行布尔函数 $Y = \overline{A \times B}$ 或 $Y = \overline{A} + \overline{B}$。

封装信息

器件型号	封装 [1]	封装尺寸 [2]
SN74AHCT1G00	DBV（SOT-23，5）	2.8 mm × 2.8 mm
	DCK（SC-70，5）	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

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4 Pin Configuration and Functions

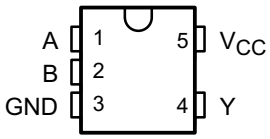

图 4-1. DBV or DCK Package 5-PIN SOT-23 OR SC-70 (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	A	I	Input A
2	B	I	Input B
3	GND	—	Ground Pin
4	Y	O	Output Y
5	V_{CC}	—	Power Pin

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Output voltage(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}	–20	20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}	–25	25	mA
	Continuous current through V_{CC} or GND		–50	50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level Input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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5.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT1G00		UNIT
		DBV (SOT-23)	DCK (SC-70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	289.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.5	205.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	184.4	176.2	
ψ_{JT}	Junction-to-top characterization parameter	115.4	117.6	
ψ_{JB}	Junction-to-board characterization parameter	183.4	175.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I_{OH} = –8 mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			1		10		10	µA
ΔI_{CC} [1]	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		2	10		10		10	pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuits and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		–40°C to 85°C		–40°C to 125°C		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF	5	6.2	1	7.1	1	8	ns
t_{PHL}				5	6.2	1	7.1	1	8	
t_{PLH}	A or B	Y	C_L = 15 pF	5.5	7.9	1	9	1	10	ns
t_{PHL}				5.5	7.9	1	9	1	10	

5.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	10.5	pF

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5.8 Typical Characteristics

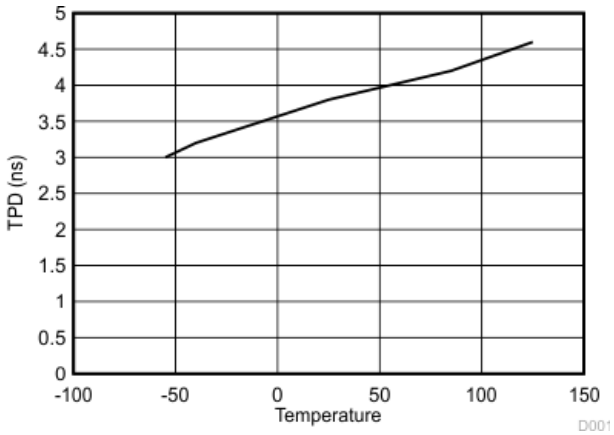

图 5-1. TPD vs Temperature

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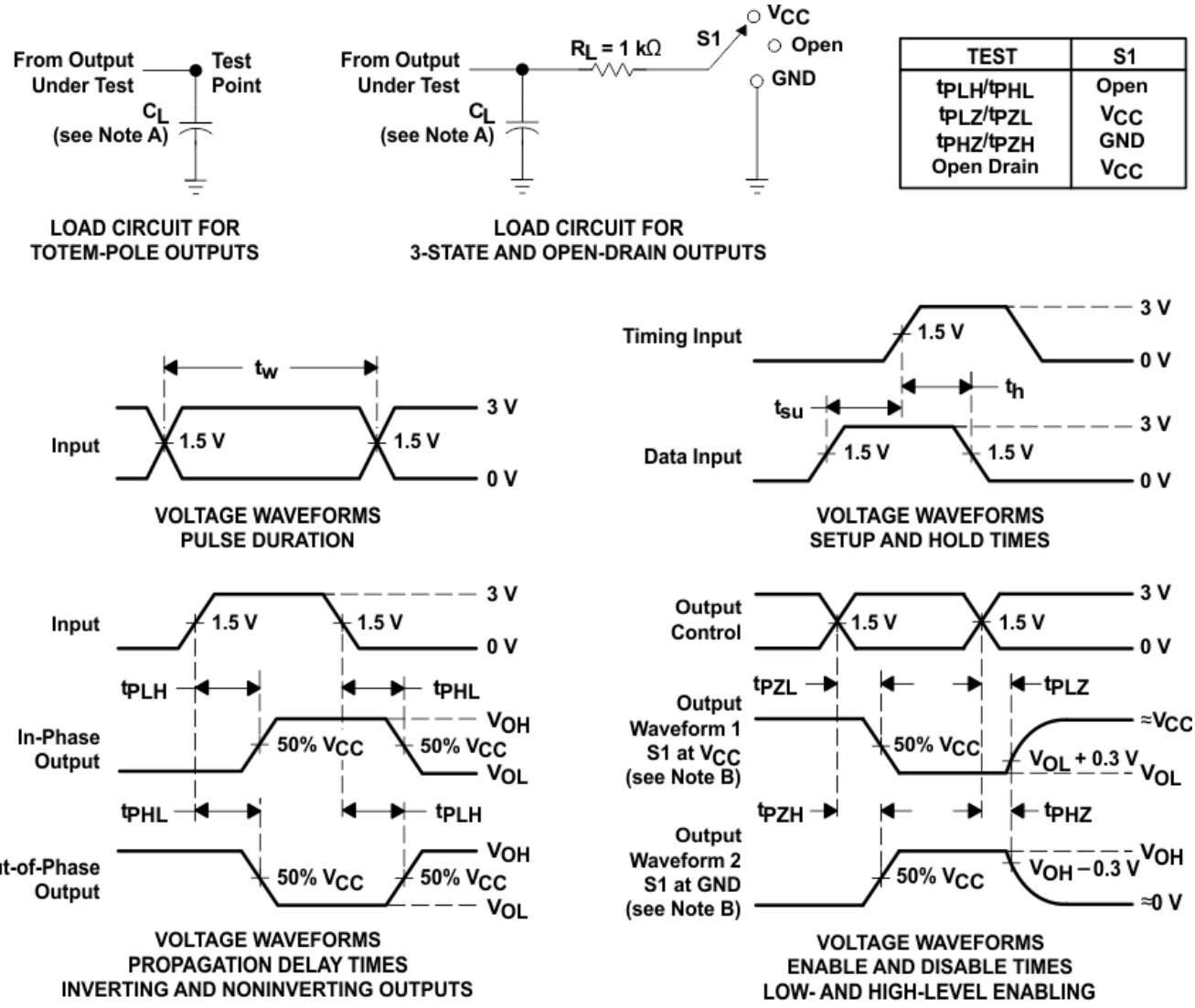
6 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuits and Voltage Waveforms

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7 Detailed Description

7.1 Overview

The SN74AHCT1G00 device performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The device has TTL inputs that allow up translation from 3.3 V to 5 V. The inputs are high impedance when V_{CC} = 0 V.

7.2 Functional Block Diagram

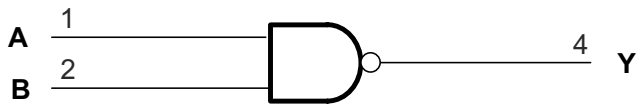

图 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

The device is ideal for operating in a 5-V logic system. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low power consumption makes this device a good choice for portable and battery power-sensitive applications.

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

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8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN74AHCT1G00 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The TTL inputs can except voltages down to 3.3 V and translate up to 5 V.

8.2 Typical Application

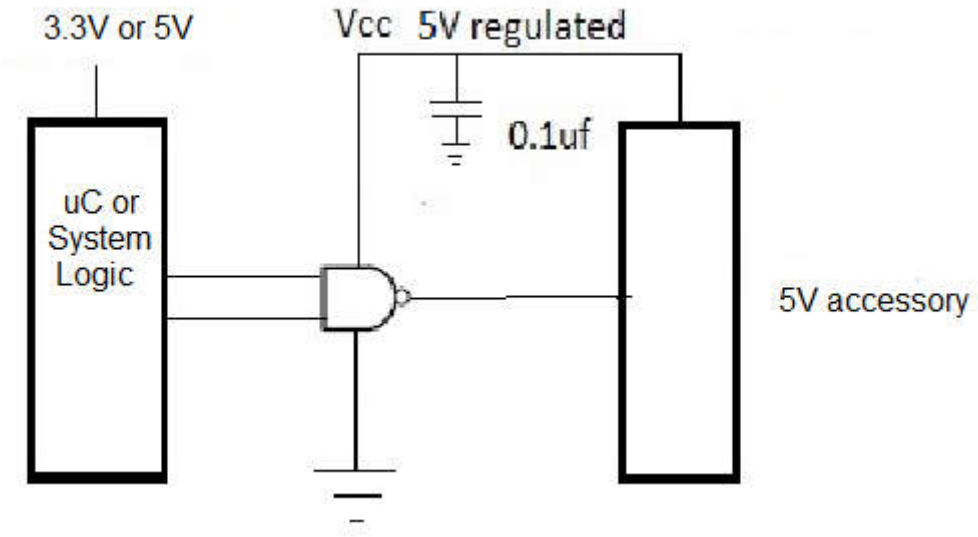

图 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

8.3 Detailed Design Procedure

- Recommended input conditions:
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *节 5.3*.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- Recommended output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V_{CC}.

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8.4 Application Curves

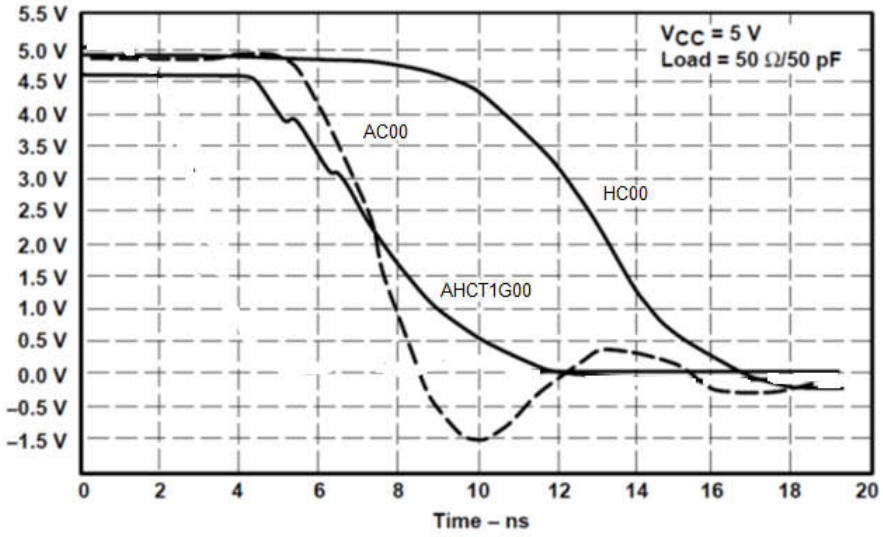

图 8-2. Switching Characteristics Comparison

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9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

Changes from Revision O (October 2023) to Revision P (February 2024)	Page
• Updated thermal values for DBV package from RθJA = 208.2 to 278, RθJC(top) = 76.1 to 180.5, RθJB = 52.5 to 184.4, ΨJT = 4 to 115.4, ΨJB = 51.8 to 183.4, RθJC(bot) = N/A, all values in °C/W	5

Changes from Revision N (March 2015) to Revision O (October 2023)	Page
• 向 *封装信息* 表中添加了封装尺寸	1
• Updated thermal values for DCK package from RθJA = 287.6 to 289.2, RθJC(top) = 97.7 to 205.8, RθJB = 65 to 176.2, ΨJT = 2 to 117.6, ΨJB = 64.2 to 175.1, RθJC(bot) = N/A, all values in °C/W	5

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AHCT1G00DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B00G
74AHCT1G00DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B00G
74AHCT1G00DBVTG4	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	B00G
74AHCT1G00DCKRE4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BA3
74AHCT1G00DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BA3
74AHCT1G00DCKRG4.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BA3
74AHCT1G00DCKTG4	Obsolete	Production	SC70 (DCK) | 5	-	-	Call TI	Call TI	-40 to 125	BA3
SN74AHCT1G00DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(37UH, 3C5F, B003, B00G, B00J, B 00S)
SN74AHCT1G00DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(37UH, 3C5F, B003, B00G, B00J, B 00S)
SN74AHCT1G00DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	(B003, B00G, B00J, B00S)
SN74AHCT1G00DCK3	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 85	BAY
SN74AHCT1G00DCK3.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 85	BAY
SN74AHCT1G00DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QO, BA3, BAG, BA J, BAS)
SN74AHCT1G00DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QO, BA3, BAG, BA J, BAS)
SN74AHCT1G00DCKT	Obsolete	Production	SC70 (DCK) | 5	-	-	Call TI	Call TI	-40 to 125	(BA3, BAG, BAJ, BA S)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AHCT1G00 :

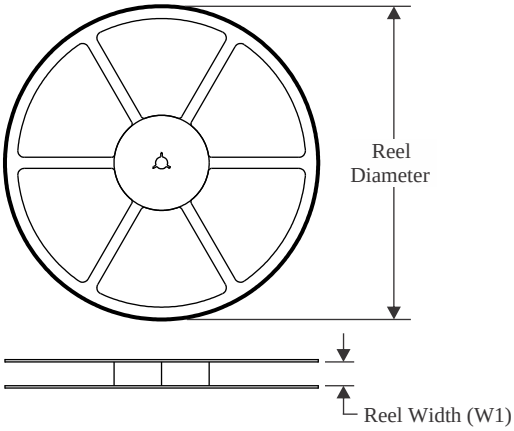
- Automotive : SN74AHCT1G00-Q1

NOTE: Qualified Version Definitions:

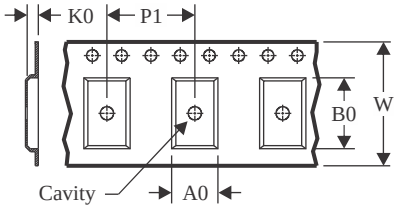
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

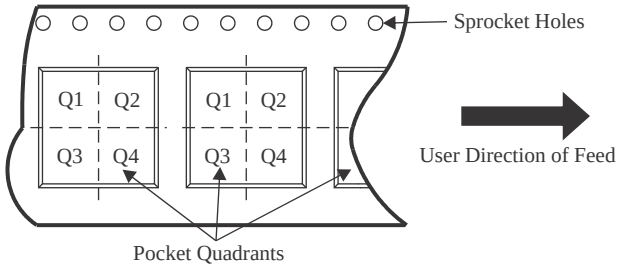


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

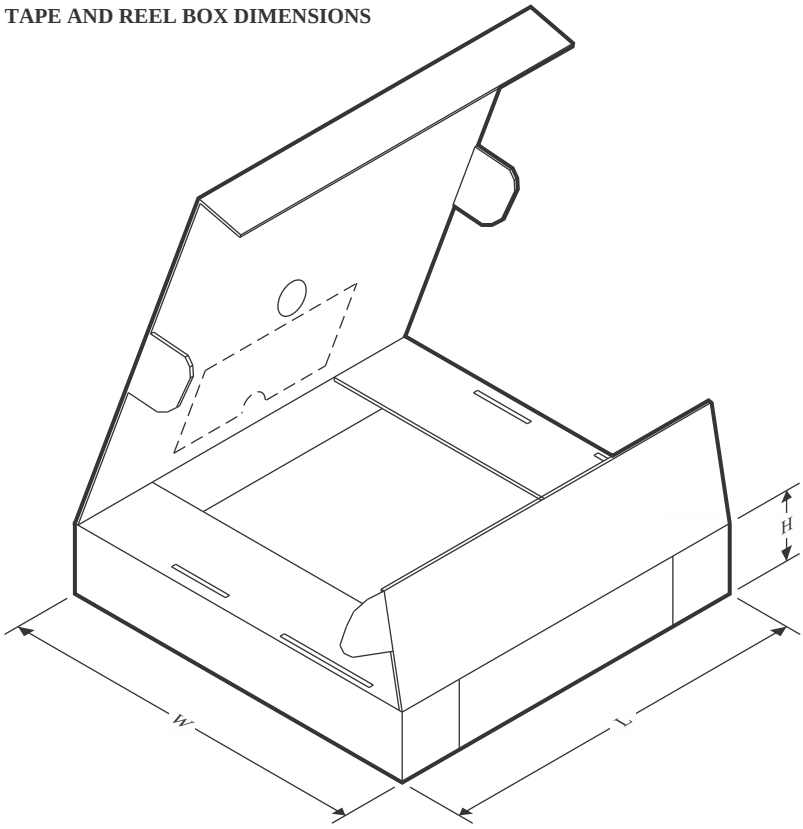
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHCT1G00DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G00DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G00DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G00DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G00DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G00DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74AHCT1G00DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

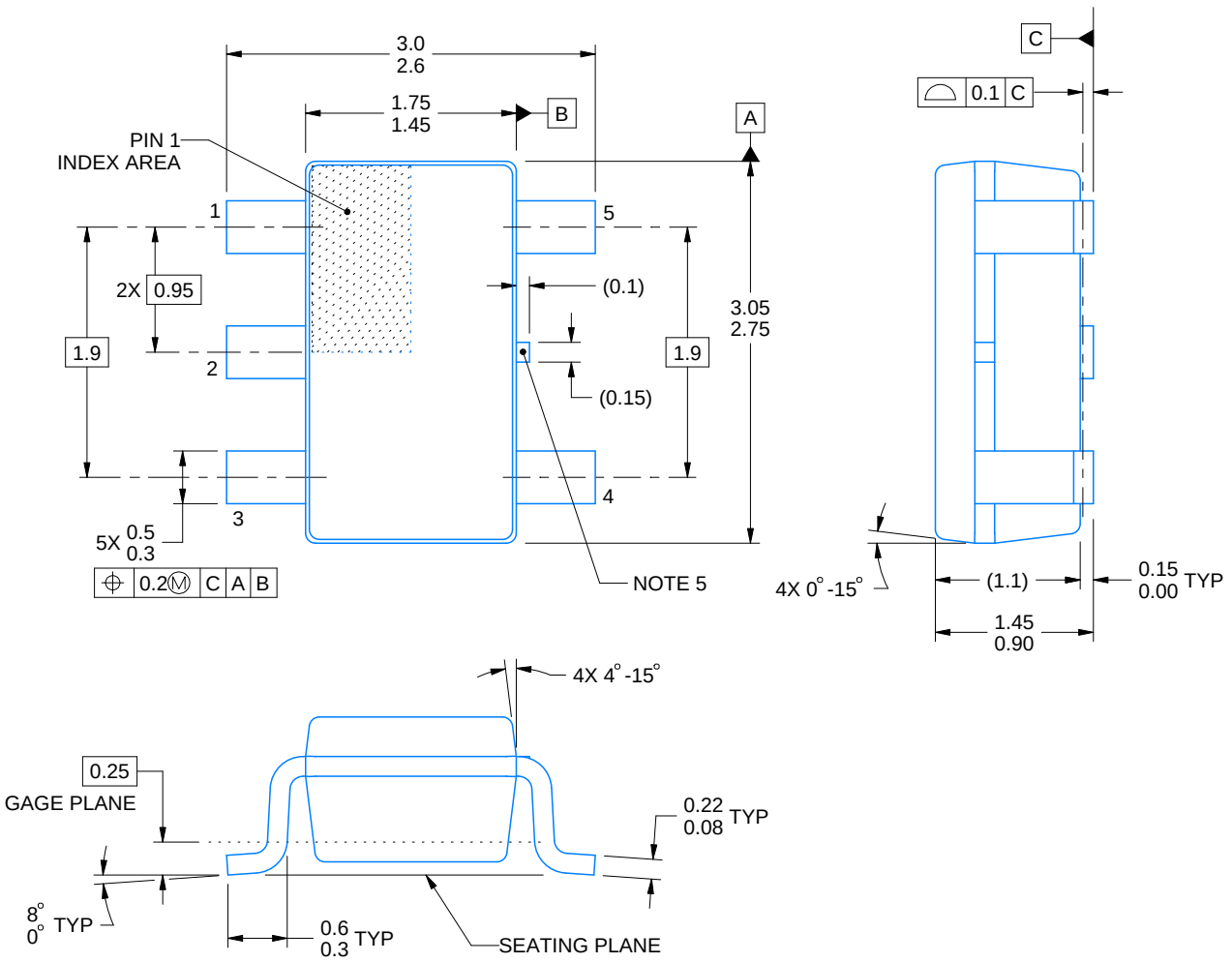
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHCT1G00DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHCT1G00DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHCT1G00DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHCT1G00DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74AHCT1G00DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHCT1G00DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AHCT1G00DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

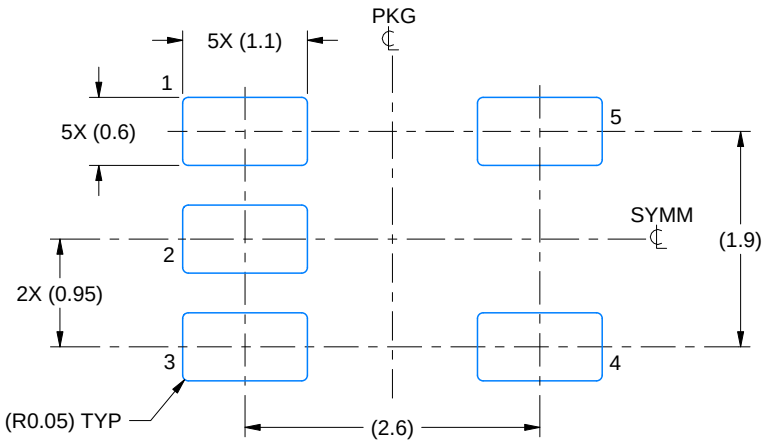
SMALL OUTLINE TRANSISTOR



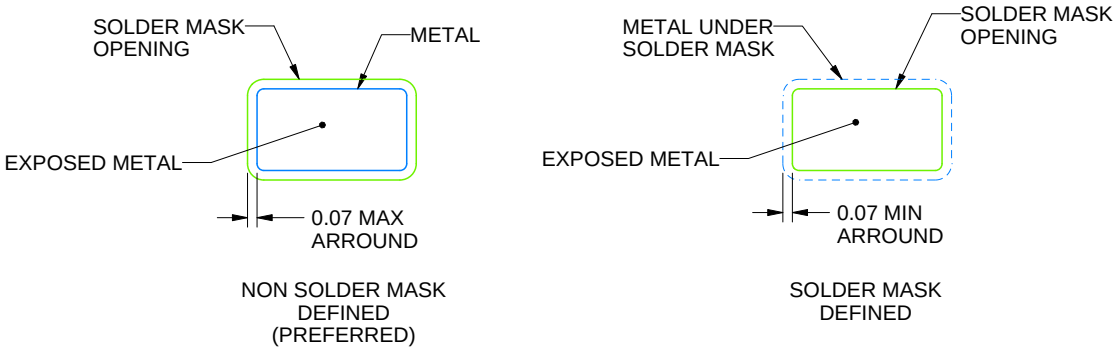
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

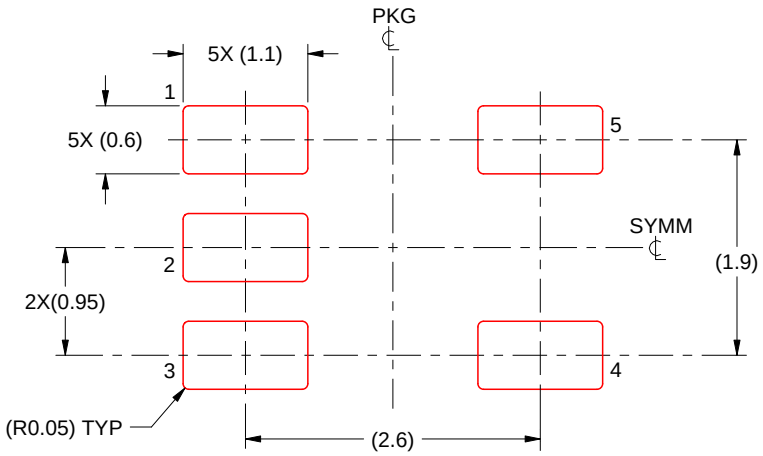


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

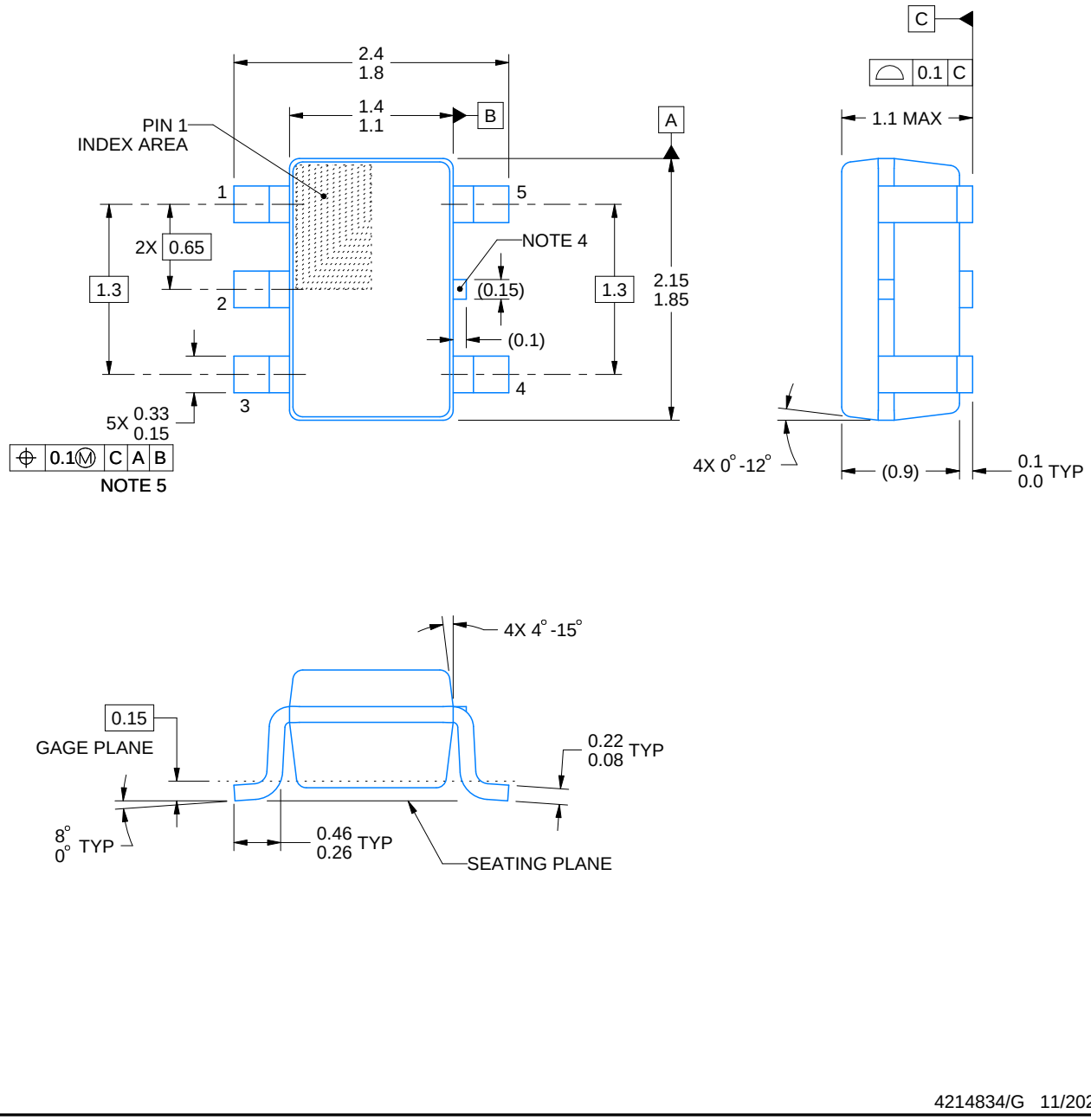
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

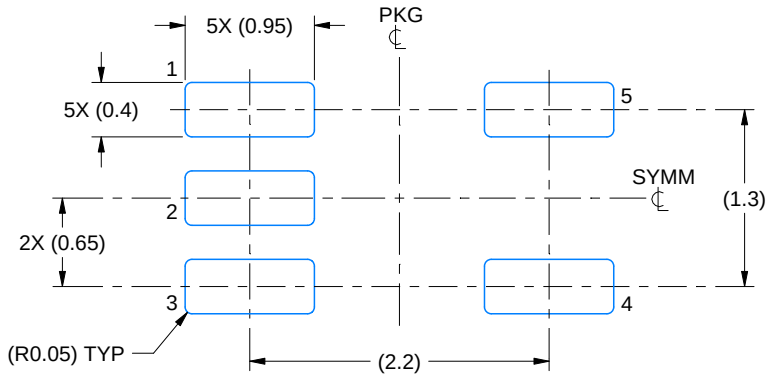
SMALL OUTLINE TRANSISTOR



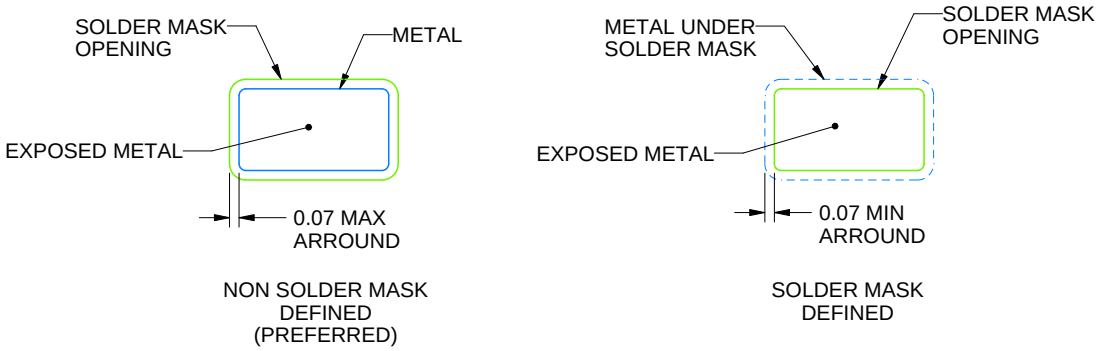
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

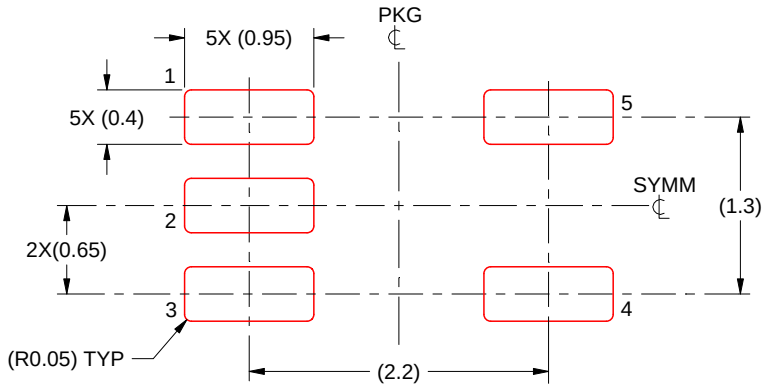


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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