OPA137, OPA2137, OPA4137 Low Cost FET-Input Operational Amplifiers Micro Amplifier™ Series

1 Features

- FET Input: I_B = ±10pA
- Low offset voltage: ±300mV
- Wide supply range: ±2.25 V to ±18 V
- Low quiescent current: 120µA/channel
- Excellent speed/power: 1.1MHz
- Input to positive supply
- Single, dual, and quad

2 Applications

- Strain gage amplifier
- Photodetector amplifier
- Precision integrator
- Battery-powered instruments
- Test equipment
- Active filters

3 Description

OPA137 series FET- input operational amplifiers are designed for low cost and miniature applications. In addition to small size (SOT-23-5 and MSOP-8 packages), amplifiers provide low input bias current (±10pA), low quiescent current (120µA/ channel), and high open-loop gain (145dB).

Either single (+4.5V to +36V) or dual (±2.25V to ±18V) supplies can be used. The input common-mode voltage range includes the positive supply an excellent choice for many single-supply applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

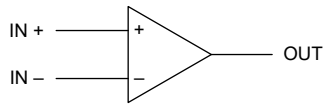
OPA137 op amps are easy to use and free from phase inversion and overload problems found in some FET- input amplifiers. High performance, including linearity, is maintained as the amplifiers swing to the specified limits. In addition, the combination of high slew rate (4.5V/µs) and wide bandwidth (1.1MHz) provide fast settling time verifies good dynamic response. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

The single (OPA137) packages are the tiny 5-lead SOT-23-5 surface mount, SO-8 surface mount, and 8-pin DIP. The dual (OPA2137) comes in the miniature MSOP-8 surface mount, and the SO-8 surface mount. The quad (OPA4137) packages are the SO-14 surface mount and the 14-pin DIP. All are specified from – 40°C to +85°C and operate from – 55°C to +125°C. A SPICE macro-model is available for design analysis.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
OPA137	SOIC (8)	4.90mm × 3.90mm
	SOT-23 (5)	2.90mm × 1.60mm
OPA2137	VSSOP (8)	3.00mm × 3.00mm
	SOIC (8)	4.90mm × 3.90mm
	PDIP (8)	6.35mm × 9.81mm
OPA4137	PDIP (14)	6.35mm × 19.30mm
	SOIC (14)	3.91mm × 8.65mm

(1) For more information, see Section 9.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol (Each Amplifier)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

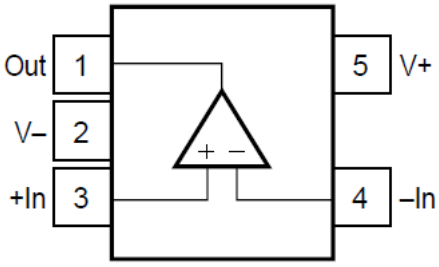

Figure 4-1. OPA137 SOT-23-5

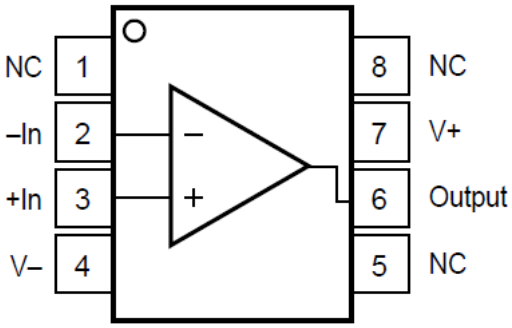

Figure 4-2. OPA137, SO-8

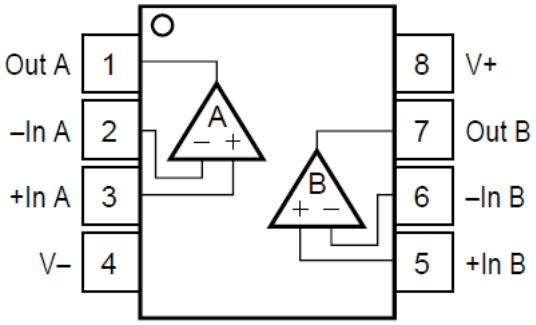

Figure 4-3. OPA2137 8-Pin DIP, SO-8, MSOP-8

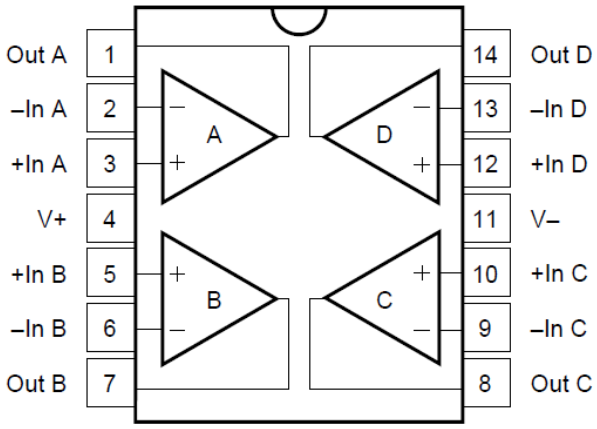

Figure 4-4. OPA4137 14-Pin DIP, SO-14

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V+ to V–	Supply voltage		36	V
	Input voltage	-0.7	+0.7	V
	Input current		2	mA
	Output short-circuit[2]	Continuous		
	Operating temperature	-55	+125	℃
	Storage temperature	-55	+125	℃
	Junction temperature		+150	℃
	Lead temperature (soldering, 10s)		300	℃

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	±2.25	±36	V
V_I	Input voltage range	V ±3		V
T_A	Specified temperature	–40	+85	°C

5.4 Electrical Characteristics, V_S = ±15V

At T_A =+25°C, R_L = 10kΩ connected to ground, unless otherwise noted.(1)
Limits apply over the specified temperature range, T_A =–40°C to +85°C.

PARAMETER		CONDITION	OPA137N, U, P OPA2137E, U, P OPA4137U, P			OPA137NA, UA, PA OPA2137EA, UA, PA OPA4137UA, PA			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE									
V_{OS}	Input offset voltage			±0.3	±3		±0.3	±10	mV
	T_A = –40°C to +85°C				**±7**			**±15**	mV
	dV_{OS}/dT vs Temperature	T_A = –40°C to +85°C		0.6					µV/°C
	PSRR vs Power supply	V_S = ±3V to ±18V		0.1	±250				µV/V
	T_A = –40°C to +85°C				±250				µV/V
	Channel separation (dual, quad)	dc		5					µV/V
INPUT BIAS CURRENT									
I_B	Input bias current	V_{CM} = 0V		±10					pA
	vs Temperature			See Section 5.5					
I_{OS}	Input offset current			±5					
NOISE									
	Input voltage noise, f = 0.1Hz to 10Hz			6					µVp-p
e_n	Input voltage noise density, f = 1kHz			30					nV/√Hz
i_n	Current noise density, f = 1kHz			2					fA/√Hz
INPUT VOLTAGE RANGE									
V_{CM}	Common-mode voltage range		(V–) + 3		(V+)				V
CMRR	Common-mode rejection ratio	V_{CM} = –12V to 13V							
	OPA137, OPA2137		76	84		70			dB
	OPA4137		74	84		70			dB
	T_A = –40°C to +85°C								
	OPA137,OPA2137		**72**			**70**			dB
	OPA4137		**70**			**70**			dB
INPUT IMPEDANCE									
	Differential			10^{10}||3					Ω ||pF
	Common-mode			10^{12}||1					Ω ||pF
OPEN-LOOP GAIN									
A_{OL}	Open-loop voltage gain	V_O = –13.8V to 13.9V	86	94					dB
	T_A = –40°C to +85°C		**86**						dB
FREQUENCY RESPONSE									
GBW	Gain-bandwidth product			1.1					MHz

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5.4 Electrical Characteristics, V_S = ±15V (continued)

At T_A =+25°C, R_L = 10kΩ connected to ground, unless otherwise noted.(1)
Limits apply over the specified temperature range, T_A =–40°C to +85°C.

PARAMETER		CONDITION	OPA137N, U, P OPA2137E, U, P OPA4137U, P			OPA137NA, UA, PA OPA2137EA, UA, PA OPA4137UA, PA			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	G = 1, 10V Step, C_L = 100pF		4.5					V/µs
Settling time	0.1%			4					µs
	0.01%			5					µs
	Overload recovery time	V_{IN} • G = V_S		1					µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1kHz, 3.5Vrms		0.02					%
OUTPUT									
V_{OUT}	Voltage output		(V–) + 1.2		(V+) – 1.1				V
	T_A = –40°C to +85°C		**(V–) + 1.2**		**(V+) – 1.1**				V
I_{SC}	Short-circuit current			–25/+60					mA
C_{LOAD}	Capacitive load drive			330					pF
ZO	Open-loop output impedance	f = 1MHz, IO = 0A		575			575		Ω
POWER SUPPLY									
V_S	Specified operating range			±15					V
	Operating voltage range								
	Dual supplies		±2.25(1)		±18				V
	Single supply		+4.5		+36				V
I_Q	Quiescent current	I_O = 0		±120	±270				µA
	T_A= –40°C to +85°C				**±375**				µA

(1) At minimum power supply, voltage inputs must be biased above ground in accordance with common-mode voltage range restrictions.

5.5 Typical Characteristics

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, connected to ground, unless otherwise noted.

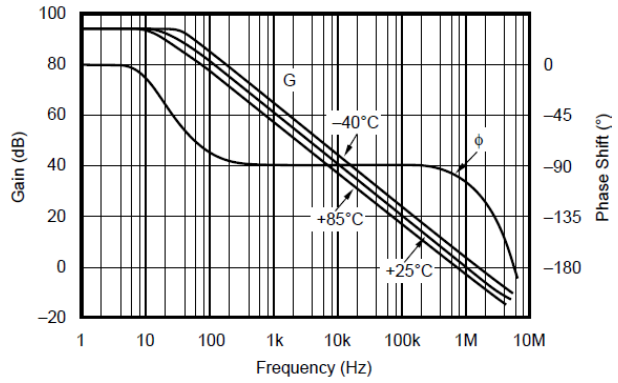

Figure 5-1. Open-Loop Gain/Phase vs Frequency (Old die)

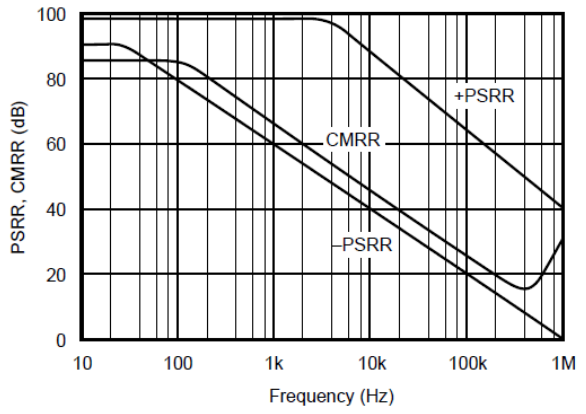

Figure 5-2. Power Supply and Common-Mode Rejection vs Frequency (Old die)

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5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, connected to ground, unless otherwise noted.

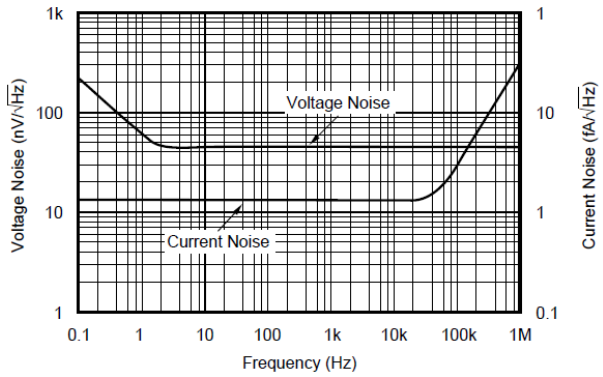

Figure 5-3. Input Voltage and Current Noise Spectral Density vs Frequency (Old die)

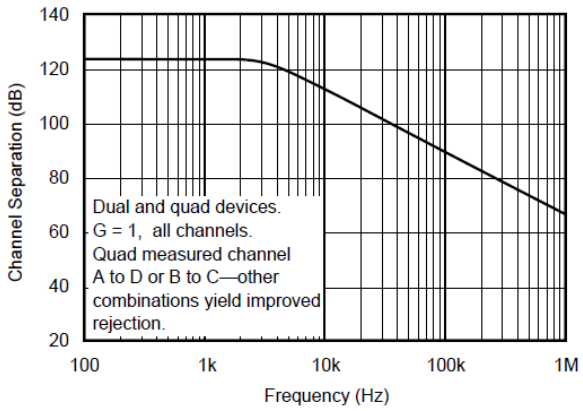

Figure 5-4. Channel Separation vs Frequency (Old die)

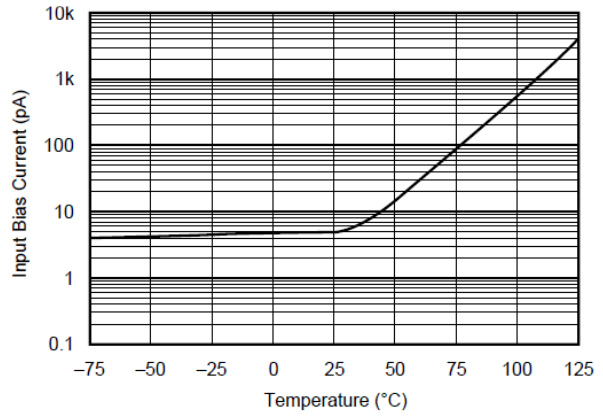

Figure 5-5. Input Bias Current vs Temperature (Old die)

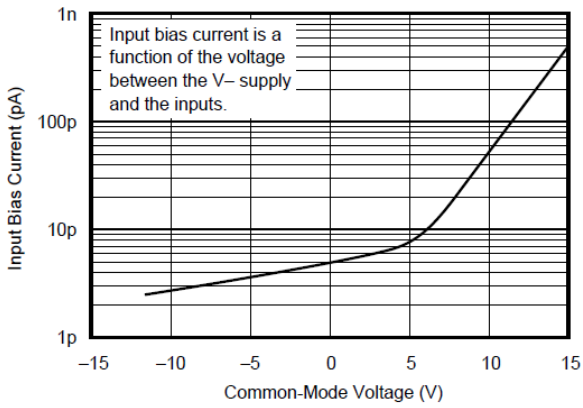

Figure 5-6. Input Bias Current vs Input Common-Mode Voltage (Old die)

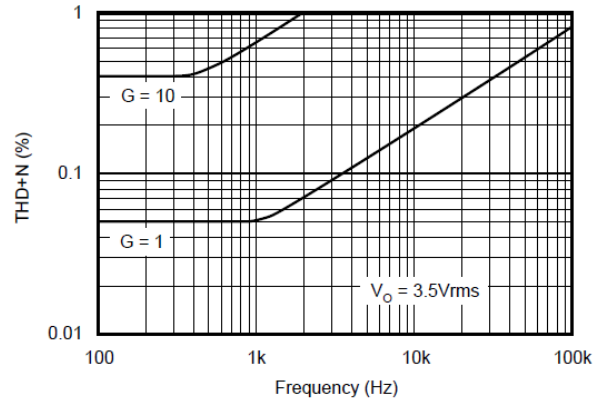

Figure 5-7. Total Harmonic Distortion + Noise vs Frequency (Old die)

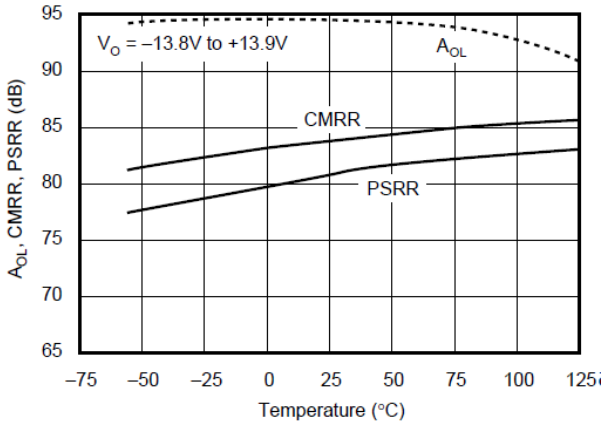

Figure 5-8. A_{OL}, CMRR, PSRR vs Temperature (Old die)

5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, connected to ground, unless otherwise noted.

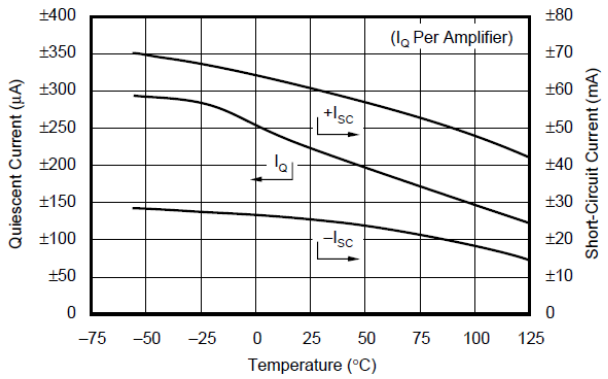

Figure 5-9. Quiescent Current and Short-Circuit Current vs Temperature (Old die)

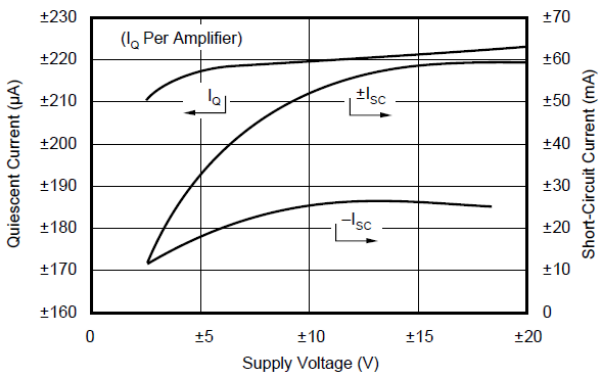

Figure 5-10. Quiescent Current and Short-Circuit Current vs Supply Voltage (Old die)

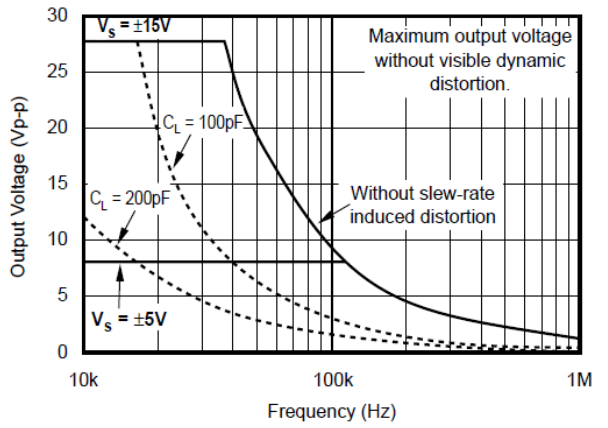

Figure 5-11. Maximum Output Voltage vs Frequency (Old die)

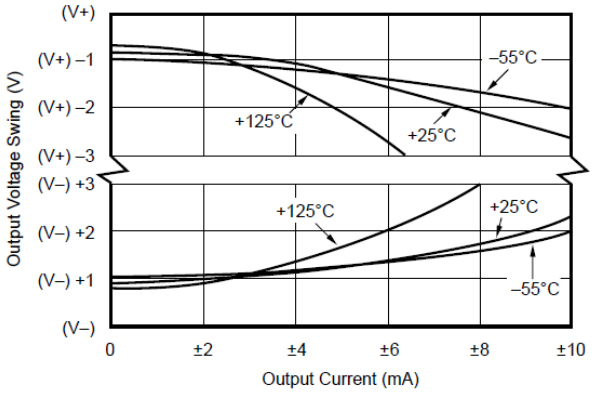

Figure 5-12. Output Voltage Swing vs Output Current (Old die)

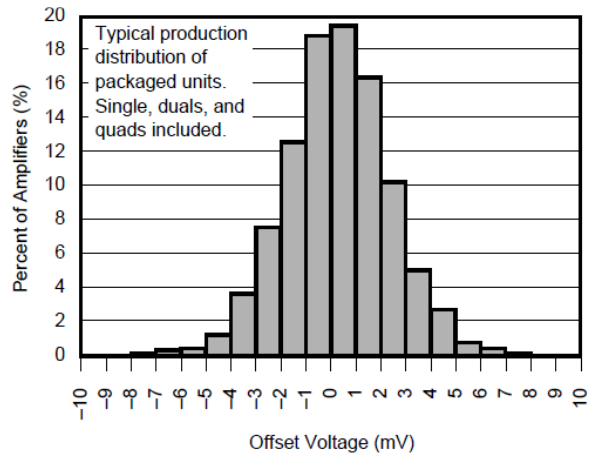

Figure 5-13. Offset Voltage Production Distribution (Old die)

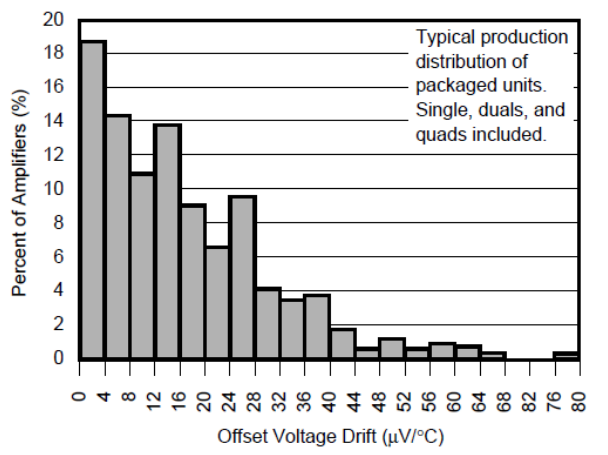

Figure 5-14. Offset Voltage Drift Production Distribution (Old die)

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5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, connected to ground, unless otherwise noted.

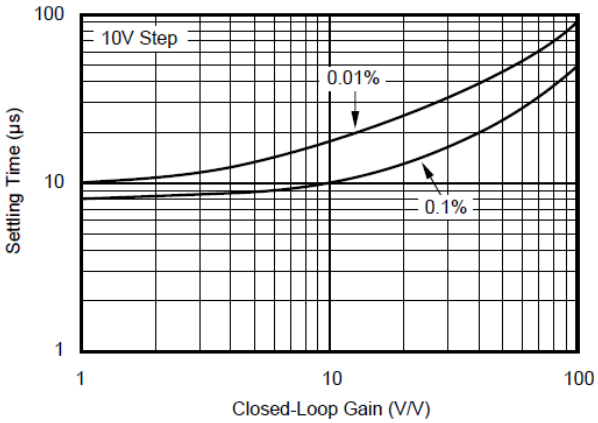


Figure 5-15. Settling Time vs Closed-Loop Gain (Old die)

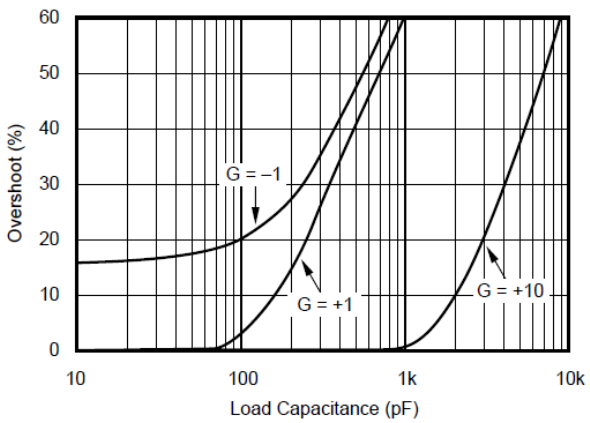


Figure 5-16. Small-Signal Overshoot vs Load Capacitance (Old die)

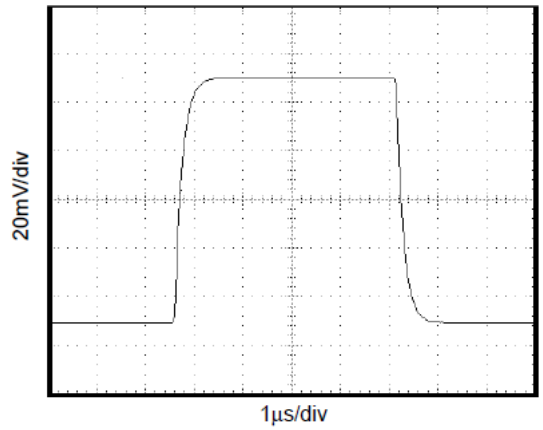


Figure 5-17. Small-Signal Step Response G = 1, C_L = 50pF (Old die)

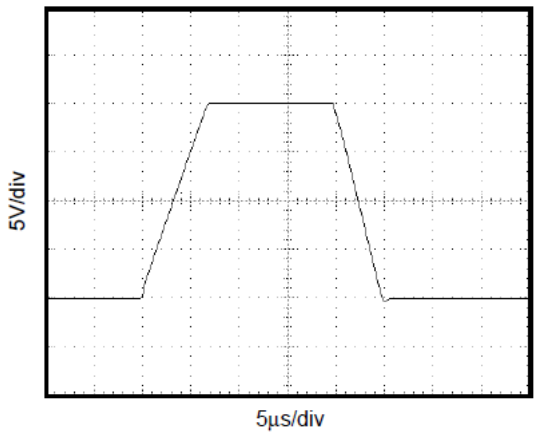
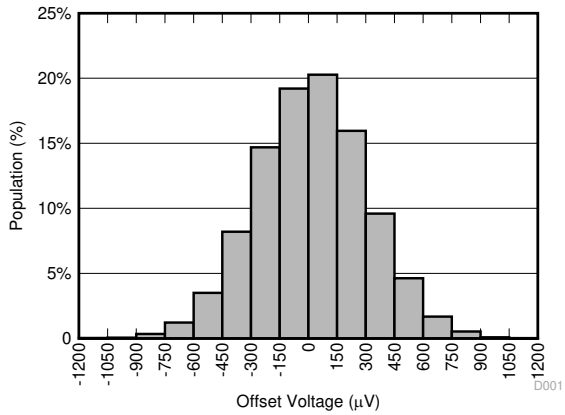
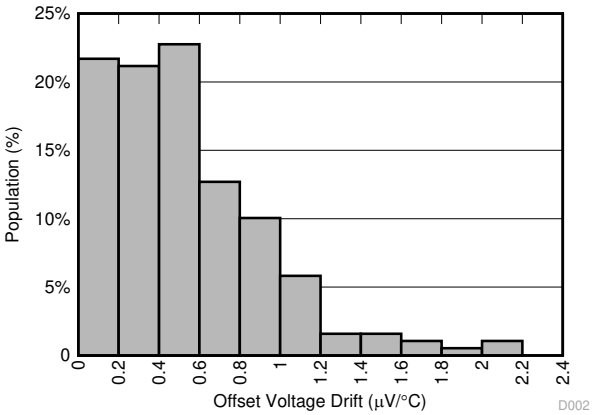


Figure 5-18. Large-Signal Step Response G = 1, C_L = 50pF (Old die)



Distribution from 15526 amplifiers, T_A = 25°C

Figure 5-19. Offset Voltage Production Distribution (New Die)

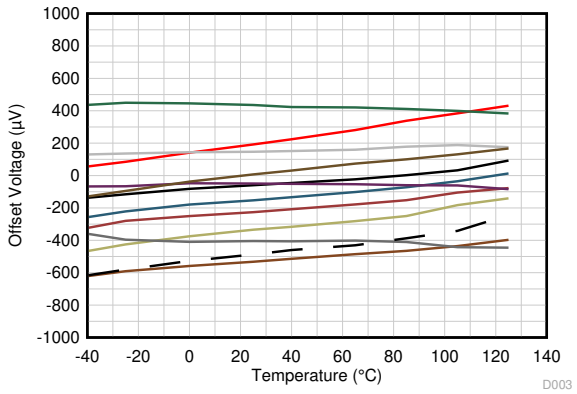


Distribution from 190 amplifiers

Figure 5-20. Offset Voltage Drift Distribution (New Die)

5.5 Typical Characteristics (continued)

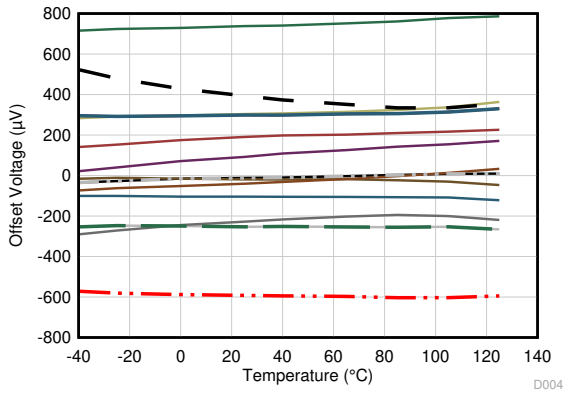
At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, connected to ground, unless otherwise noted.



V_{CM} = V+

Each color represents one sample device.

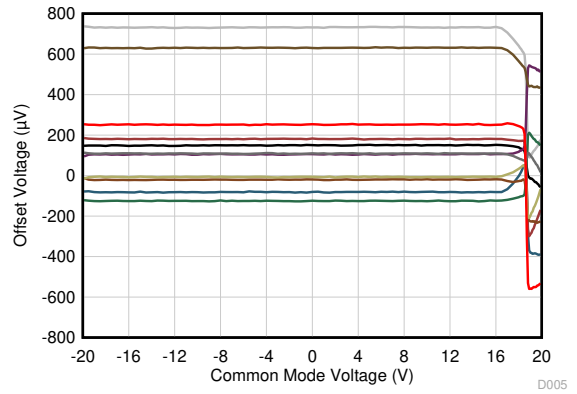
Figure 5-21. Offset Voltage vs Temperature (New Die)



V_{CM} = V–

Each color represents one sample device.

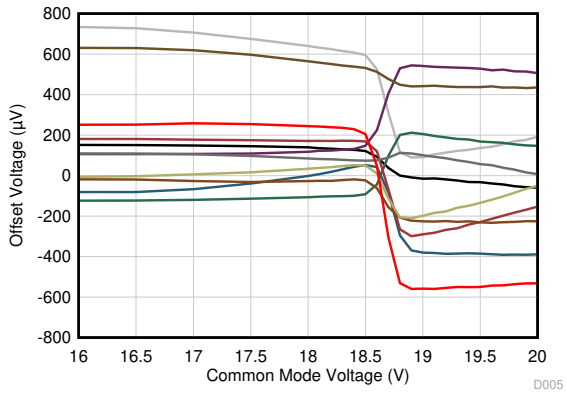
Figure 5-22. Offset Voltage vs Temperature (New Die)



T_A = 25°C

Each color represents one sample device.

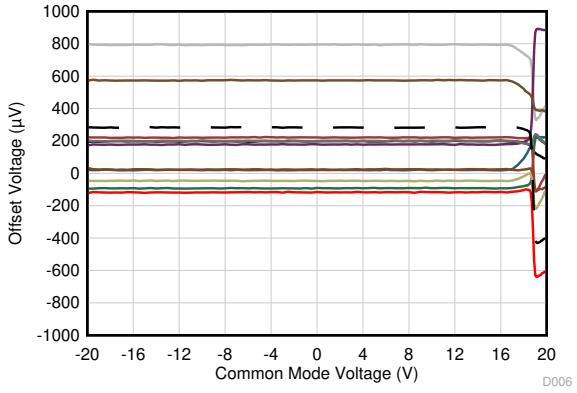
Figure 5-23. Offset Voltage vs Common-Mode Voltage (New Die)



T_A = 25°C

Each color represents one sample device.

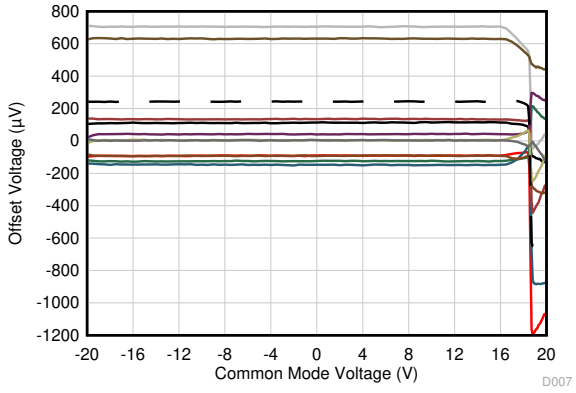
Figure 5-24. Offset Voltage vs Common-Mode Voltage (Transition Region) (New Die)



T_A = 125°C

Each color represents one sample device.

Figure 5-25. Offset Voltage vs Common-Mode Voltage (New Die)



T_A = –40°C

Each color represents one sample device.

Figure 5-26. Offset Voltage vs Common-Mode Voltage (New Die)

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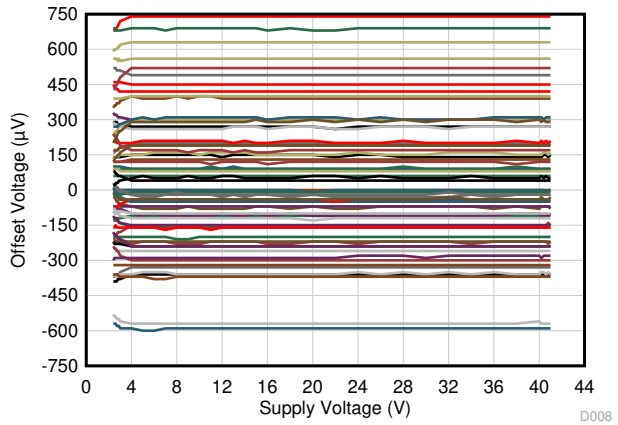
5.5 Typical Characteristics (continued)

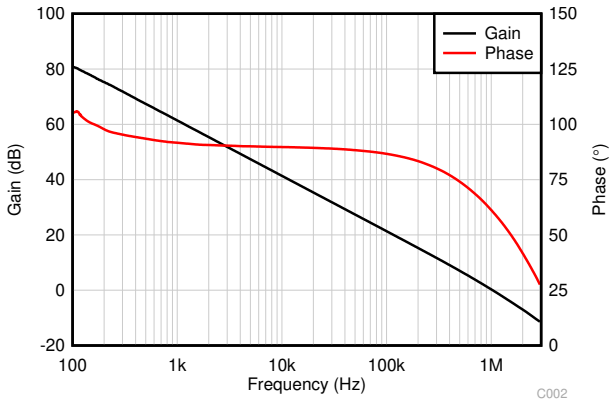
At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, connected to ground, unless otherwise noted.



V_{CM} = V–

Each color represents one sample device.

Figure 5-27. Offset Voltage vs Power Supply (New Die)



C_L = 20pF

Figure 5-28. Open-Loop Gain and Phase vs Frequency (New Die)

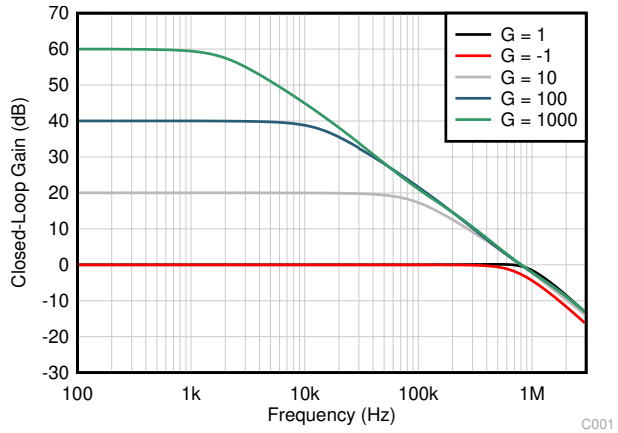


Figure 5-29. Closed-Loop Gain vs Frequency (New Die)

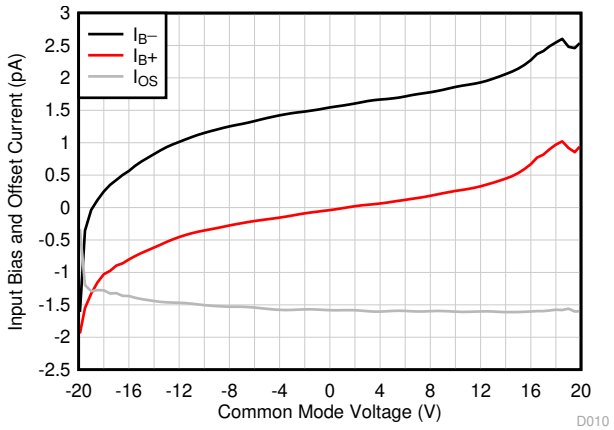


Figure 5-30. Input Bias Current vs Common-Mode Voltage (New Die)

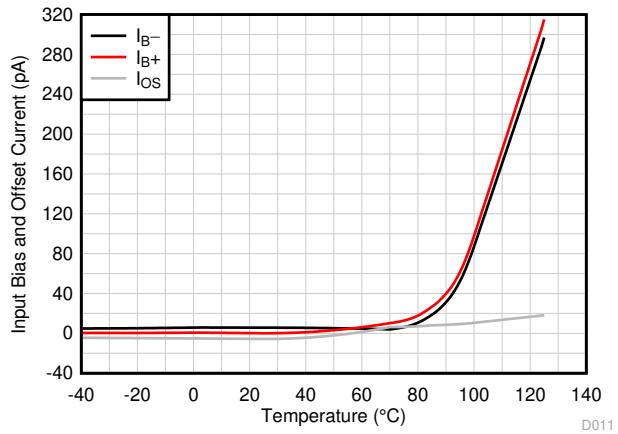


Figure 5-31. Input Bias Current vs Temperature (New Die)

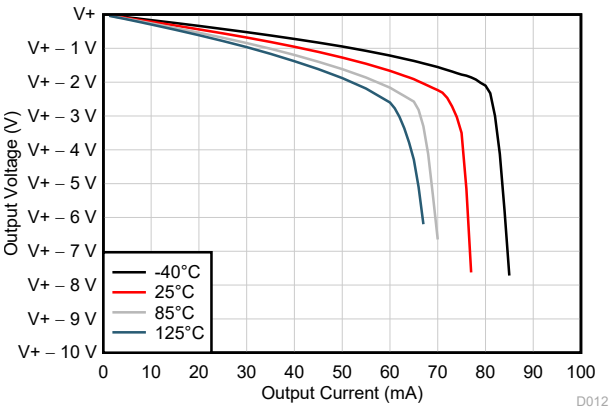


Figure 5-32. Output Voltage Swing vs Output Current (Sourcing) (New Die)

5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, connected to ground, unless otherwise noted.

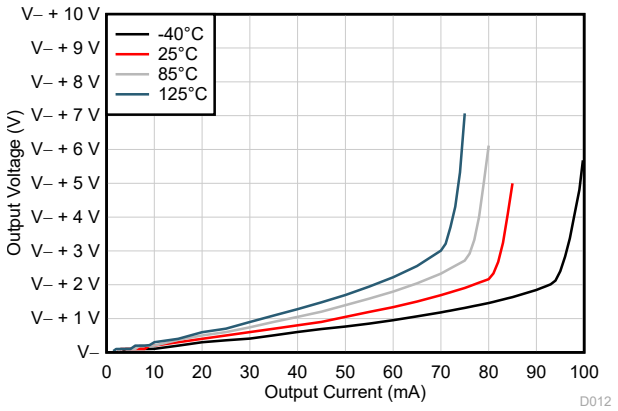


Figure 5-33. Output Voltage Swing vs Output Current (Sinking) (New Die)

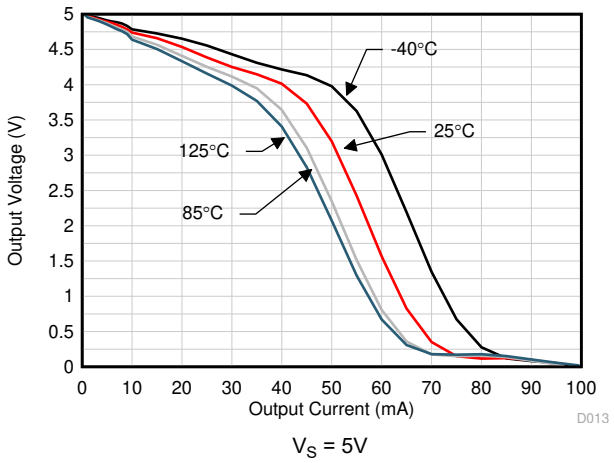


Figure 5-34. Output Voltage Swing vs Output Current (Sourcing) (New Die)

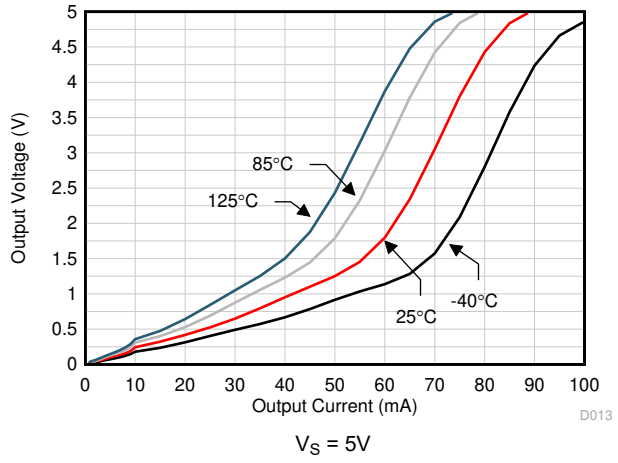


Figure 5-35. Output Voltage Swing vs Output Current (Sinking) (New Die)

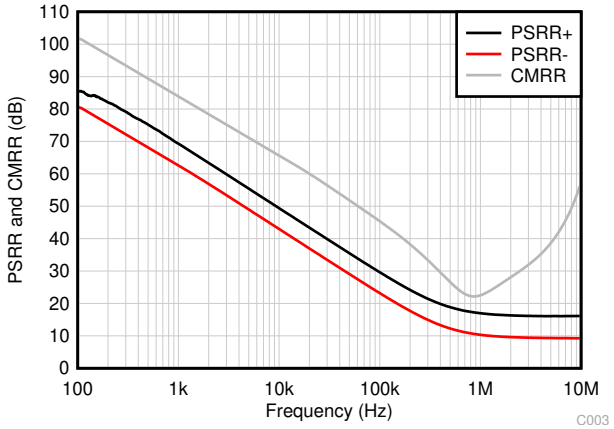


Figure 5-36. CMRR and PSRR vs Frequency (New Die)

5.6 Old Die to New Die Transition

As of the publication of revision A of this data sheet, Texas Instruments has moved manufacturing of the die for OPAX137 to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die (current fabrication site). The die origin can be separated from the “Chip Source Origin” (CSO) parameter in the shipping information. The old die CSO is “SFAB”, for the new die the CSO is “RFB”. The old die information is maintained in this data sheet for comparison purposes, but all new manufacturing has moved to the new die.

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6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

OPA137 series op amps are unity-gain stable and designed for a wide range of general-purpose applications. Power supply pins can be bypassed with 10nF ceramic capacitors or larger. All circuitry is completely independent in dual and quad versions, provides normal performance when one amplifier in a package is over-driven or short circuited. Many key parameters are maintained over the specified temperature range, –40°C to +85°C.

6.1.1 Operating Voltage

OPA137 op amps can be operated on power supplies as low as ±2.25 V. Performance remains excellent with power supplies ranging from ±2.25 V to ±18 V (+4.5 V to +36 V single supply). Most parameters vary only slightly throughout this supply voltage range. Quiescent current and short-circuit current vs supply voltage are shown in Section 5.5.

Operation at very low supply voltage (V_S ≤ ±3 V) requires careful attention to ensure that the common-mode voltage remains within the linear range, V_{CM} = (V–)+3 V to (V+). Inputs may need to be biased above ground in accordance with the common-mode voltage range restrictions for linear operation.

6.1.2 Input Voltage

The input common-mode voltage range of OPA137 series op amps extends from (V–)+3V to the positive rail, V+. For normal operation, inputs can be limited to this range. The inputs can go beyond the power supplies without output phase-reversal. Many FET-input op amps (such as TL061 types) exhibit phase-reversal of the output when the input common-mode range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications.

Input terminals are diode-clamped to the power supply rails for ESD protection. If the input voltage can exceed the negative supply by 500mV, input current can be limited to 2mA (or less). If the input current is not adequately limited, you can see unpredictable behavior in the other amplifiers in the package. This is easily accomplished with an input resistor as shown in Figure 6-1. Many input signals are inherently current-limited, therefore, a limiting resistor can not be neglected.

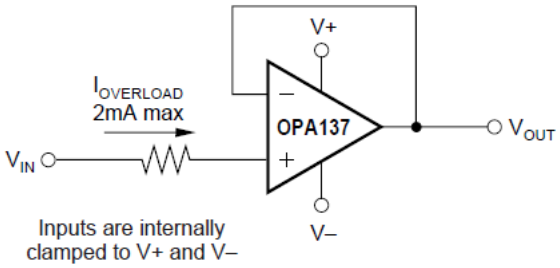

Figure 6-1. Input Current Protection for Voltages Exceeding the Supply Voltage

6.1.3 High-Side Current Sensing

Many applications require the sensing of signals near the positive supply. The common-mode input range of OPA137 op amps includes the positive rail, enabling them to be used to sense power supply currents as shown in Figure 6-2.

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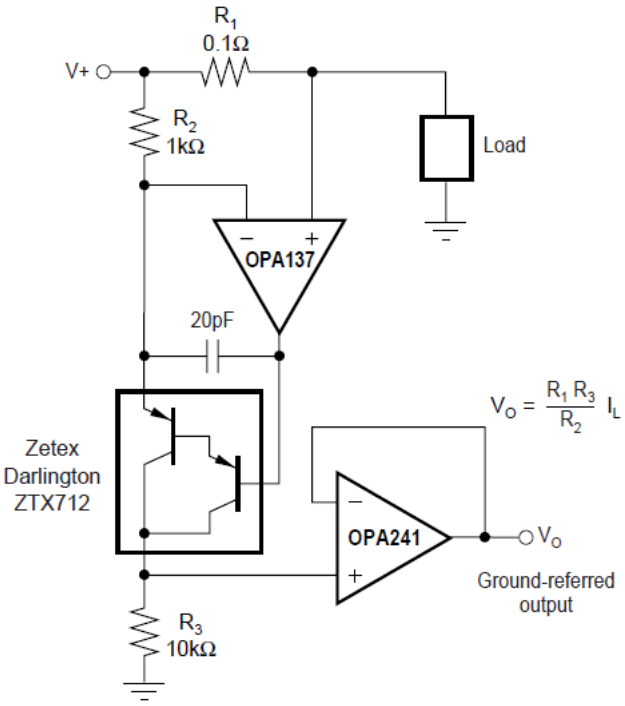

Figure 6-2. High-Side Current Monitor

6.1.4 Input Bias Current

The input bias current is approximately 5pA at room temperature and increases with temperature as shown in the typical performance curve Figure 5-5.

Input Bias current also varies with common-mode voltage and power supply voltage. This variation is dependent on the voltage between the negative power supply and the common-mode input voltage. The effect is shown in the typical performance curve Figure 5-6.

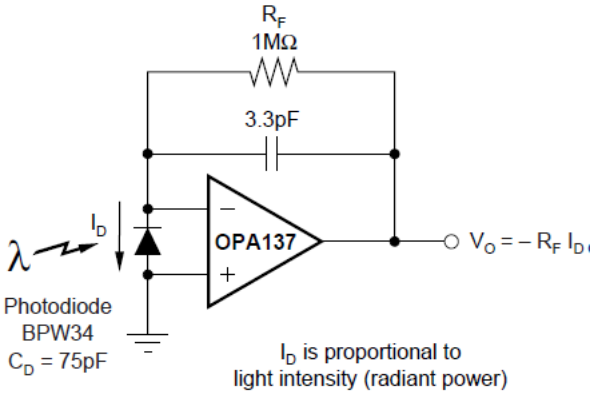

Figure 6-3. Photo-detector Amplifier

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7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 1998) to Revision A (March 2026)	Page
• Updated FET Input from IB = 5pA to IB = ± 10pA	1
• Updated Low offset voltage from 1.5mV to ±300mV	1
• Updated Low quiescent current from 220µA/channel to 120µA/channel	1
• Updated Excellent speed/power from 1MHz to 1.1MHz	1
• Updated Low input bias current from 5pA to ±10pA	1
• Updated Low quiescent current from 220µA to 120µA	1
• Updated High open-loop gain from 94dB to 145dB	1
• Updated High slew rate from 3.5V/ms to (4.5V/ms)	1
• Added Block diagram and package information	1
• Updated Input voltage noise from 2µVp-p to 6µVp-p	5
• Updated Input offset voltage from ±1.5mV and ±2.5mV to ±0.3mV	5
• Updated Input offset voltage vs Temperature from ±15mV/°C to ±0.6mV/°C	5
• Updated PSRR from ±90µV/V to ±0.1µV/V	5
• Updated Channel Separation (dual, quad) from 0.6µV/V to 5µV/V	5
• Updated Input bias current from 5pA to 10pA	5
• Updated Input offset current from 2pA to 5pA	5
• Updated Input Voltage Noise from 2µVp-p to 6µVp-p	5
• Updated Input Voltage Noise Density from 45nV/$\sqrt{Hz}$ to 30nV/$\sqrt{Hz}$	5
• Updated Input offset current from 1.2fA/$\sqrt{Hz}$to 2fA/$\sqrt{Hz}$	5
• Updated Gain-Bandwidth Product from 1MHz to 1.1MHz	5
• Updated Slew Rate from 3.5V/µs to 4.5V/µs	5
• Updated Settling Time at 0.1% from 8µs to 4µs	5
• Updated Settling Time at 0.01% from 10µs to 5µs	5
• Updated Total Harmonic Distortion + Noise from 0.05% to 0.02%	5
• Updated Capacitive Load Drive from 1000pF to 330pF	5
• Updated Quiescent Current from ±220µA to ±120µAOpen-loop output impedance	5
• Added Open-loop output impedance value 575Ω	5
• Updated New die typical characteristics plots	6
• Added New and old die to new die transition	12
• Deleted Recommended SOT-23-5 and MSOP-8 Solder Footprints	14

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA137N/250	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	E37
OPA137N/3K	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	E37
OPA137N/3K.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	E37
OPA137NA/250	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	E37
OPA137NA/3K	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	E37
OPA137NA/3K.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	E37
OPA137U	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 137U
OPA137U.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 137U
OPA137UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 137U A
OPA137UA.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 137U A
OPA137UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	(137UA, OPA) 137U A
OPA137UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	(137UA, OPA) 137U A
OPA2137E/250	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 85	E37
OPA2137E/2K5	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	E37
OPA2137E/2K5.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	E37
OPA2137EA/250	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 85	E37
OPA2137EA/2K5	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	E37
OPA2137EA/2K5.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	E37
OPA2137P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2137P
OPA2137P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2137P

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2137PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	(OPA2137P, OPA2137 PA) A
OPA2137PA.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	(OPA2137P, OPA2137 PA) A
OPA2137U	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 2137U
OPA2137U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	(2137U, OPA)
OPA2137U/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	(2137U, OPA)
OPA2137UA	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 2137U A
OPA2137UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	(2137UA, OPA) 2137U A
OPA2137UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	(2137UA, OPA) 2137U A
OPA4137P	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	OPA4137P
OPA4137P.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	OPA4137P
OPA4137PA	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	OPA4137P A
OPA4137PA.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	OPA4137P A
OPA4137PAG4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	OPA4137P A
OPA4137U	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	OPA4137U
OPA4137U/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	OPA4137U
OPA4137U/2K5.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	OPA4137U
OPA4137UA	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	OPA4137U A
OPA4137UA/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	(OPA4137U, OPA4137 UA) A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4137UA/2K5.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	(OPA4137U, OPA4137 UA) A

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

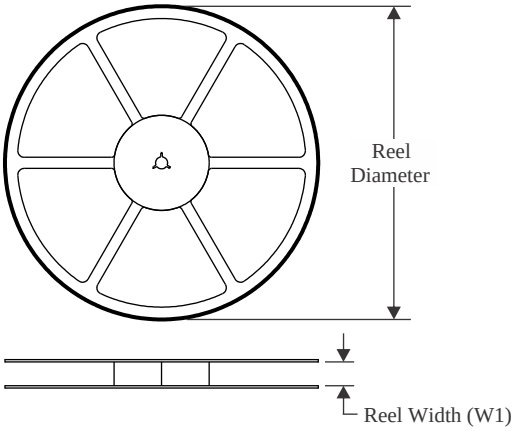
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

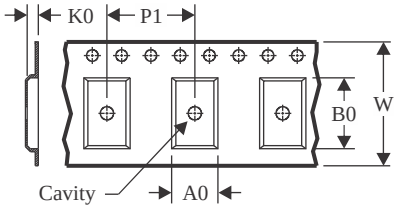
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

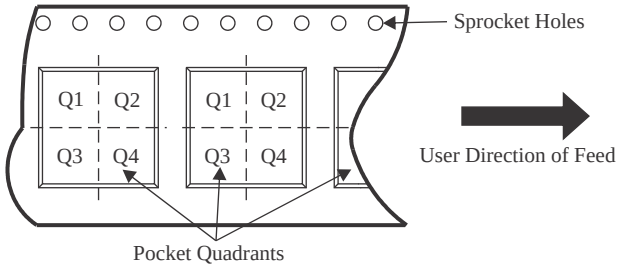


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

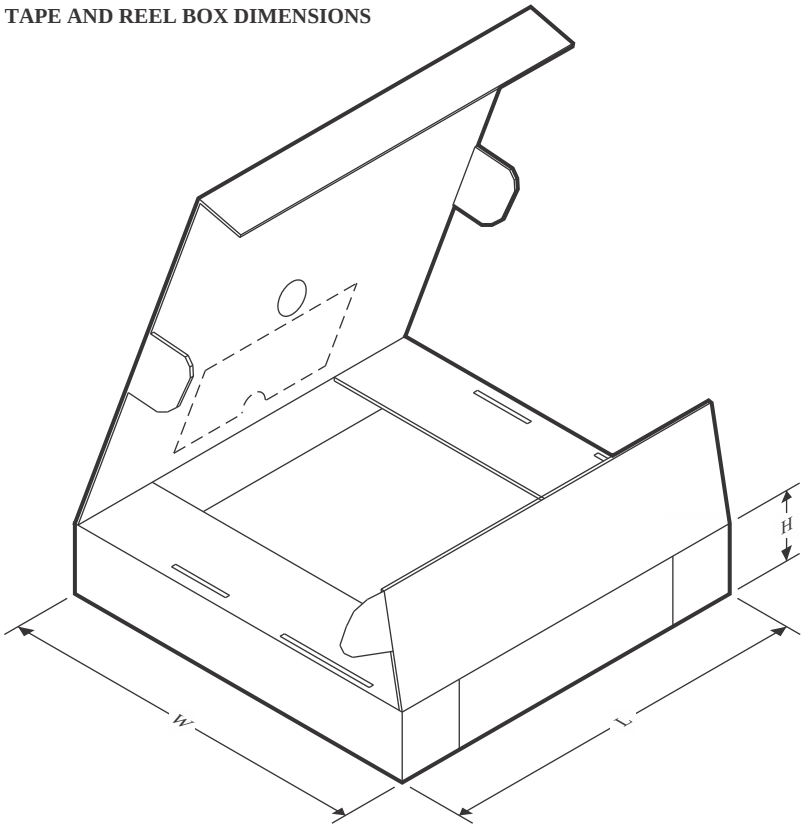
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA137N/3K	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA137N/3K	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA137N/3K	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA137NA/3K	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA137UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2137E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2137EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2137U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2137UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4137U/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4137UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

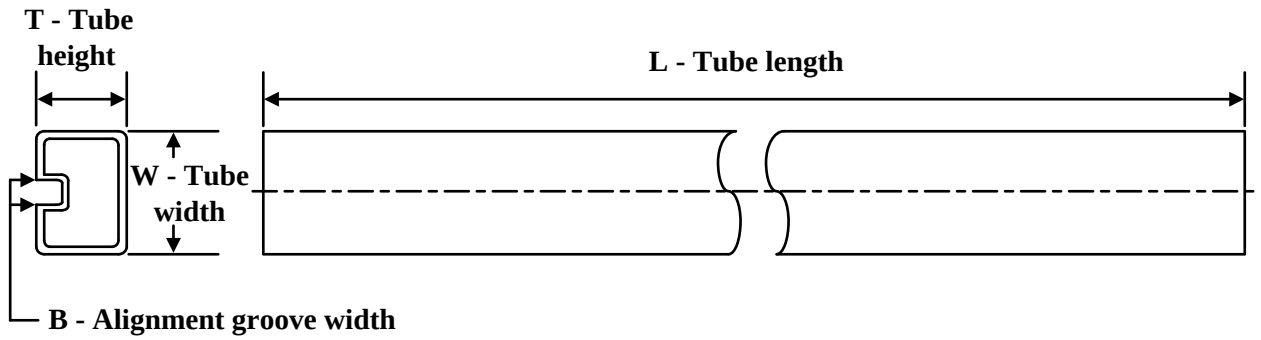
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA137N/3K	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA137N/3K	SOT-23	DBV	5	3000	208.0	191.0	35.0
OPA137N/3K	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA137NA/3K	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA137UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2137E/2K5	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2137EA/2K5	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2137U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2137UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA4137U/2K5	SOIC	D	14	2500	353.0	353.0	32.0
OPA4137UA/2K5	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA137U	D	SOIC	8	75	506.6	8	3940	4.32
OPA137U.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA137UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA137UA.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2137P	P	PDIP	8	50	506	13.97	11230	4.32
OPA2137P.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA2137PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2137PA.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA4137P	N	PDIP	14	25	506	13.97	11230	4.32
OPA4137P.A	N	PDIP	14	25	506	13.97	11230	4.32
OPA4137PA	N	PDIP	14	25	506	13.97	11230	4.32
OPA4137PA.A	N	PDIP	14	25	506	13.97	11230	4.32
OPA4137PAG4	N	PDIP	14	25	506	13.97	11230	4.32

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