LMH664x Low Power, 130 MHz, 75 mA Rail-to-Rail Output Amplifiers

1 Features

(V_S = ±5 V, T_A = 25°C, R_L = 2 kΩ, A_V = +1. Typical Values Unless Specified).

- −3 dB BW (A_V = +1) 130 MHz
- Supply Voltage Range 2.7 V to 12.8 V
- Slew Rate, (A_V = −1) 130V/µs(1)
- Supply Current (no load) 2.7 mA/amp
- Output Short Circuit Current +115 mA to 145 mA
- Linear Output Current ±75 mA
- Input Common Mode Volt. 0.5 V Beyond V^-, 1 V from V^+
- Output Voltage Swing 40 mV from Rails
- Input Voltage Noise (100 kHz) 17nV/$\sqrt{Hz}$
- Input Current Noise (100 kHz) 0.9pA/$\sqrt{Hz}$
- THD (5MHz, R_L = 2kΩ, V_O = $2V_{PP}$, A_V = +2) −62 dBc
- Settling Time 68 ns
- Fully Characterized for 3 V, 5 V, and ±5 V
- Overdrive Recovery 100 ns
- Output Short Circuit Protected(2)
- No Output Phase Reversal with CMVR Exceeded

(1) Slew rate is the average of the rising and falling slew rates

(2) Output short circuit duration is infinite for V_S < 6 V at room temperature and below. For V_S > 6 V, allowable short circuit duration is 1.5 ms.

2 Applications

- Active Filters
- CD/DVD ROM
- ADC Buffer Amp
- Portable Video
- Current Sense Buffer

3 Description

The LMH664X family true single supply voltage feedback amplifiers offer high speed (130 MHz), low distortion (−62 dBc), and exceptionally high output current (approximately 75 mA) at low cost and with reduced power consumption when compared against existing devices with similar performance.

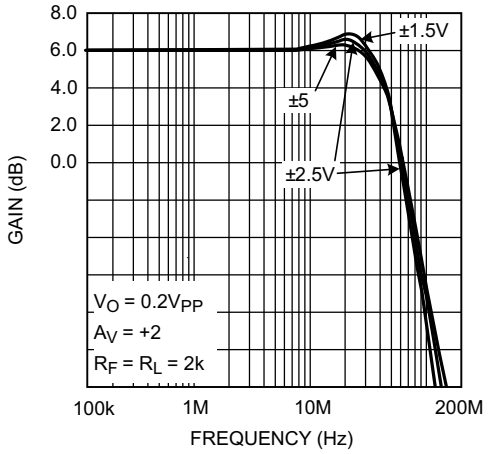
Input common mode voltage range extends to 0.5 V below V^- and 1 V from V^+. Output voltage range extends to within 40 mV of either supply rail, allowing wide dynamic range especially desirable in low voltage applications. The output stage is capable of approximately 75 mA in order to drive heavy loads. Fast output Slew Rate (130 V/µs) ensures large peak-to-peak output swings can be maintained even at higher speeds, resulting in exceptional full power bandwidth of 40 MHz with a 3 V supply. These characteristics, along with low cost, are ideal features for a multitude of industrial and commercial applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6642	SOT-23 (5)	2.90 mm × 1.60 mm
	SOIC (8)	4.90 mm × 3.91 mm
LMH6643	SOIC (8)	3.00 mm × 3.00 mm
	VSSOP (8)	
LMH6644	SOIC (14)	8.64 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Closed Loop Gain vs. Frequency for Various Supplies



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (March 2013) to Revision Q **Page**

- Added, revised, or updated the following sections: Device Information Table, Application and Implementation; Power Supply Recommendations; Device and Documentation Support; Mechanical, Packaging, and Ordering Information ... 1
- Changed "Junction Temperature Range" to "Operating Temperature Range" ... 5
- Deleted T_J = 25°C for Electrical Characteristics tables. ... 6
- Changed from "R_L " to "Rf" ... 6
- Deleted T_J = 25°C for Typical Performance Characteristics ... 12

Changes from Revision O (March 2013) to Revision P **Page**

- Changed layout of National Data Sheet to TI format ... 1

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5 Description (continued)

Careful attention has been paid to ensure device stability under all operating voltages and modes. The result is a very well behaved frequency response characteristic (0.1dB gain flatness up the 12 MHz under 150 Ω load and A_V = +2) with minimal peaking (typically 2dB maximum) for any gain setting and under both heavy and light loads. This along with fast settling time (68ns) and low distortion allows the device to operate well in an ADC buffer as well as high frequency filter applications.

This device family offers professional quality video performance with low DG (0.01%) and DP (0.01°) characteristics. Differential Gain and Differential Phase characteristics are also well maintained under heavy loads (150 Ω) and throughout the output voltage range. The LMH664X family is offered in single (LMH6642), dual (LMH6643), and quad (LMH6644) options.

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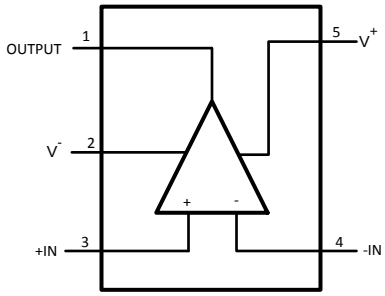
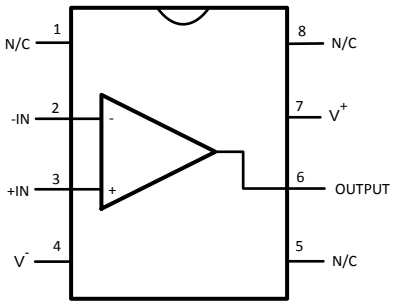
6 Pin Configuration and Functions

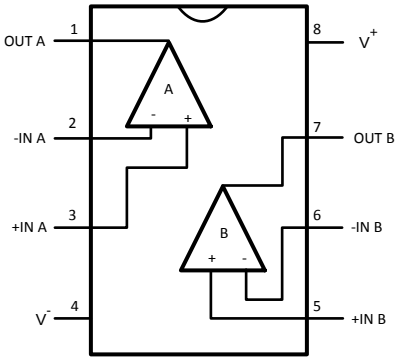
5-Pin SOT-23 (LMH6642)
Package DBV05A
Top View



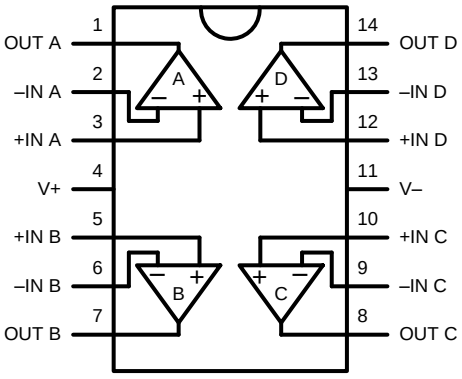
8-Pin SOIC (LMH6642)
Package D08A
Top View



8-Pin SOIC and VSSOP (LMH6643)
Package DGK08A
Top View



14-Pin SOIC and 14-Pin TSSOP (LMH6644)
Package D14A, PW14A
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	LMH6642		LMH6643	LMH6644		
	DBV05A	D08A	DGK08A	D14A and PW14A		
-IN	4	2			I	Inverting Input
+IN	3	3			I	Non-inverting Input
-IN A			2	2	I	ChA Inverting Input
+IN A			3	3	I	ChA Non-inverting Input
-IN B			6	6	I	ChB Inverting Input
+IN B			5	5	I	ChB Non-inverting Input
-IN C				9	I	ChC Inverting Input
+IN C				10	I	ChC Non-inverting Input
-IN D				13	I	ChD Inverting Input
+IN D				12	I	ChD Non-inverting Input
N/C		1,5,8			—	No connection
OUT A			1	1	O	ChA Output
OUT B			7	7	O	ChB Output
OUT C				8	O	ChC Output
OUT D				14	O	ChD Output
OUTPUT	1	6			O	Output
V^-	2	4	4	11	I	Negative Supply
V^+	5	7	8	4	I	Positive Supply

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7 Specifications

7.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN} Differential			±2.5	V
Output Short Circuit Duration			See (3) and (4)	
Supply Voltage (V^+ - V^-)			13.5	V
Voltage at Input/Output pins			V^+ +0.8 V^- −0.8	V
Input Current			±10	mA
Junction Temperature(5)			+150	°C
Soldering Information	Infrared or Convection Reflow (20 sec)		235	°C
	Wave Soldering Lead Temp.(10 sec)		260	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	+150	°C
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)		2000	V
		Machine model (MM)(3)		200	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(4)		1000	

(1) Human body model, 1.5 kΩ in series with 100 pF. Machine Model, 0 Ω in series with 200 pF.
(2) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process.
(4) JEDEC document JEP157 states that 1000-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V^+ – V^-)	2.7	12.8	V
Operating Temperature Range(2)	−40	+85	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

7.4 Thermal Information

THERMAL METRIC(1)		LMH6642		LMH6643	LMH6644		UNIT
		DBV05A	D08A	DGK08A	D14A	PW14A	
		5 PINS	8 PINS	8 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient Thermal Resistance(2)	265	190	235	145	155	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

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7.5 3V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to $V^+/2$.

PARAMETER		TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$, V_{ID} R_L = 2 kΩ to $V^+/2$			UNIT
			MIN	TYP	MAX	MIN (1)	TYP (2)	MAX (1)	
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV$_{PP}$				80	115		MHz
		A_V = +2, −1, V_{OUT} = 200mV$_{PP}$					46		
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, Rf = 402Ω, V_{OUT} = 200mV$_{PP}$					19		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = 1V$_{PP}$					40		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz					17		nV/√Hz
		f = 1kHz					48		
i_n	Input-Referred Current Noise	f = 100kHz					0.90		pA/√Hz
		f = 1kHz					3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = −1, R_L = 100Ω to $V^+/2$					−48		dBc
DG	Differential Gain	V_{CM} = 1V, NTSC, A_V = +2 R_L =150Ω to $V^+/2$					0.17%		
		R_L =1kΩ to $V^+/2$					0.03%		
DP	Differential Phase	V_{CM} = 1V, NTSC, A_V = +2 R_L =150Ω to $V^+/2$					0.05		deg
		R_L =1kΩ to $V^+/2$					0.03		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2					47		dB
T_S	Settling Time	V_O = 2V$_{PP}$, ±0.1%, 8pF Load, V_S = 5V					68		ns
SR	Slew Rate (3)	A_V = −1, V_I = 2V$_{PP}$				90	120		V/µs
V_{OS}	Input Offset Voltage	For LMH6642 and LMH6644			±7		±1	±5	mV
		For LMH6643			±7		±1	±3.4	
TC V_{OS}	Input Offset Average Drift	See (4)					±5		µV/°C
I_B	Input Bias Current	See (5)			−3.25		−1.50	−2.60	µA
I_{OS}	Input Offset Current				1000		20	800	nA
R_{IN}	Common Mode Input Resistance						3		MΩ

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

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3V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = 3V, V^- = 0V, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to $V^+/2$.

PARAMETER		TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 3V, V^- = 0V, $V_{CM} = V_O = V^+/2$, V_{ID} R_L = 2 kΩ to $V^+/2$			UNIT
			MIN	TYP	MAX	MIN (1)	TYP (2)	MAX (1)	
C_{IN}	Common Mode Input Capacitance						2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB			−0.1		−0.5	−0.2	V
			1.6			1.8	2.0		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 1.5V				72	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 2.5V R_L = 2kΩ to $V^+/2$	75			80	96		dB
		V_O = 0.5V to 2.5V R_L = 150Ω to $V^+/2$	70			74	82		
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$, V_{ID} = 200mV				2.90	2.98		V
		R_L = 150Ω to $V^+/2$, V_{ID} = 200mV				2.80	2.93		
	Output Swing Low	R_L = 2kΩ to $V^+/2$, V_{ID} = −200mV					25	75	mV
		R_L = 150Ω to $V^+/2$, V_{ID} = −200mV					75	150	
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$ V_{ID} = 200mV (6)	35			50	95		mA
		Sinking to $V^+/2$ V_{ID} = −200mV (6)	40			55	110		
I_{OUT}	Output Current	V_{OUT} = 0.5V from either supply					±65		mA
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 3.0V to 3.5V, V_{CM} = 1.5V				75	85		dB
I_S	Supply Current (per channel)	No Load			4.50		2.70	4.00	mA

(6) Short circuit test is a momentary test. See Note 7 under 5 V Electrical Characteristics.

7.6 5V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to $V^+/2$.

PARAMETER		TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, V_{ID} R_L = 2kΩ to $V^+/2$			UNIT
			MIN	TYP	MAX	MIN(1)	TYP(2)	MAX(1)	
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV$_{PP}$				90	120		MHz
		A_V = +2, −1, V_{OUT} = 200mV$_{PP}$					46		
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, R_f = 402Ω, V_{OUT} = 200mV$_{PP}$					15		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = 2V$_{PP}$					22		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz					17		nV/√Hz
		f = 1kHz					48		
i_n	Input-Referred Current Noise	f = 100kHz					0.90		pA/√Hz
		f = 1kHz					3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = +2					−60		dBc
DG	Differential Gain	NTSC, A_V = +2 R_L =150Ω to $V^+/2$					0.16%		
		R_L = 1kΩ to $V^+/2$					0.05%		
DP	Differential Phase	NTSC, A_V = +2 R_L = 150Ω to $V^+/2$					0.05		deg
		R_L = 1kΩ to $V^+/2$					0.01		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2					47		dB
T_S	Settling Time	V_O = 2V$_{PP}$, ±0.1%, 8pF Load					68		ns
SR	Slew Rate (3)	A_V = −1, V_I = 2V$_{PP}$				95	125		V/µs
V_{OS}	Input Offset Voltage	For LMH6642 and LMH6644			±7		±1	±5	mV
		For LMH6643			±7		±1	±3.4	
TC V_{OS}	Input Offset Average Drift	See (4)					±5		µV/°C
I_B	Input Bias Current	See (5)			−3.25		−1.70	−2.60	µA
I_{OS}	Input Offset Current				1000		20	800	nA
R_{IN}	Common Mode Input Resistance						3		MΩ
C_{IN}	Common Mode Input Capacitance						2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB			−0.1		−0.5	−0.2	V
			3.6			3.8	4.0		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.5V				72	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.50V R_L = 2kΩ to $V^+/2$	82			86	98		dB
		V_O = 0.5V to 4.25V R_L = 150Ω to $V^+/2$	72			76	82		

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

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5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to $V^+/2$.

PARAMETER		TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$, V_{ID} R_L = 2kΩ to $V^+/2$			UNIT
			MIN	TYP	MAX	MIN(1)	TYP(2)	MAX(1)	
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$, V_{ID} = 200mV				4.90	4.98		V
		R_L = 150Ω to $V^+/2$, V_{ID} = 200mV				4.65	4.90		
	Output Swing Low	R_L = 2kΩ to $V^+/2$, V_{ID} = −200mV					25	100	mV
		R_L = 150Ω to $V^+/2$, V_{ID} = −200mV					100	150	
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$ V_{ID} = 200mV (6)(7)	40			55	115		mA
		Sinking to $V^+/2$ V_{ID} = −200mV (6)(7)	55			70	140		
I_{OUT}	Output Current	V_O = 0.5V from either supply					±70		mA
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 4.0V to 6V				79	90		dB
I_S	Supply Current (per channel)	No Load			5.00		2.70	4.25	mA

(6) Short circuit test is a momentary test. See Note 7.
(7) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

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7.7 ±5V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to ground.

	PARAMETER	TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V, V_{ID}			UNIT
			MIN	TYP	MAX	MIN(1)	TYP(2)	MAX(1)	
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV$_{PP}$				95	130		MHz
		A_V = +2, −1, V_{OUT} = 200mV$_{PP}$					46		
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, R_f = 806Ω, V_{OUT} = 200mV$_{PP}$					12		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = 2V$_{PP}$					24		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz					17		nV/√Hz
		f = 1kHz					48		
i_n	Input-Referred Current Noise	f = 100kHz					0.90		pA/√Hz
		f = 1kHz					3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = +2					−62		dBc
DG	Differential Gain	NTSC, A_V = +2 R_L = 150Ω to V^+/2					0.15%		
		R_L = 1kΩ to V^+/2					0.01%		
DP	Differential Phase	NTSC, A_V = +2 R_L = 150Ω to V^+/2					0.04		deg
		R_L = 1kΩ to V^+/2					0.01		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2					47		dB
T_S	Settling Time	V_O = 2V$_{PP}$, ±0.1%, 8pF Load, V_S = 5V					68		ns
SR	Slew Rate (3)	A_V = −1, V_I = 2V$_{PP}$				100	135		V/µs
V_{OS}	Input Offset Voltage	For LMH6642 and LMH6644			±7		±1	±5	mV
		For LMH6643			±7		±1	±3.4	
TC V_{OS}	Input Offset Average Drift	See (4)					±5		µV/°C
I_B	Input Bias Current	See (5)			−3.25		−1.60	−2.60	µA
I_{OS}	Input Offset Current				1000		20	800	nA
R_{IN}	Common Mode Input Resistance						3		MΩ
C_{IN}	Common Mode Input Capacitance						2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB			−5.1		−5.5	−5.2	V
			3.6			3.8	4.0		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −5V to 3.5V				74	95		dB

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

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±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to ground.

PARAMETER		TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V, V_{ID}			UNIT
			MIN	TYP	MAX	MIN(1)	TYP(2)	MAX(1)	
A_{VOL}	Large Signal Voltage Gain	V_O = −4.5V to 4.5V, R_L = 2kΩ	84			88	96		dB
		V_O = −4.0V to 4.0V, R_L = 150Ω	74			78	82		
V_O	Output Swing High	R_L = 2kΩ, V_{ID} = 200mV				4.90	4.96		V
		R_L = 150Ω, V_{ID} = 200mV				4.65	4.80		
	Output Swing Low	R_L = 2kΩ, V_{ID} = −200mV					−4.96	−4.90	V
		R_L = 150Ω, V_{ID} = −200mV					−4.80	−4.65	
I_{SC}	Output Short Circuit Current	Sourcing to Ground V_{ID} = 200mV (6)(7)	35			60	115		mA
		Sinking to Ground V_{ID} = −200mV (6)(7)	65			85	145		
I_{OUT}	Output Current	V_O = 0.5V from either supply				±75			mA
PSRR	Power Supply Rejection Ratio	(V^+, V^-) = (4.5V, −4.5V) to (5.5V, −5.5V)				78	90		dB
I_S	Supply Current (per channel)	No Load			5.50		2.70	4.50	mA

(6) Short circuit test is a momentary test. See (7).
(7) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

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7.8 Typical Performance Characteristics

$V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2\ k\Omega$. Unless otherwise specified.

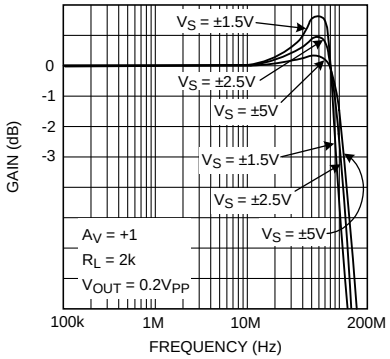

Figure 1. Closed Loop Frequency Response for Various Supplies

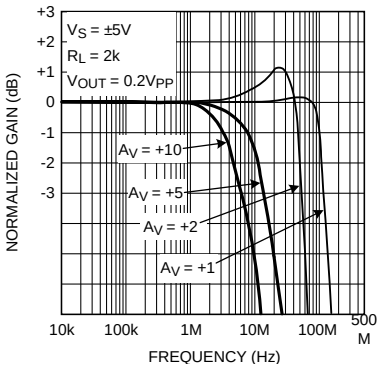

Figure 2. Closed Loop Gain vs. Frequency for Various Gain

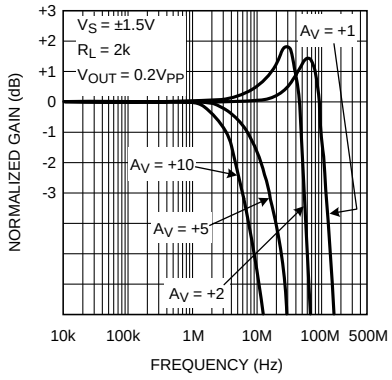

Figure 3. Closed Loop Gain vs. Frequency for Various Gain

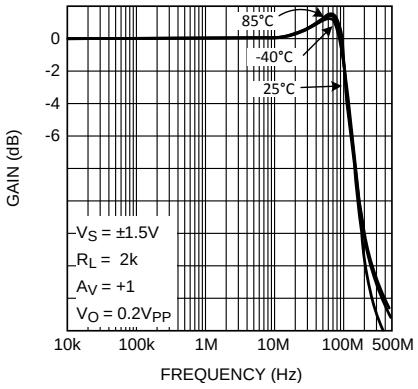

Figure 4. Closed Loop Frequency Response for Various Temperature

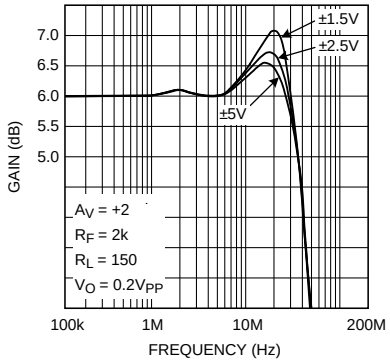

Figure 5. Closed Loop Gain vs. Frequency for Various Supplies

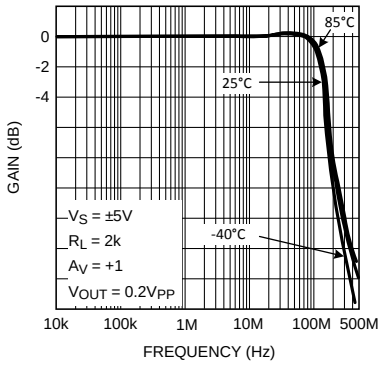

Figure 6. Closed Loop Frequency Response for Various Temperature

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Typical Performance Characteristics (continued)

$V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2\ k\Omega$. Unless otherwise specified.

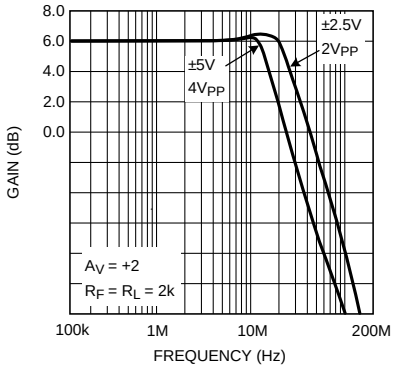

Figure 7. Large Signal Frequency Response

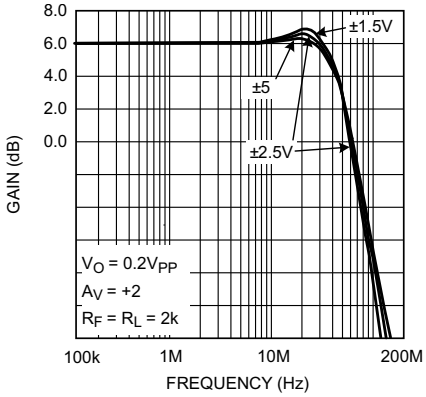

Figure 8. Closed Loop Small Signal Frequency Response for Various Supplies

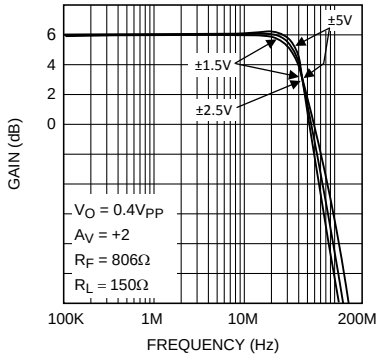

Figure 9. Closed Loop Frequency Response for Various Supplies

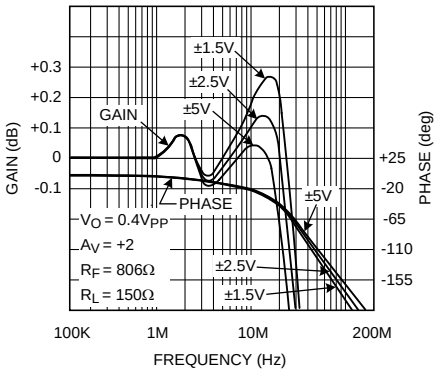

Figure 10. ±0.1dB Gain Flatness for Various Supplies

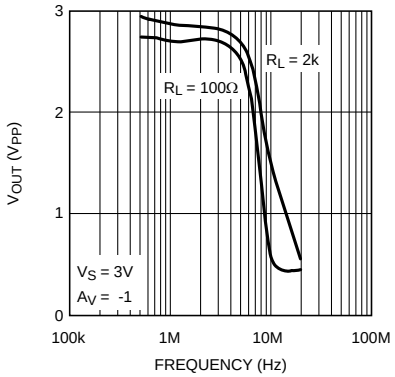

Figure 11. V_{OUT} (V_{PP}) for THD < 0.5%

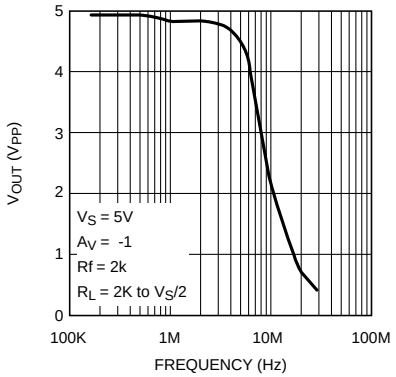

Figure 12. V_{OUT} (V_{PP}) for THD < 0.5%

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Typical Performance Characteristics (continued)

$V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2\ k\Omega$. Unless otherwise specified.

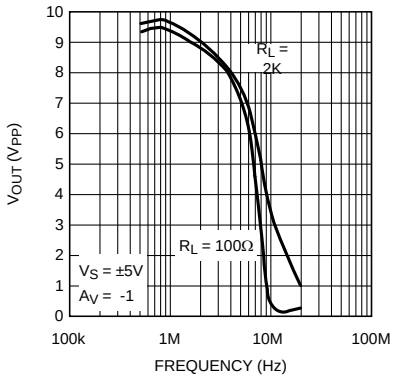

Figure 13. V_{OUT} (V_{PP}) for THD < 0.5%

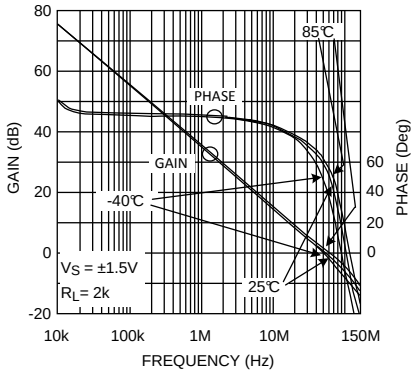

Figure 14. Open Loop Gain/Phase for Various Temperature

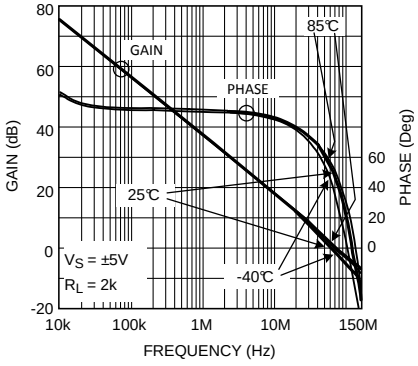

Figure 15. Open Loop Gain/Phase for Various Temperature

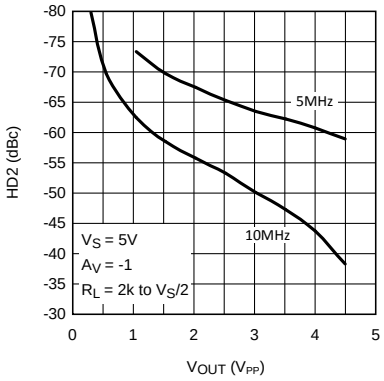

Figure 16. HD2 (dBc) vs. Output Swing

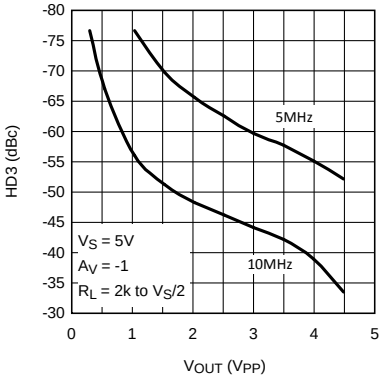

Figure 17. HD3 (dBc) vs. Output Swing

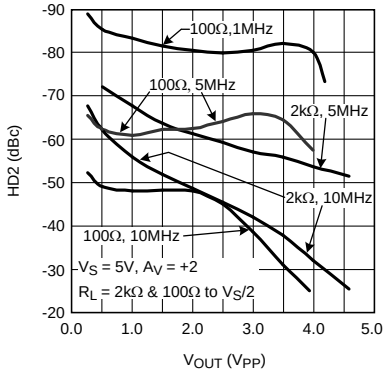

Figure 18. HD2 vs. Output Swing

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Typical Performance Characteristics (continued)

V^+ = +5, V^- = −5V, R_F = R_L = 2 kΩ. Unless otherwise specified.

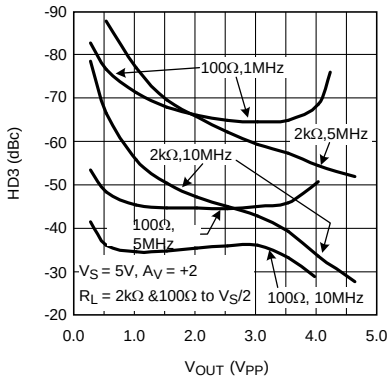

Figure 19. HD3 vs. Output Swing

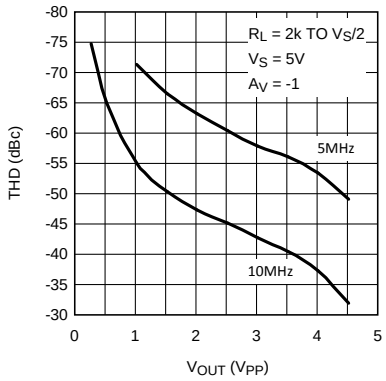

Figure 20. THD (dBc) vs. Output Swing

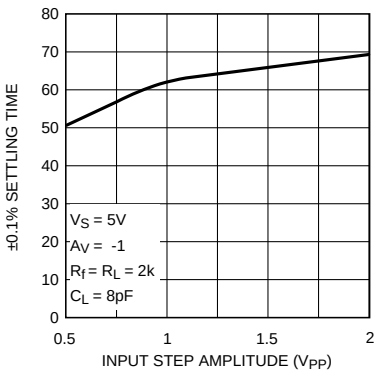

Figure 21. Settling Time vs. Input Step Amplitude (Output Slew and Settle Time)

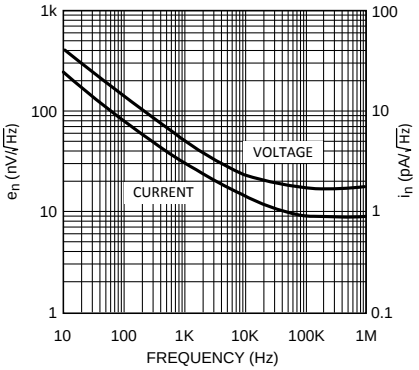

Figure 22. Input Noise vs. Frequency

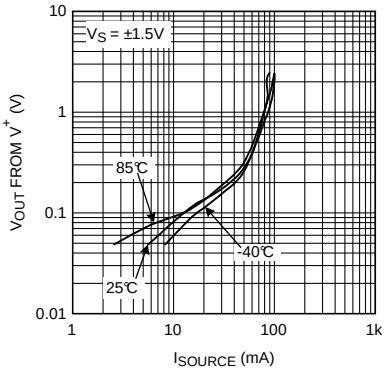

Figure 23. V_{OUT} from V^+ vs. I_{SOURCE}

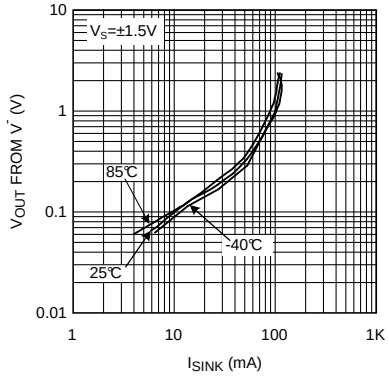

Figure 24. V_{OUT} from V^- vs. I_{SINK}

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Typical Performance Characteristics (continued)

$V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2\ k\Omega$. Unless otherwise specified.

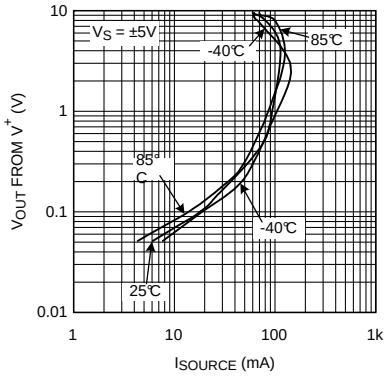

Figure 25. V_{OUT} from V^+ vs. I_{SOURCE}

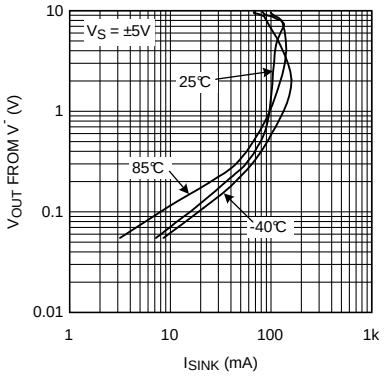

Figure 26. V_{OUT} from V^- vs. I_{SINK}

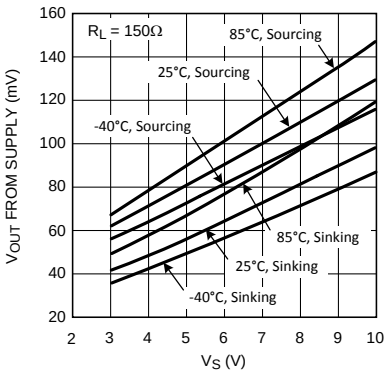

Figure 27. Swing vs. V_S

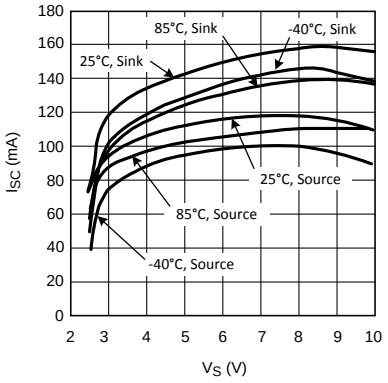

Figure 28. Short Circuit Current (to $V_S/2$) vs. V_S

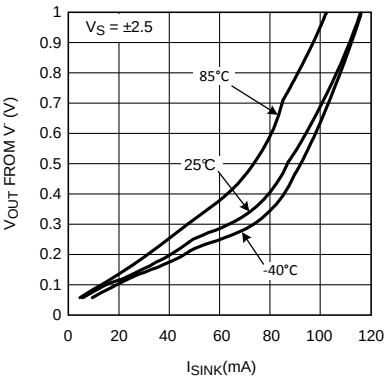

Figure 29. Output Sinking Saturation Voltage vs. I_{OUT}

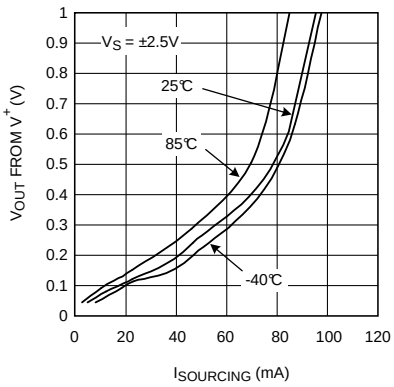

Figure 30. Output Sourcing Saturation Voltage vs. I_{OUT}

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Typical Performance Characteristics (continued)

V^+ = +5, V^- = −5V, R_F = R_L = 2 kΩ. Unless otherwise specified.

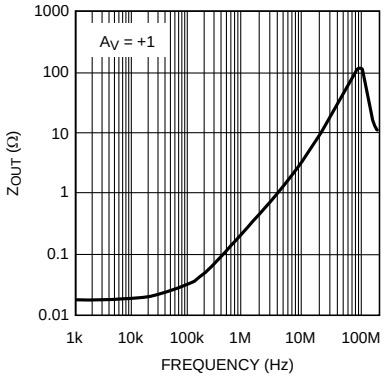

Figure 31. Closed Loop Output Impedance vs. Frequency A_V = +1

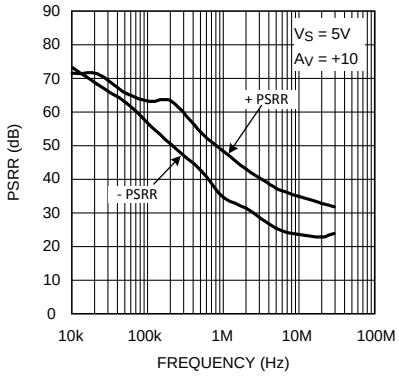

Figure 32. PSRR vs. Frequency

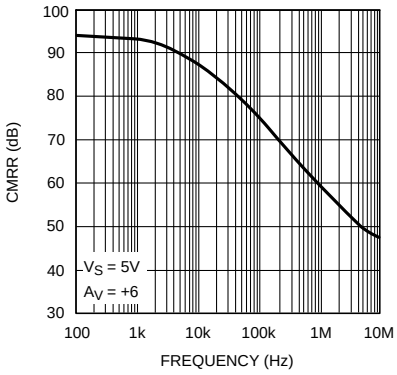

Figure 33. CMRR vs. Frequency

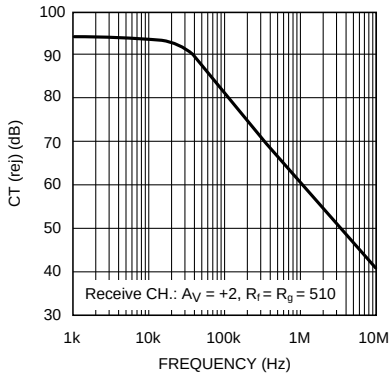

Figure 34. Crosstalk Rejection vs. Frequency (Output to Output)

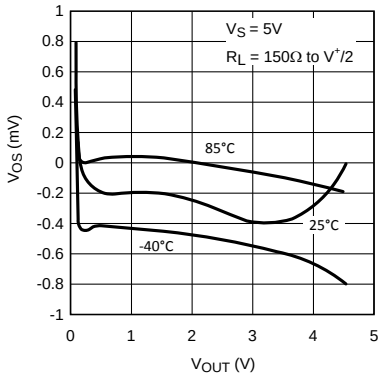

Figure 35. V_{OS} vs. V_{OUT} (Typical Unit)

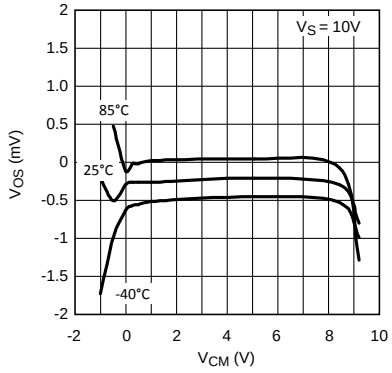

Figure 36. V_{OS} vs. V_{CM} (Typical Unit)

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Typical Performance Characteristics (continued)

V^+ = +5, V^- = −5V, R_F = R_L = 2 kΩ. Unless otherwise specified.

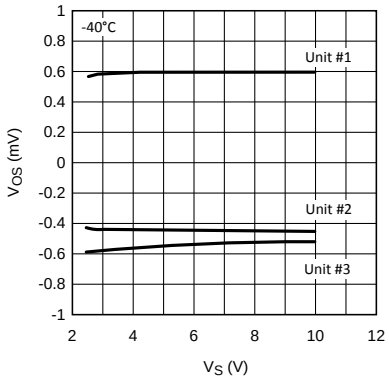

Figure 37. V_{OS} vs. V_S (for 3 Representative Units)

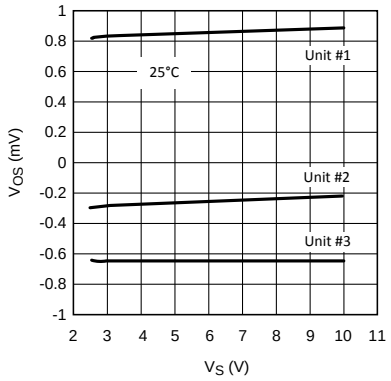

Figure 38. V_{OS} vs. V_S (for 3 Representative Units)

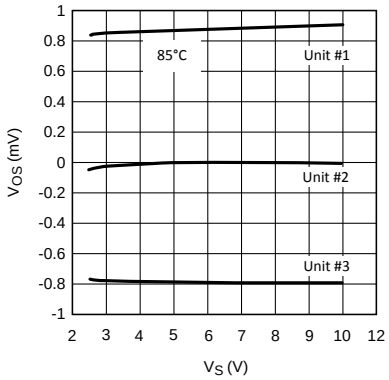

Figure 39. V_{OS} vs. V_S (for 3 Representative Units)

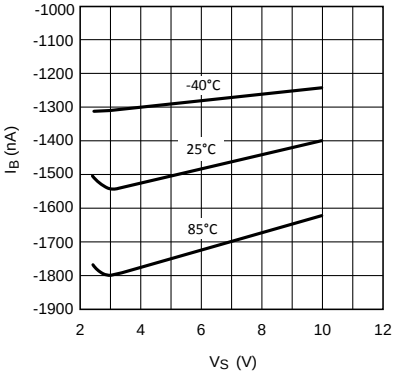

Figure 40. I_B vs. V_S

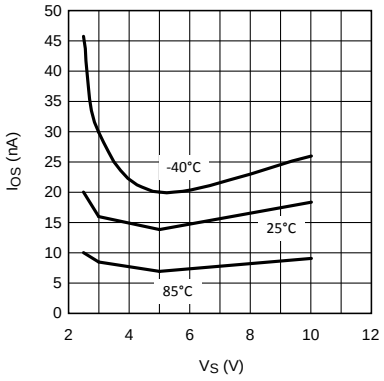

Figure 41. I_{OS} vs. V_S

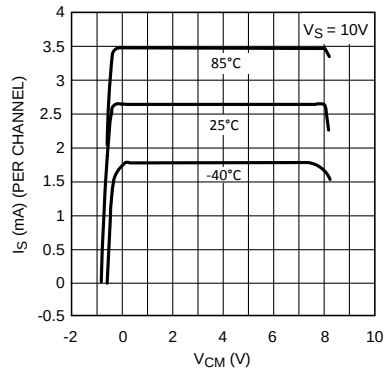

Figure 42. I_S vs. V_{CM}

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Typical Performance Characteristics (continued)

V^+ = +5, V^- = −5V, R_F = R_L = 2 kΩ. Unless otherwise specified.

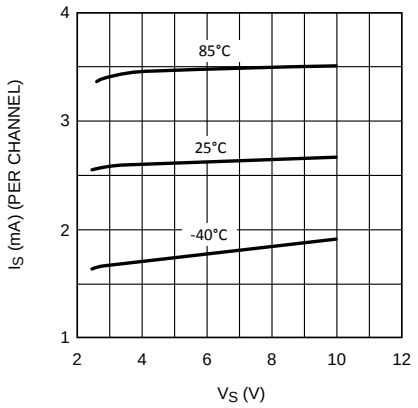

Figure 43. I_S vs. V_S

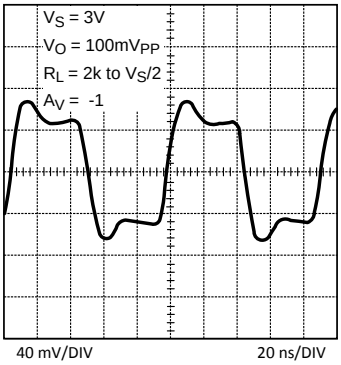

Figure 44. Small Signal Step Response

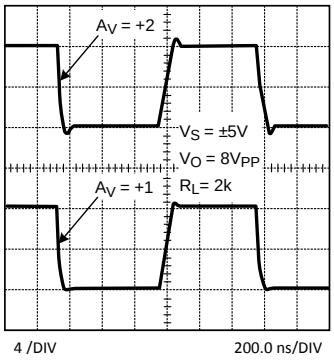

Figure 45. Large Signal Step Response

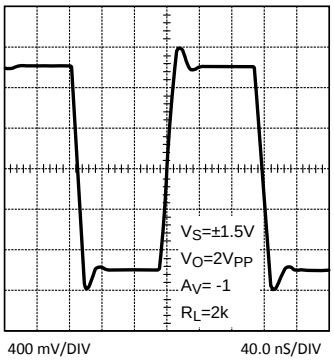

Figure 46. Large Signal Step Response

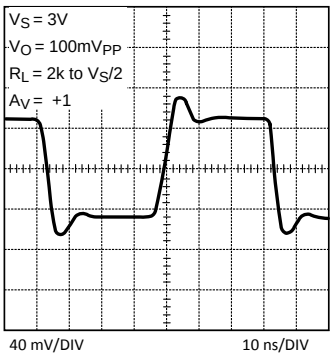

Figure 47. Small Signal Step Response

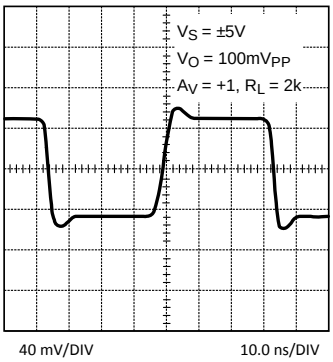

Figure 48. Small Signal Step Response

Typical Performance Characteristics (continued)

$V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2\ k\Omega$. Unless otherwise specified.

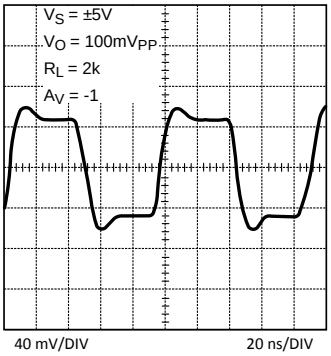

Figure 49. Small Signal Step Response

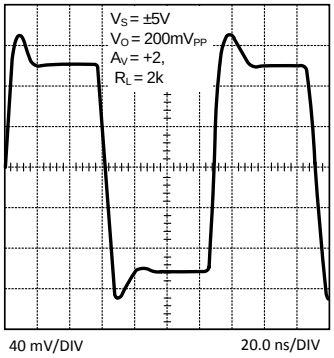

Figure 50. Small Signal Step Response

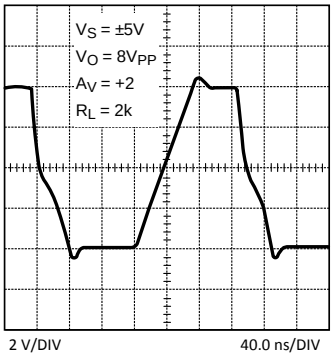

Figure 51. Large Signal Step Response

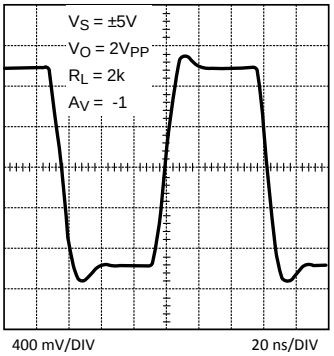

Figure 52. Large Signal Step Response

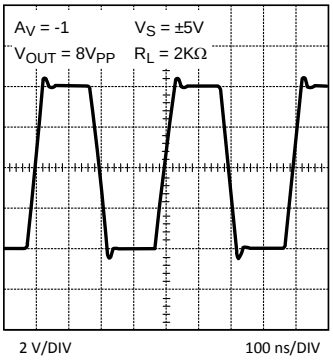

Figure 53. Large Signal Step Response

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8 Detailed Description

8.1 Overview

The LMH664X family is based on proprietary VIP10 dielectrically isolated bipolar process. This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8 GHz) even under low supply voltage (2.7 V) and low bias current.
- A class A-B "turn-around" stage with improved noise, offset, and reduced power dissipation compared to similar speed devices (patent pending).
- Common Emitter push-push output stage capable of 75 mA output current (at 0.5 V from the supply rails) while consuming only 2.7 mA of total supply current per channel. This architecture allows output to reach within mV of either supply rail.
- Consistent performance over the entire operating supply voltage range with little variation for the most important specifications (for example, BW, SR, I_{OUT}, and so forth)
- Significant power saving (~40%) compared to competitive devices on the market with similar performance.

8.2 Functional Block Diagram

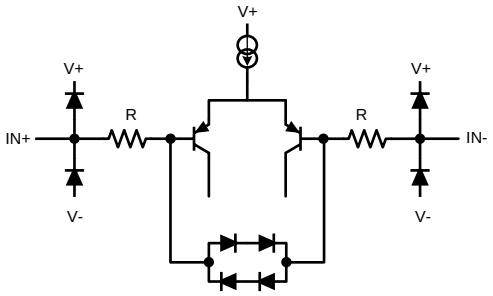

Figure 54. Input Equivalent Circuit

8.3 Feature Description

The LMH664X family is a drop-in replacement for the AD805X family of high speed Op Amps in most applications. In addition, the LMH664X will typically save about 40% on power dissipation, due to lower supply current, when compared to competition. All AD805X family's specified parameters are included in the list of LMH664X ensured specifications in order to ensure equal or better level of performance. However, as in most high performance parts, due to subtleties of applications, it is strongly recommended that the performance of the part to be evaluated is tested under actual operating conditions to ensure full compliance to all specifications.

8.4 Device Functional Modes

With 3-V supplies and a common mode input voltage range that extends 0.5 V below V^-, the LMH664X find applications in low voltage/low power applications. Even with 3-V supplies, the −3dB BW (@ A_V = +1) is typically 115 MHz with a tested limit of 80 MHz. Production testing guarantees that process variations will not compromise speed. High frequency response is exceptionally stable, confining the typical −3dB BW over the industrial temperature range to ±2.5%.

As seen in *Typical Performance Characteristics*, the LMH664X output current capability (~75 mA) is enhanced compared to AD805X. This enhancement increases the output load range, adding to the LMH664X's versatility. Since LMH664X is capable of high output current, device junction temperature should not to exceed the Absolute Maximum Ratings.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This device family was designed to avoid output phase reversal. With input overdrive, the output is kept near supply rail (or as closed to it as mandated by the closed loop gain setting and the input voltage). See Figure 56.

However, if the input voltage range of −0.5 V to 1 V from V^+ is exceeded by more than a diode drop, the internal ESD protection diodes will start to conduct. The current in the diodes should be kept at or below 10 mA.

Output overdrive recovery time is less than 100 ns as can be seen in Figure 57.

9.2 Typical Application

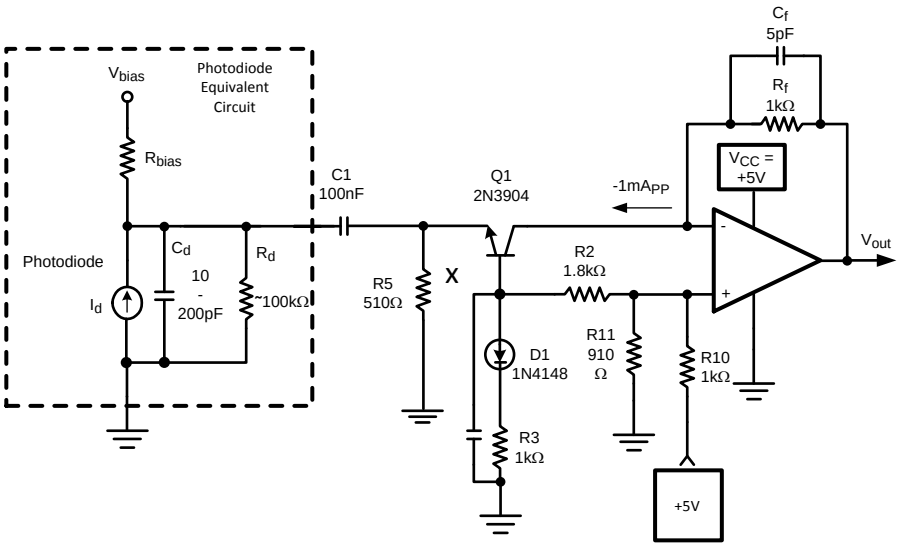

Figure 55. Single Supply Photodiode I-V Converter

9.2.1 Design Requirements

The circuit shown in Figure 55 is used to amplify the current from a photodiode into a voltage output. In this circuit, the emphasis is on achieving high bandwidth and the transimpedance gain setting is kept relatively low. Because of its high slew rate limit and high speed, the LMH664X family lends itself well to such an application. This circuit achieves approximately 1V/mA of transimpedance gain and capable of handling up to 1mApp from the photodiode. Q1, in a common base configuration, isolates the high capacitance of the photodiode (Cd) from the Op Amp input in order to maximize speed. Input is AC coupled through C1 to ease biasing and allow single supply operation. With 5-V single supply, the device input/output is shifted to near half supply using a voltage divider from VCC. Note that Q1 collector does not have any voltage swing and the Miller effect is minimized. D1, tied to Q1 base, is for temperature compensation of Q1's bias point. Q1 collector current was set to be large enough to handle the peak-to-peak photodiode excitation and not too large to shift the U1 output too far from mid-supply.

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Typical Application (continued)

9.2.1.1 Input and Output Topology

All input / output pins are protected against excessive voltages by ESD diodes connected to V^+ and V^- rails (see Figure 54). These diodes start conducting when the input / output pin voltage approaches $1V_{be}$ beyond V^+ or V^- to protect against over voltage. These diodes are normally reverse biased. Further protection of the inputs is provided by the two resistors (R in Figure 54), in conjunction with the string of anti-parallel diodes connected between both bases of the input stage. The combination of these resistors and diodes reduces excessive differential input voltages approaching $2V_{be}$. This occurs most commonly when the device is used as a comparator (or with little or no feedback) and the device inputs no longer follow each other. In such a case, the diodes may conduct. As a consequence, input current increases and the differential input voltage is clamped. It is important to make sure that the subsequent current flow through the device input pins does not violate the Absolute Maximum Ratings of the device. To limit the current through this protection circuit, extra series resistors can be placed. Together with the built-in series resistors of several hundred ohms, these external resistors can limit the input current to a safe number (that is, less than 10mA). Be aware that these input series resistors may impact the switching speed of the device and could slow down the device.

9.2.1.2 Single Supply, Low Power Photodiode Amplifier

The circuit shown in Figure 55 is used to amplify the current from a photodiode into a voltage output. In this circuit, the emphasis is on achieving high bandwidth and the transimpedance gain setting is kept relatively low. Because of its high slew rate limit and high speed, the LMH664X family lends itself well to such an application.

This circuit achieves approximately 1V/mA of transimpedance gain and capable of handling up to $1mA_{pp}$ from the photodiode. Q1, in a common base configuration, isolates the high capacitance of the photodiode (C_d) from the Op Amp input in order to maximize speed. Input is AC coupled through C1 to ease biasing and allow single supply operation. With 5V single supply, the device input/output is shifted to near half supply using a voltage divider from V_{CC}. Note that Q1 collector does not have any voltage swing and the Miller effect is minimized. D1, tied to Q1 base, is for temperature compensation of Q1's bias point. Q1 collector current was set to be large enough to handle the peak-to-peak photodiode excitation and not too large to shift the U1 output too far from mid-supply.

No matter how low an R_f is selected, there is a need for C_f in order to stabilize the circuit. The reason for this is that the Op Amp input capacitance and Q1 equivalent collector capacitance together (C_{IN}) will cause additional phase shift to the signal fed back to the inverting node. C_f will function as a zero in the feedback path counter-acting the effect of the C_{IN} and acting to stabilized the circuit. By proper selection of C_f such that the Op Amp open loop gain is equal to the inverse of the feedback factor at that frequency, the response is optimized with a theoretical 45° phase margin.

$$C_F = \sim \text{SQRT}\left[(C_{IN})/(2\pi \cdot \text{GBWP} \cdot R_F)\right] \quad (1)$$

where

- GBWP is the Gain Bandwidth Product of the Op Amp

Optimized as such, the I-V converter will have a theoretical pole, f_p, at:

$$f_P = \text{SQRT}\left[\text{GBWP}/(2\pi R_F \cdot C_{IN})\right] \quad (2)$$

With Op Amp input capacitance of 3pF and an estimate for Q1 output capacitance of about 3pF as well, C_{IN} = 6 pF. From the typical performance plots, LMH6642/6643 family GBWP is approximately 57 MHz. Therefore, with R_f = 1k, from Equation 1 and Equation 2:

$$C_f = \sim 4.1 \text{ pF and } f_p = 39 \text{ MHz} \quad (3)$$

For this example, optimum C_f was empirically determined to be around 5 pF. This time domain response is shown in Figure 58 below showing about 9 ns rise/fall times, corresponding to about 39 MHz for f_p. The overall supply current from the +5 V supply is around 5 mA with no load.

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Typical Application (continued)

9.2.2 Detailed Design Procedure

No matter how low an Rf is selected, there is a need for C_f in order to stabilize the circuit. The reason for this is that the Op Amp input capacitance and Q1 equivalent collector capacitance together (C_{IN}) will cause additional phase shift to the signal fed back to the inverting node. C_f will function as a zero in the feedback path counteracting the effect of the C_{IN} and acting to stabilized the circuit. By proper selection of C_f such that the Op Amp open loop gain is equal to the inverse of the feedback factor at that frequency, the response is optimized with a theoretical 45° phase margin where GBWP is the Gain Bandwidth Product of the Op Amp, Optimized as such, the I-V converter will have a theoretical pole, fp, at: (2) With Op Amp input capacitance of 3pF and an estimate for Q1 output capacitance of about 3pF as well, C_{IN} = 6 pF. From the typical performance plots, LMH6642/6643 family GBWP is approximately 57 MHz. Therefore, with Rf = 1k, from Equation 2 and Equation 3 : C_f = ~4.1 pF and fp = 39 MHz.

Single Supply Photodiode I-V Converter For this example, optimum C_f was empirically determined to be around 5 pF. This time domain response is shown in Figure 58 showing about 9 ns rise/fall times, corresponding to about 39 MHz for fp. The overall supply current from the +5 V supply is around 5 mA with no load.

9.2.3 Application Curves

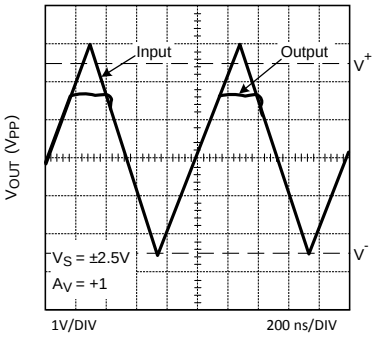

Figure 56. Input and Output Shown with CMVR Exceeded

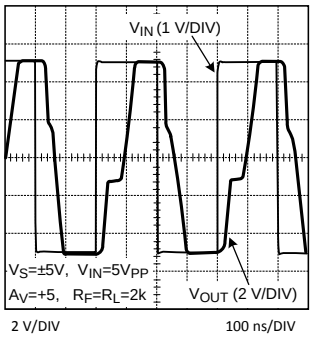

Figure 57. Overload Recovery Waveform

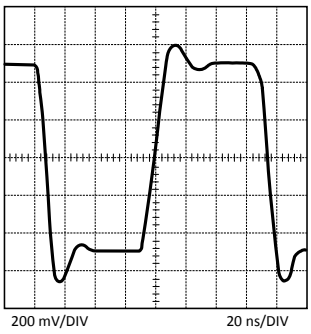

Figure 58. Converter Step Response ($1V_{PP}$, 20 ns/DIV)

10 Power Supply Recommendations

The LMH664x device family can operate off a single supply or with dual supplies. The input CM capability of the parts (CMVR) extends all the way down to the V- rail to simplify single supply applications. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

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11 Layout

11.1 Layout Guidelines

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15, "Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers", SNOA367, for more information). Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Table 1. Printed Circuit Board Layout And Component Values

DEVICE	PACKAGE	EVALUATION BOARD PN
LMH6642MF	5-Pin SOT-23	LMH730216
LMH6642MA	8-Pin SOIC	LMH730227
LMH6643MA	8-Pin SOIC	LMH730036
LMH6643MM	8-Pin VSSOP	LMH730123
LMH6644MA	14-Pin SOIC	LMH730231
LMH6644MT	14-Pin TSSOP	LMH730131

Another important parameter in working with high speed/high performance amplifiers, is the component values selection. Choosing external resistors that are large in value will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction to a large extent. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation.

11.2 Layout Example

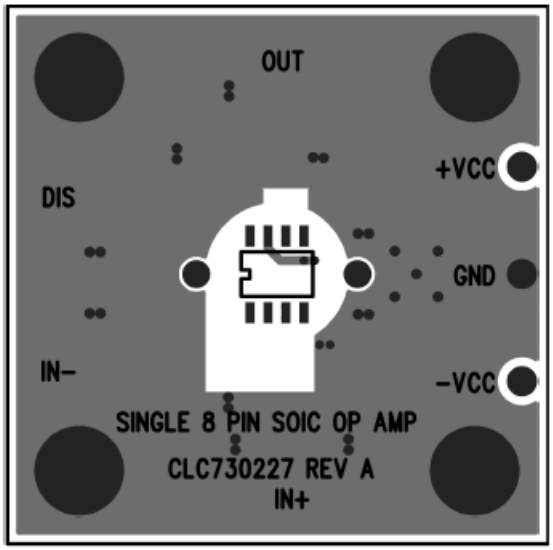

Figure 59. LMH6642/LMH6643/LMH6644 Layer 1

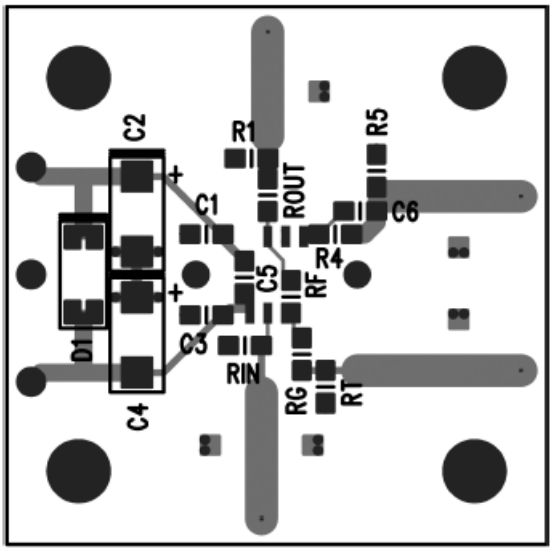

Figure 60. LMH6642/LMH6643/LMH6644 Layer 2

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMH6642	Click here	Click here	Click here	Click here	Click here
LMH6643	Click here	Click here	Click here	Click here	Click here
LMH6644	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6642MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 42MA
LMH6642MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 42MA
LMH6642MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 42MA
LMH6642MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 42MA
LMH6642MF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	A64A
LMH6642MF/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A64A
LMH6642MFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	A64A
LMH6642MFX/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A64A
LMH6643MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 43MA
LMH6643MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 43MA
LMH6643MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 43MA
LMH6643MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 43MA
LMH6643MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A65A
LMH6643MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A65A
LMH6643MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A65A
LMH6643MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A65A
LMH6644MA/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH6644MA
LMH6644MA/NOPB.A	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH6644MA
LMH6644MAX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH6644MA
LMH6644MAX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH6644MA
LMH6644MT/NOPB	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LMH66 44MT
LMH6644MT/NOPB.A	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMH66 44MT

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6644MTX/NOPB	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LMH66 44MT
LMH6644MTX/NOPB.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMH66 44MT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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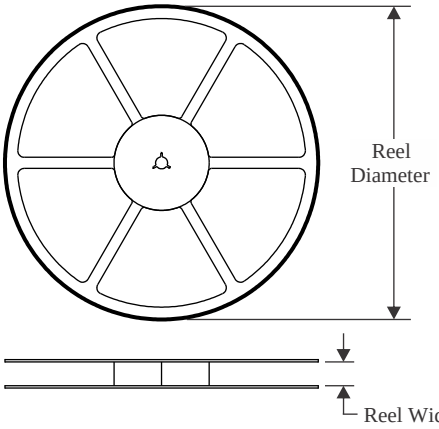
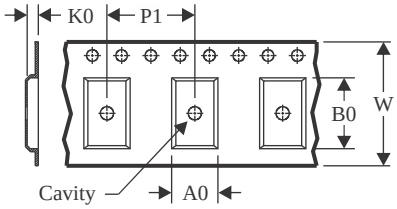
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

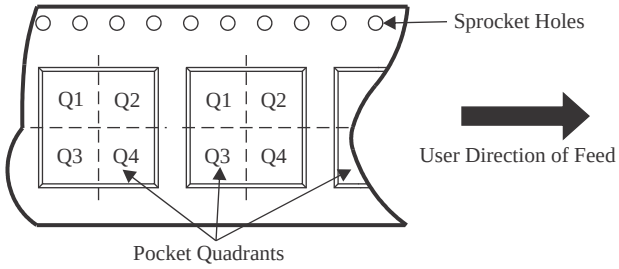


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

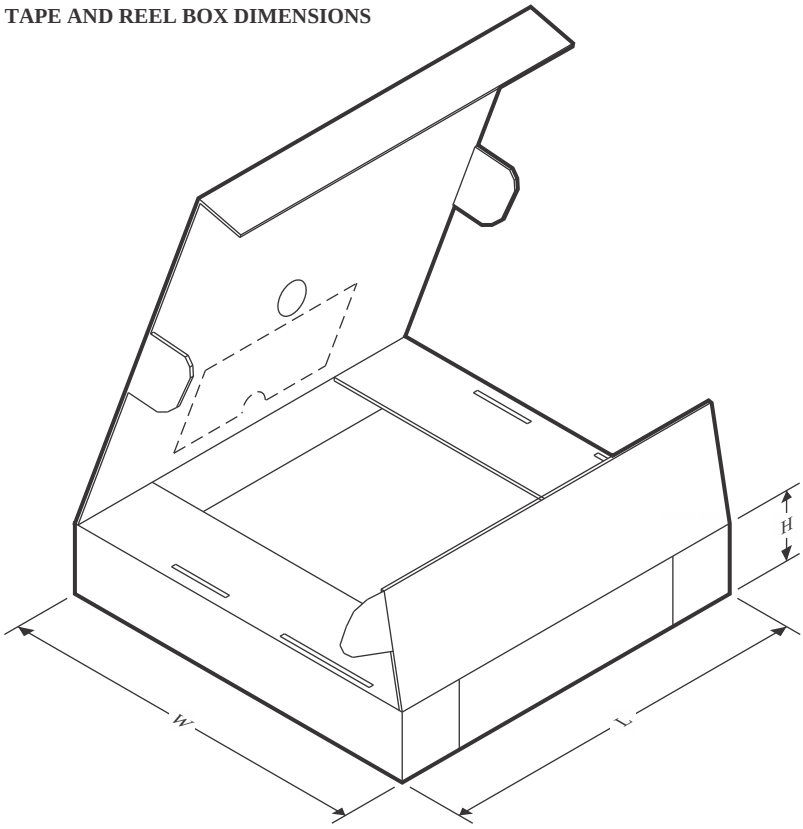
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6642MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6642MF/NOPB	SOT-23	DBV	5	1000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6642MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6642MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6642MFX/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6643MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6643MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6643MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6644MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMH6644MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMH6644MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

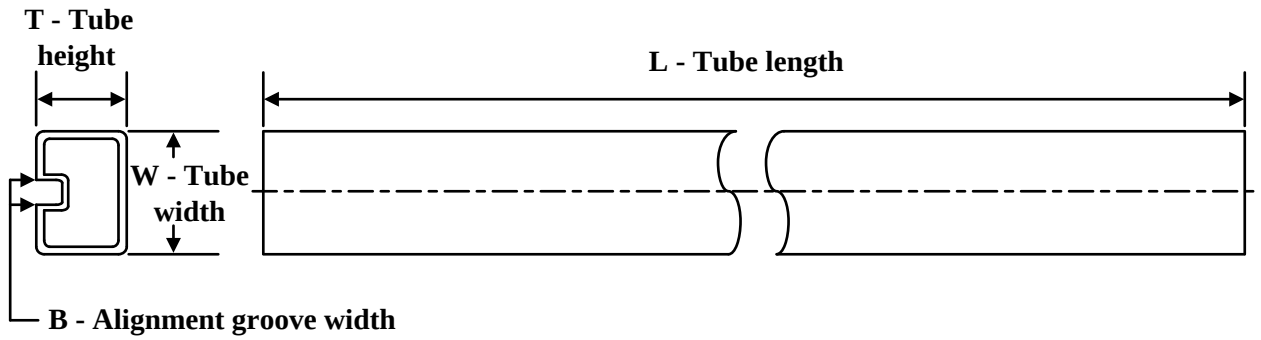
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6642MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6642MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6642MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMH6642MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMH6642MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6643MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6643MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMH6643MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMH6644MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMH6644MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMH6644MTX/NOPB	TSSOP	PW	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

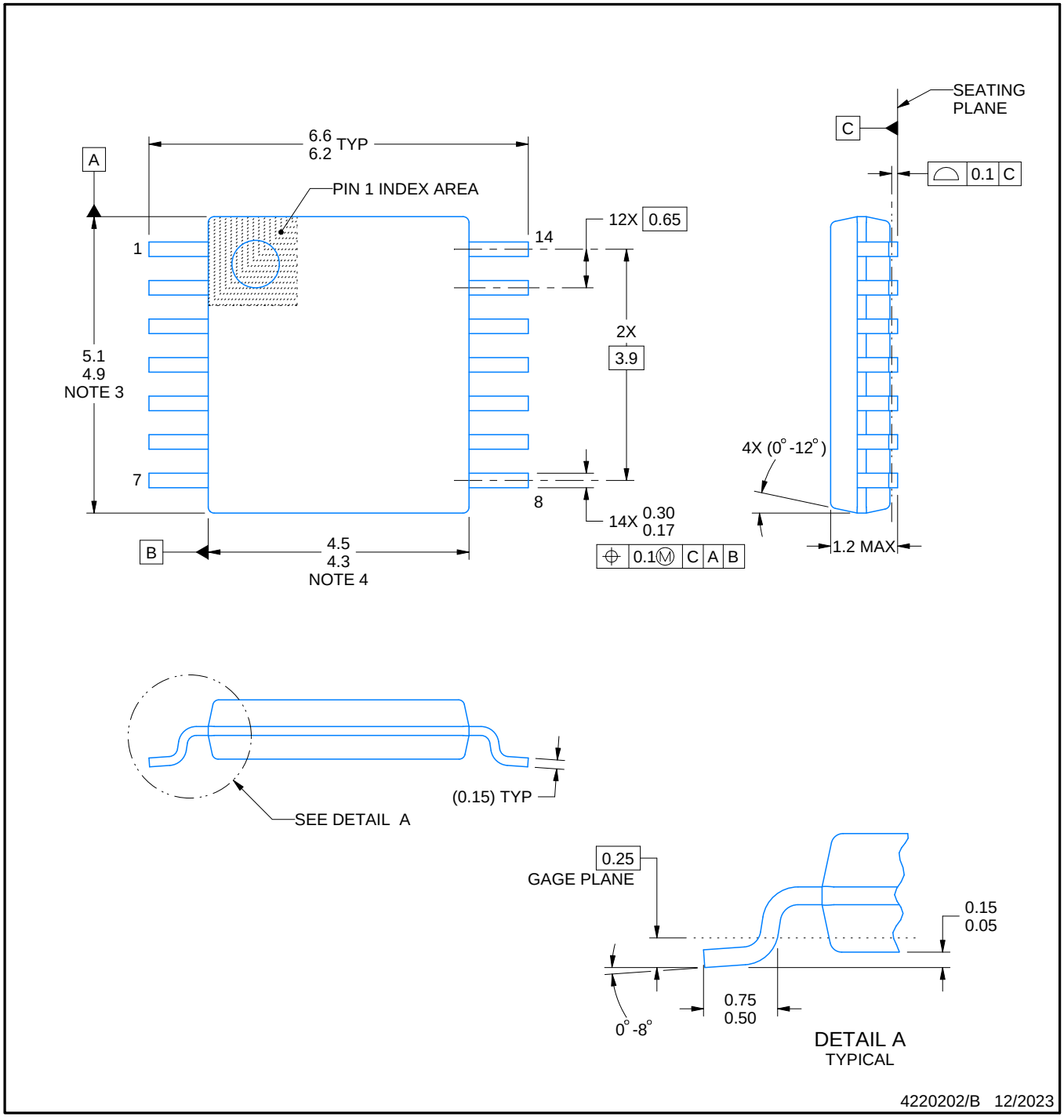
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6642MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6642MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMH6643MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6643MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMH6644MA/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMH6644MA/NOPB.A	D	SOIC	14	55	495	8	4064	3.05
LMH6644MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LMH6644MT/NOPB	PW	TSSOP	14	94	530	10.2	3600	3.5
LMH6644MT/NOPB.A	PW	TSSOP	14	94	530	10.2	3600	3.5
LMH6644MT/NOPB.A	PW	TSSOP	14	94	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0014A

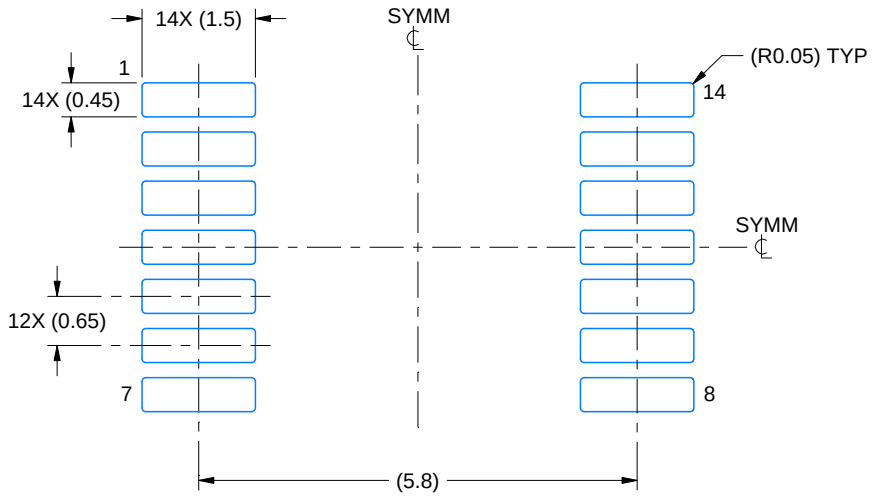
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

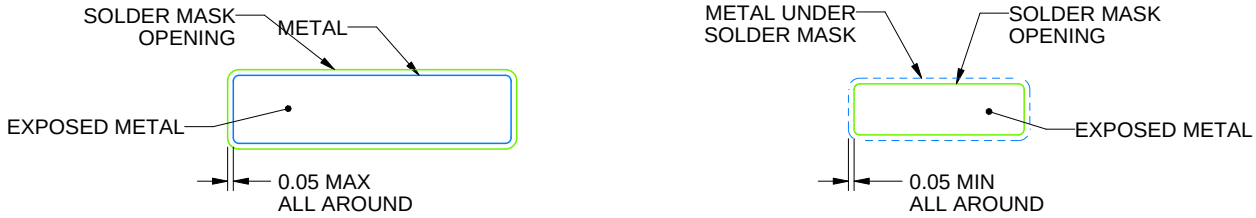


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

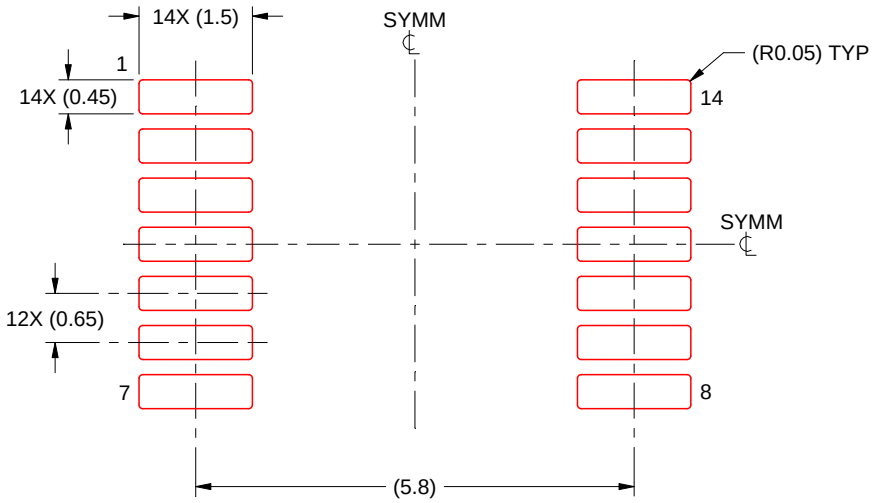


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

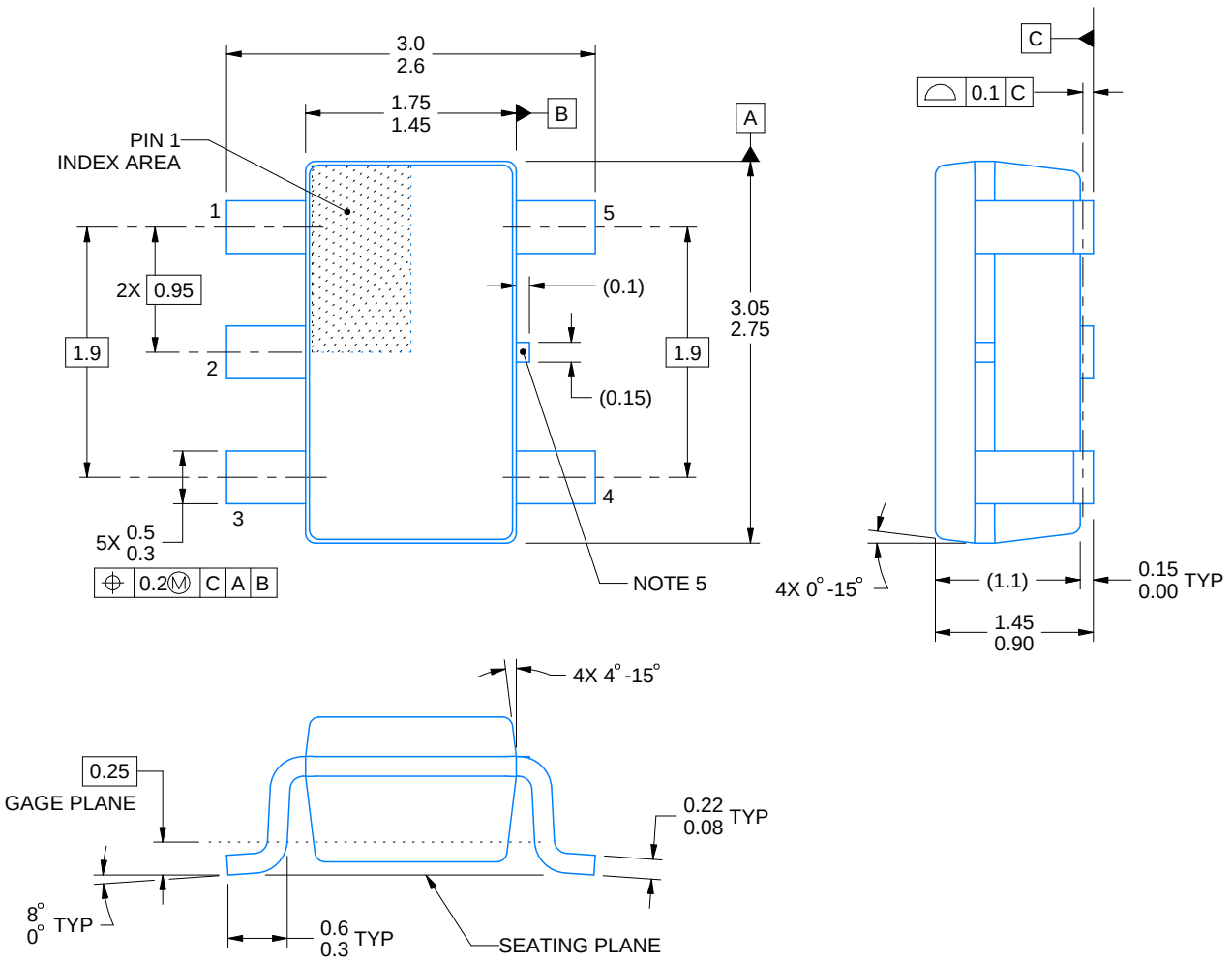
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

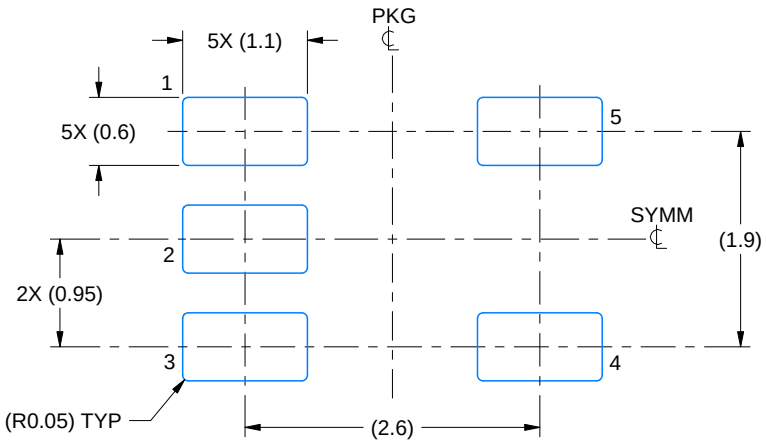
SMALL OUTLINE TRANSISTOR



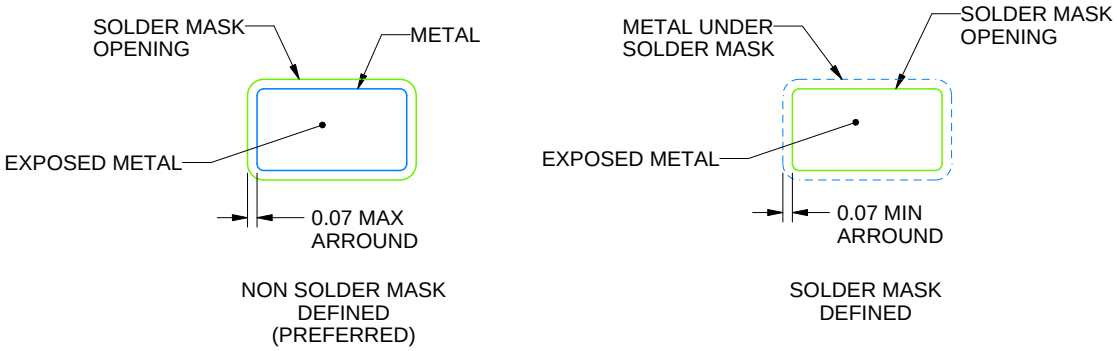
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

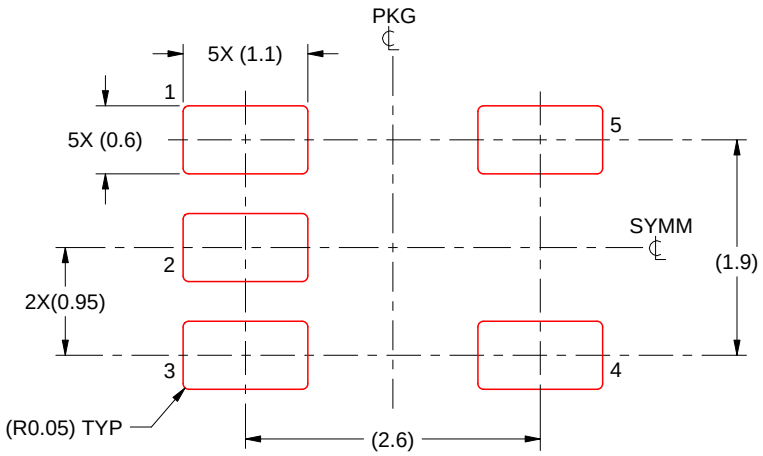


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

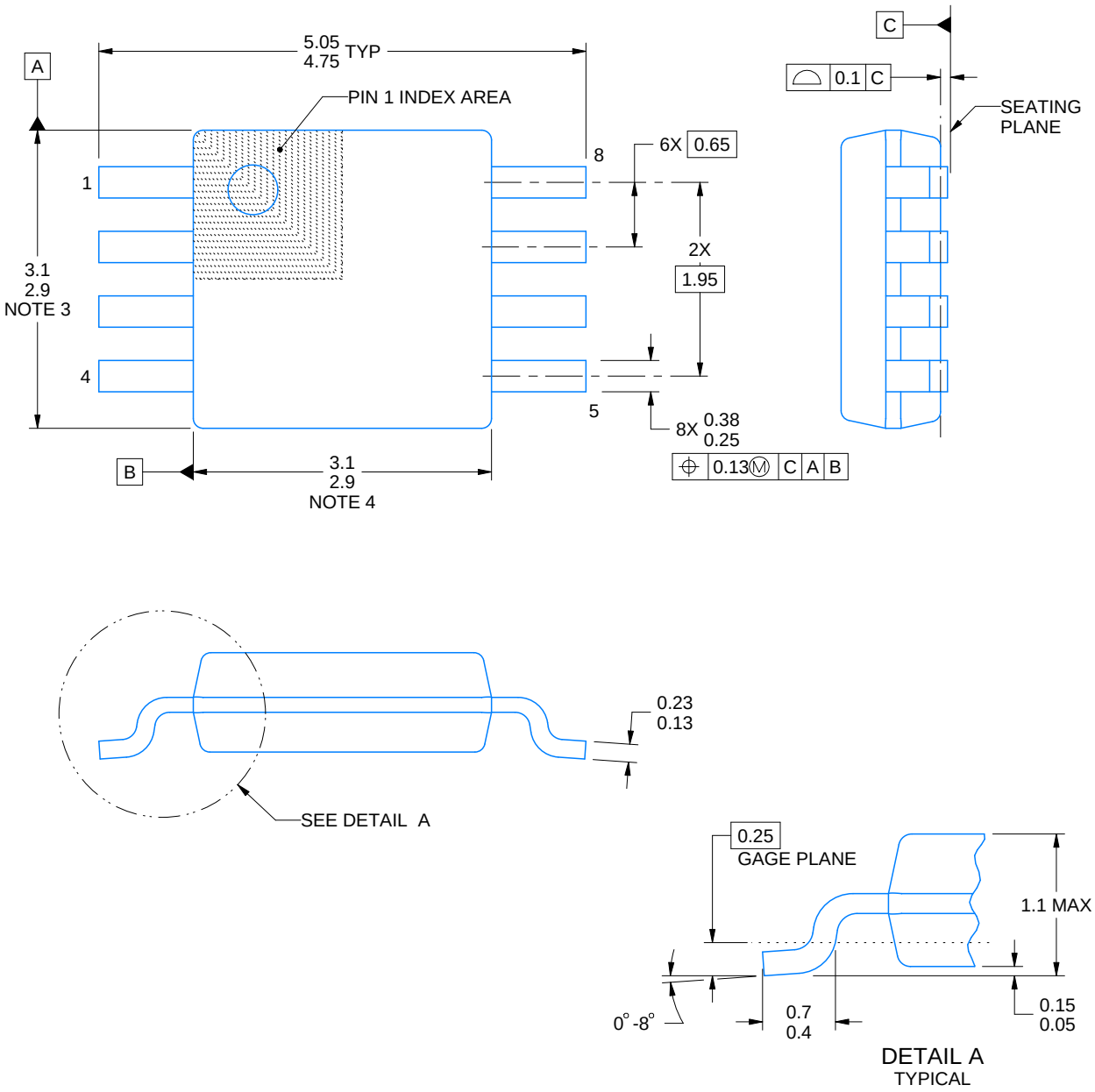
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

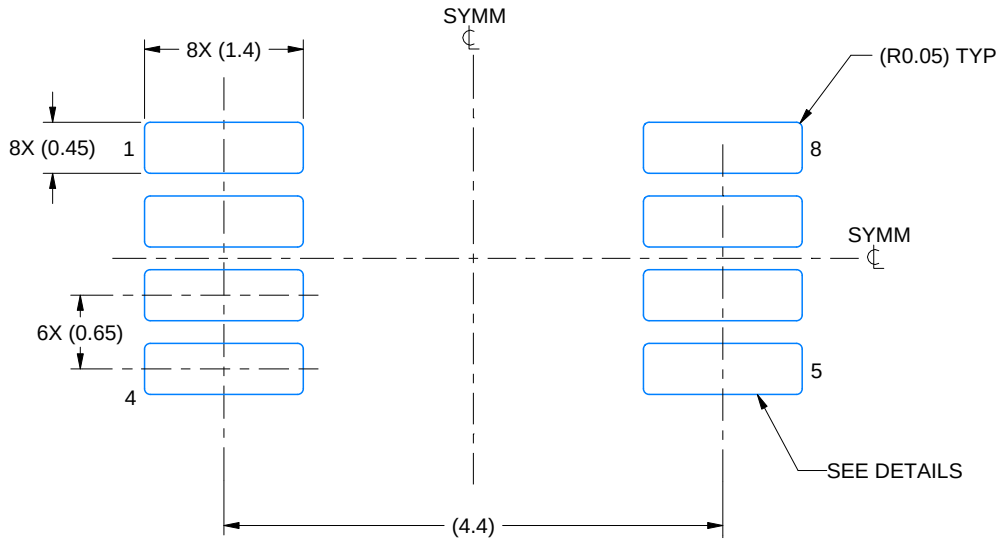
SMALL OUTLINE PACKAGE



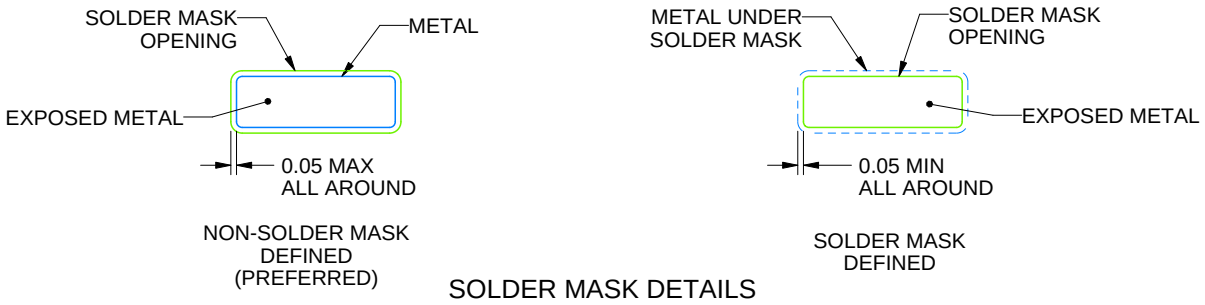
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

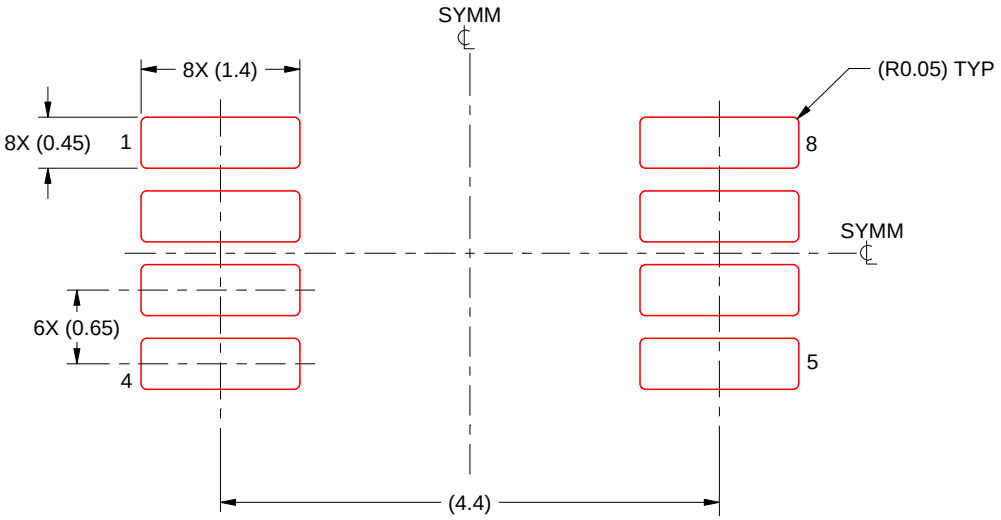


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

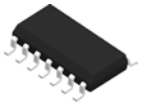


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

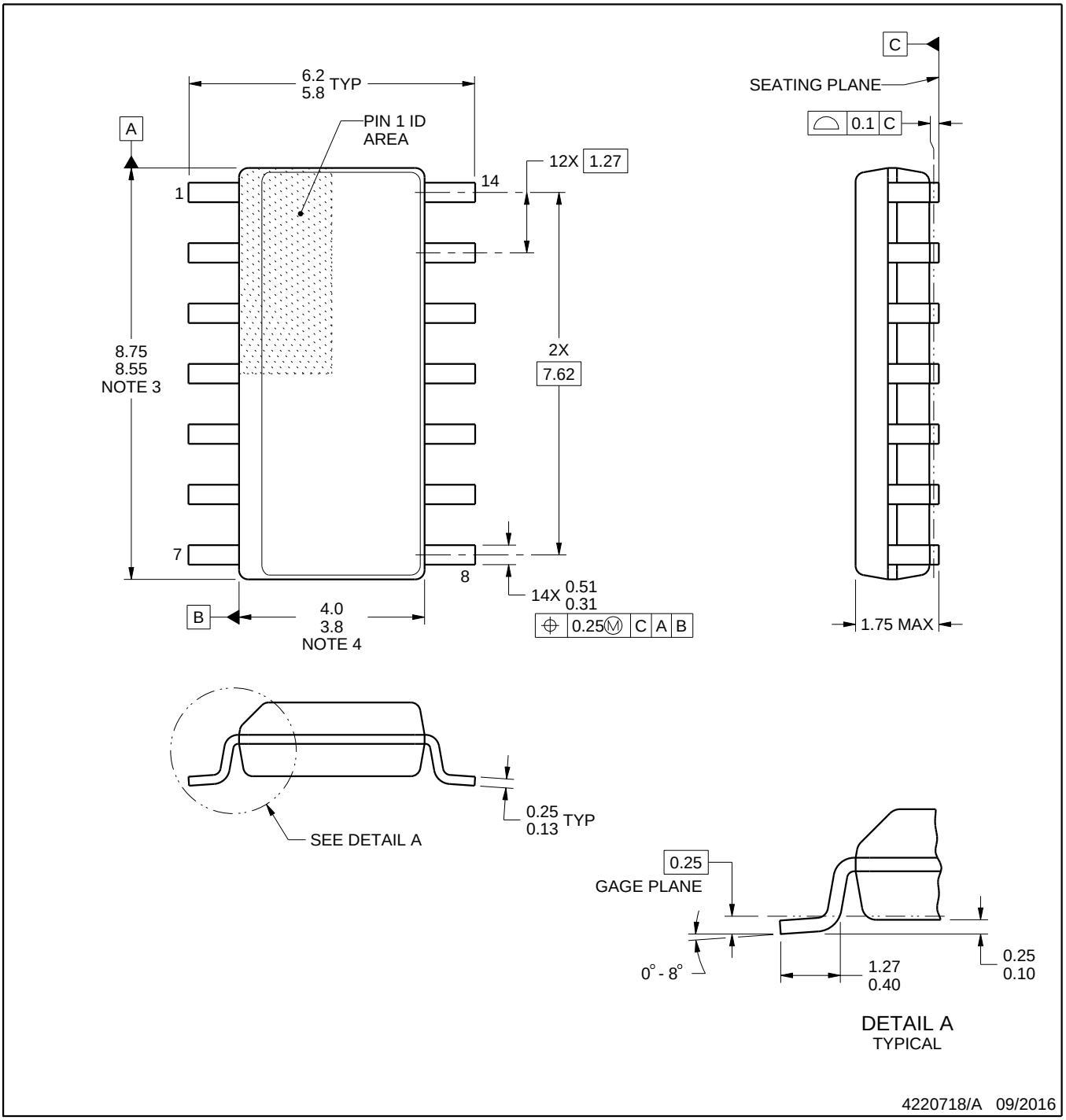


PACKAGE OUTLINE

D0014A

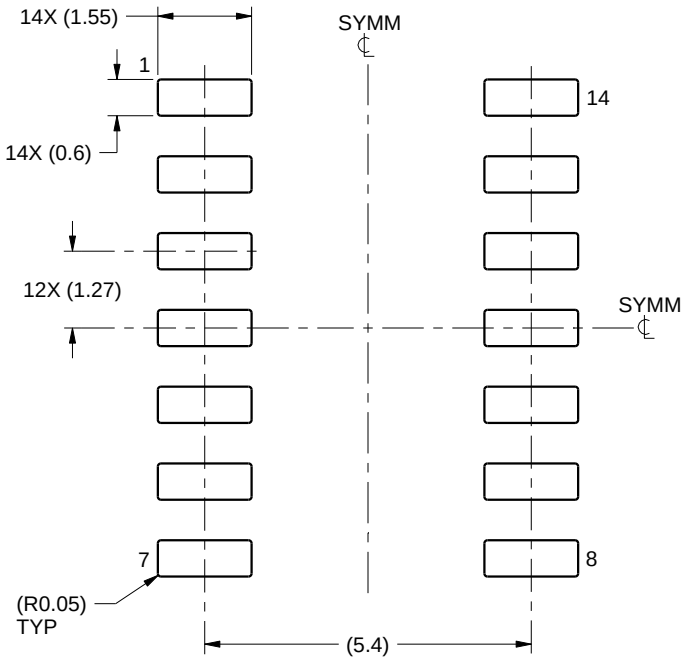
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

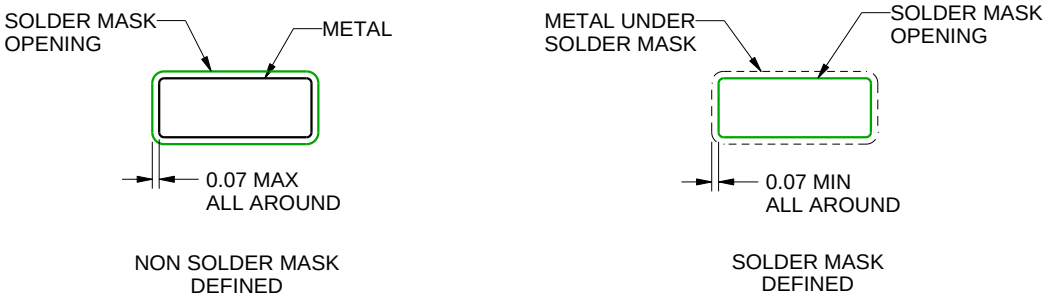


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

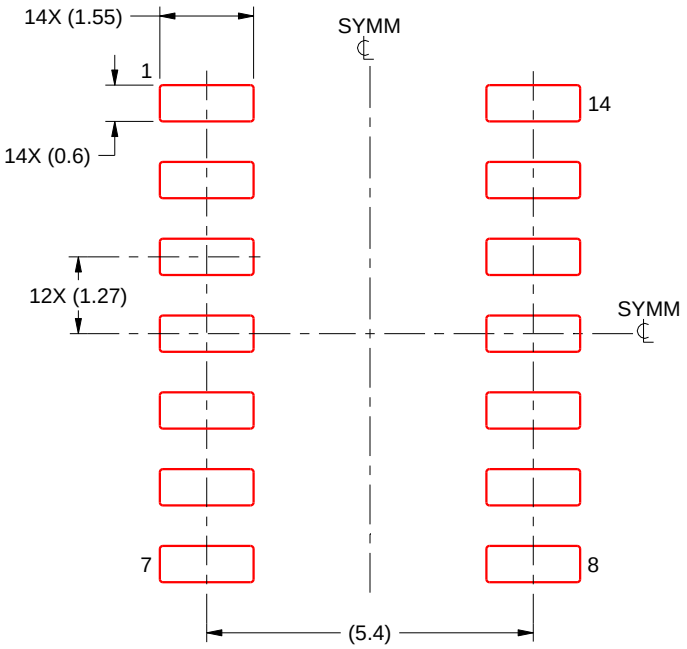
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

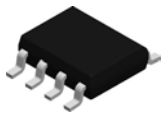


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

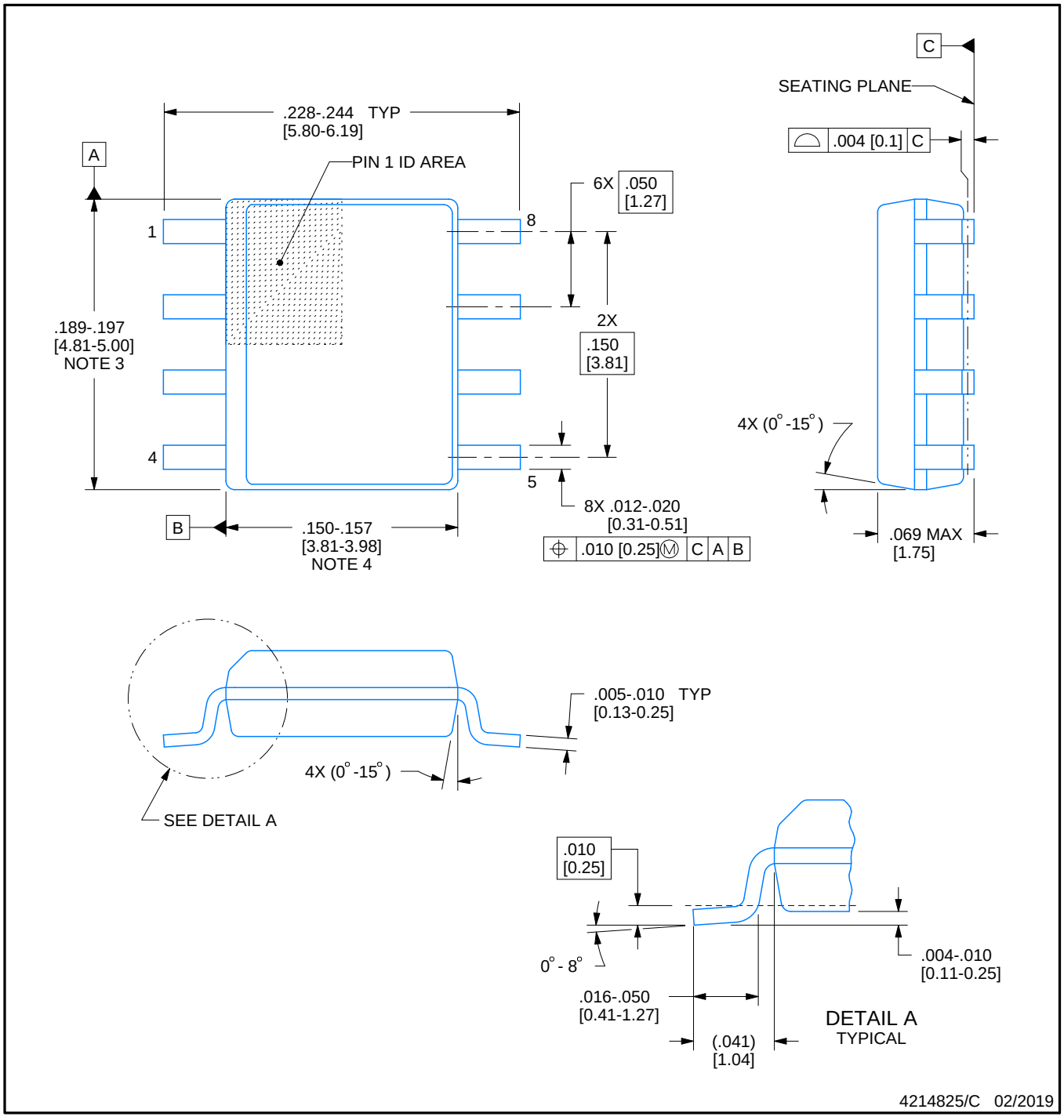


PACKAGE OUTLINE

D0008A

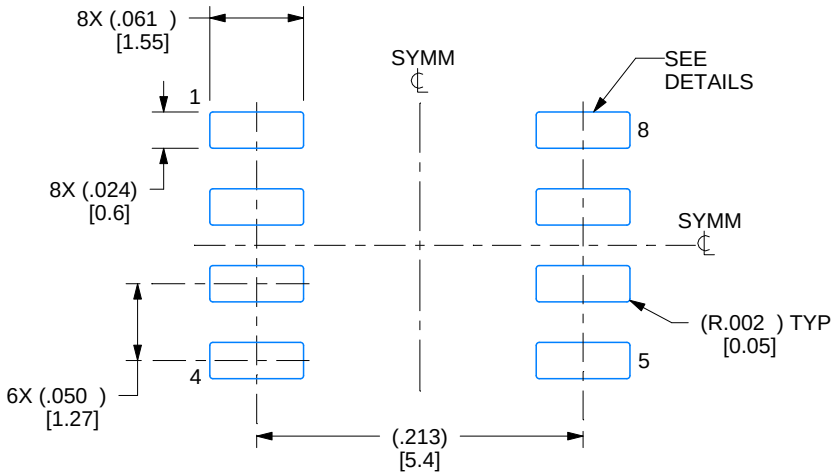
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

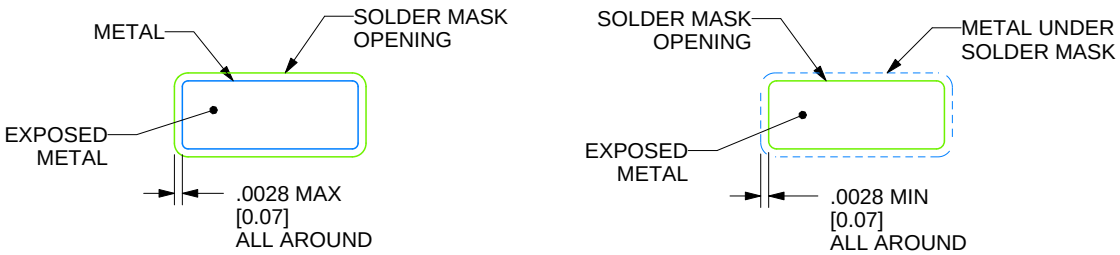


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

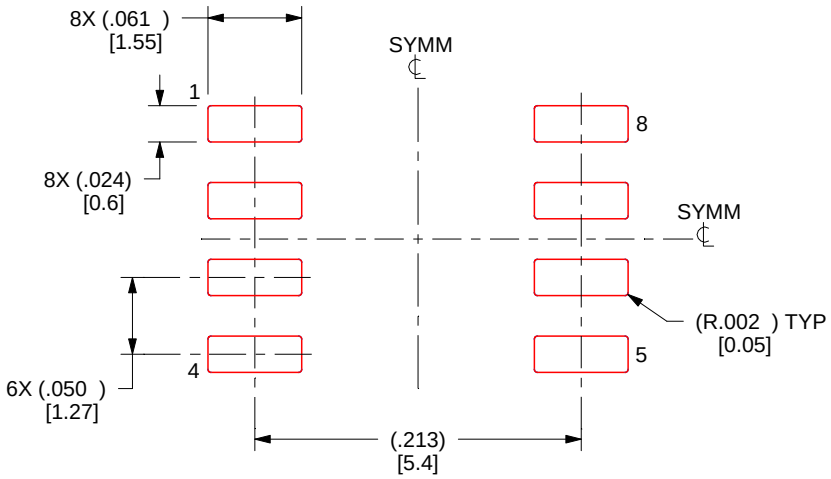
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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