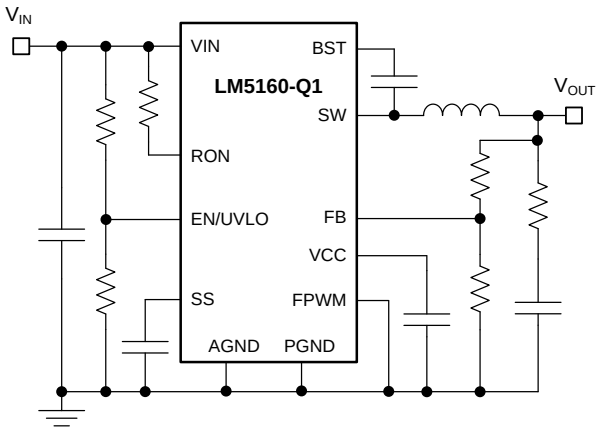
LM5160-Q1 宽输入 65V、2A 同步降压/Fly-Buck™ 直流/直流转换器

1 特性

- 符合适用于汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C ≤ T_A ≤ 125°C
  - HBM ESD 分类等级 2
  - CDM ESD 分类等级 C5
- 4.5V 至 65V 宽输入电压范围
- 集成高侧和低侧开关
  - 无需外部肖特基二极管
- 2A 最大负载电流
- 符合 CISPR 25 EMI 标准
- 自适应恒定导通时间控制
  - 无外部环路补偿
  - 快速瞬态响应
- 可选强制 PWM 或 DCM 运行
  - FPWM 支持多输出 Fly-Buck™
- 近似恒定的开关频率
  - 可通过电阻器调节至最高 1MHz
- 可编程软启动时间
- 预偏置启动
- ±1% 反馈电压基准
- 固有保护 特性 可实现稳健设计
  - 峰值电流限制保护
  - 可调输入欠压闭锁 (UVLO) 和滞后
  - VCC 和栅极驱动 UVLO 保护
  - 具有迟滞的热关断保护
- 14 引脚 HTSSOP 封装，0.65mm 间距
- 使用 LM5160-Q1 及其 WEBENCH® 电源设计器创建定制设计

典型同步降压应用电路



2 应用

- 汽车直流/直流转换器
- IGBT 栅极驱动偏置电源
- 低功耗隔离式直流/直流 (Fly-Buck)

3 说明

LM5160-Q1 是一款具有集成式高侧和低侧 MOSFET 的 65V 2A 同步降压转换器。自适应恒定导通时间控制方案无需环路补偿，可在快速瞬态响应下支持高降压比。内部反馈放大器保持着整体工作温度范围 ±1% 的输出电压调节度。导通时间与输入时间成反比，其结果是切换频率接近恒定。

峰谷电流限制电路可防御过载情况。欠压锁定 (EN/UVLO) 电路提供可独立调节的输入欠压阈值和迟滞。LM5160-Q1 通过 FPWM 引脚进行编程，以在从空载到满载过程中采用连续传导模式 (CCM) 或在轻负载时自动切换至断续传导模式 (DCM)，从而实现更高的效率。强制 CCM 运行支持使用耦合电感器的多输出隔离式 Fly-Buck 应用 。

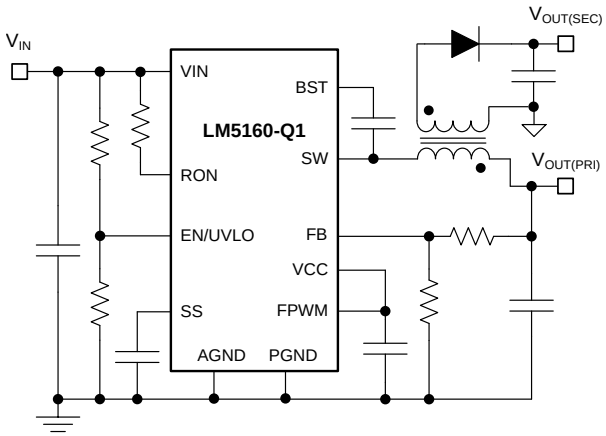
LM5160-Q1 符合汽车 AEC-Q100 1 级标准，并且可采用引脚间距为 0.65mm 的 14 引脚 HTSSOP 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM5160-Q1	HTSSOP (14)	4.40mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型 Fly-Buck 应用电路



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (November 2017) to Revision C — **Page**

- 已更改 *特性* ... 1
- 已更改 首页原理图 ... 1
- Changed *Pinout Drawing* ... 3
- Changed *ESD Ratings* ... 4
- Changed *Function Block Diagram* ... 10
- Changed *Power Supply Recommendations* ... 25
- 已更改 *相关文档* ... 27

Changes from Revision A (November 2015) to Revision B — **Page**

- 更新了与符合 AEC-Q100 标准相关的要点 ... 1
- Deleted the lead temperature from the *Absolute Maximum Ratings* table ... 4
- Moved the *Ripple Configuration* section to the *Application Information* section ... 15
- Changed the *Application Performance Plots* title to *Application Curves* in both typical application sections ... 20
- Added layout details with LM5160-Q1 HTSSOP-14 package ... 26
- 已更改 *静电放电注意事项*声明 ... 28

Changes from Original (July 2015) to Revision A — **Page**

- Changed current limit off-timer in the Electrical Characteristics to 16 ... 5

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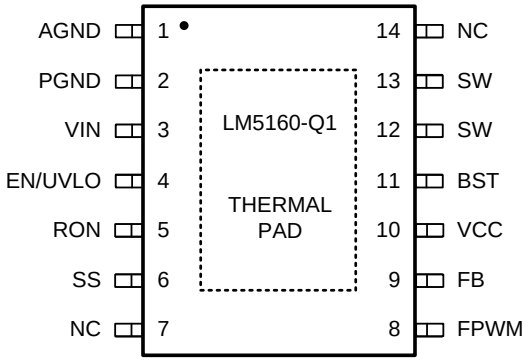
5 Pin Configuration and Functions

PWP PowerPAD™ Package
14-Pin HTSSOP
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	AGND	—	Analog Ground. Ground connection of internal control circuits.
2	PGND	P	Power Ground. Ground connection of the internal synchronous rectifier FET.
3	VIN	P	Input supply connection. Operating input range is 4.5 V to 65 V.
4	EN/UVLO	I	Precision enable. Input pin of undervoltage lockout (UVLO) comparator.
5	RON	I	On-time programming pin. A resistor between this pin and VIN sets the switch on-time as a function of input voltage.
6	SS	I	Soft-start. Connect a capacitor from SS to AGND to control output rise time and limit overshoot.
8	FPWM	I	Forced PWM logic input pin. Connect to AGND for discontinuous conduction mode (DCM) with light loads. Connect to VCC for continuous conduction mode (CCM) at all loads and Fly-Buck configuration.
9	FB	I	Feedback input of voltage regulation comparator.
10	VCC	O	Internal high voltage start-up regulator bypass capacitor pin.
11	BST	P	Bootstrap capacitor pin. Connect a capacitor between BST and SW to bias gate driver of high-side buck FET.
12,13	SW	P	Switch node. Source connection of high-side buck FET and drain connection of low-side synchronous rectifier FET.
7,14	NC	—	No Connection.
—	EP	—	Exposed Pad. Connect to AGND and printed-circuit board ground plane to improve power dissipation.

(1) P = Power, G = Ground, I = Input, O = Output.

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6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature of –40°C to 150°C (unless otherwise noted).(1)(2)

		MIN	MAX	UNIT
Input voltages	VIN to AGND	–0.3	70	V
	EN/UVLO to AGND	–0.3	70	
	RON to AGND	–0.3	70	
	BST to AGND	–0.3	84	
	VCC to AGND	–0.3	14	
	FPWM to AGND	–0.3	14	
	SS to AGND	–0.3	7	
	FB to AGND	–0.3	7	
Output voltages	BST to SW	–0.3	14	V
	BST to VCC		70	
	SW to AGND	–1.5	70	
	SW to AGND (20-ns transient)	–3		
Operating junction temperature, T_J(3)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature of –40°C to 150°C (unless otherwise noted).(1)

	MIN	MAX	UNIT
V_{IN} input voltage	4.5	65	V
I_{OUT} output current		2	A
Operating junction temperature	-40	150	°C

(1) *Recommended Operating Ratings* are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.

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6.4 Thermal Information

THERMAL METRIC[1]		LM5160-Q1 PWP (HTSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.3	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W
ψ_{JB}	Junction-to-board thermal characteristic parameter	19.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.6	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	22.8	°C/W
ψ_{JT}	Junction-to-top thermal characteristic parameter	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* report.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{IN} = 24 V.[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{SD}	Input shutdown current	V_{IN} = 24 V, $V_{EN/UVLO}$ = 0 V		50	90.7	µA
I_{OP}	Input operating current	V_{IN} = 24 V, V_{FB} = 3 V, non-switching		2.3	2.84	mA
VCC SUPPLY						
V_{CC}	Bias regulator output	V_{IN} = 24 V, I_{CC} = 20 mA	6.47	7.5	8.52	V
V_{CC}	Bias regulator current limit	V_{IN} = 24 V	30			mA
$V_{CC(UV)}$	VCC undervoltage threshold	V_{VCC} rising		3.98	4.1	V
$V_{CC(HYS)}$	VCC undervoltage hysteresis	V_{VCC} falling		185		mV
$V_{CC(LDO)}$	VIN – VCC dropout voltage	V_{IN} = 4.5 V, I_{VCC} = 20 mA		165	260	mV
HIGH-SIDE FET						
$R_{DS(ON)}$	High-side on-state resistance	$V_{BST} – V_{SW}$ = 7 V, I_{SW} = 1 A		0.29		Ω
$BST_{(UV)}$	Bootstrap gate drive UV	$V_{BST} – V_{SW}$ rising		2.93	3.6	V
$BST_{(HYS)}$	Gate drive UV hysteresis	$V_{BST} – V_{SW}$ falling		200		mV
LOW-SIDE FET						
$R_{DS(ON)}$	Low-side on-state resistance	I_{SW} = 1 A		0.13		Ω
HIGH-SIDE CURRENT LIMIT						
$I_{LIM\ (HS)}$	High-side current limit threshold		2.125	2.5	2.875	A
T_{RES}	Current limit response time	$I_{LIM\ (HS)}$ threshold detect to FET turnoff		100		ns
T_{OFF1}	Current limit forced off-time	V_{FB} = 0 V, V_{IN} = 65 V	16	29	39.8	µs
T_{OFF2}	Current limit forced off-time	V_{FB} = 1 V, V_{IN} = 24 V	2.18	3.5	5.12	µs
LOW-SIDE CURRENT LIMIT						
$I_{SOURCE(LS)}$	Sourcing current limit		1.9	2.5	3	A
$I_{SINK(LS)}$	Sinking current limit			5.4		A
DIODE EMULATION						
$V_{FPWM(LOW)}$	FPWM input logic low	V_{IN} = 24 V			1	V
$V_{FPWM(HIGH)}$	FPWM input logic high	V_{IN} = 24 V	3			V
I_{ZX}	Zero cross detect current	FPWM = AGND (diode emulation)		0		mA
REGULATION COMPARATOR						
V_{REF}	FB regulation level	V_{IN} = 24 V	1.975	1.995	2.015	V
$I_{(Bias)}$	FB input bias current	V_{IN} = 24 V			100	nA

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \bullet R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in Thermal Information.

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Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{IN} = 24 V.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR CORRECTION AMPLIFIER and SOFT START						
G_M	Error amp transconductance	$V_{FB} = V_{REF} \pm 10$ mV		105		µA/V
$I_{EA(Source)}$	Error amp source current	V_{FB} = 1 V, V_{SS} = 1 V	7.62	10.2	12.51	µA
$I_{EA(Sink)}$	Error amp sink current	V_{FB} = 5 V, V_{SS} = 2.25 V	7.46	10	12.2	µA
$V_{(SS-FB)}$	$V_{SS} – V_{FB}$ clamp voltage	V_{FB} = 1.75 V, C_{SS}= 1 nF		135		mV
I_{SS}	Soft-start charging current	V_{SS} = 0.5 V	7.63	10.2	12.5	µA
ENABLE/UVLO						
$V_{UVLO\ (TH)}$	UVLO threshold	$V_{EN/UVLO}$ rising	1.213	1.24	1.277	V
$I_{UVLO(HYS)}$	UVLO hysteresis current	$V_{EN/UVLO}$ = 1.4 V	15	20	25	µA
$V_{SD(TH)}$	Shutdown mode threshold	$V_{EN/UVLO}$ falling	0.28	0.35		V
$V_{SD(HYS)}$	Shutdown threshold hysteresis	$V_{EN/UVLO}$ rising		47		mV
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			175		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			20		°C

6.6 Switching Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{IN} = 24 V.(1)

		MIN	TYP	MAX	UNIT
MINIMUM OFF-TIME					
$T_{OFF-MIN}$	Minimum off-time, V_{FB} = 0 V		170		ns
ON-TIME GENERATOR					
T_{ON1}	V_{IN} = 24 V, R_{ON} = 100 kΩ	312	428	520	ns
T_{ON2}	V_{IN} = 24 V, R_{ON} = 200 kΩ	625	818	1040	ns
T_{ON3}	V_{IN} = 8 V, R_{ON} = 100 kΩ	937	1247	1563	ns
T_{ON4}	V_{IN} = 65 V, R_{ON} = 100 kΩ	132	176	220	ns

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

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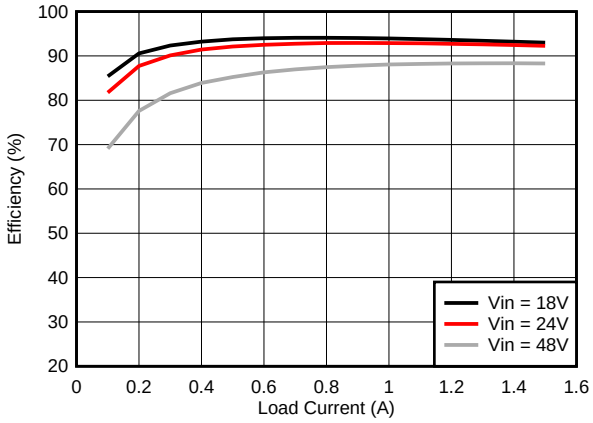
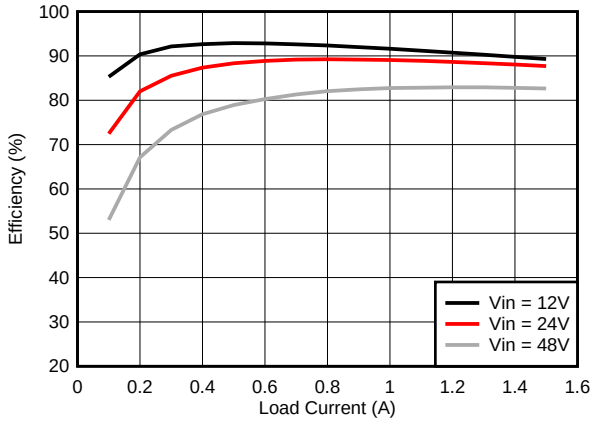
6.7 Typical Characteristics

T_A = 25°C, unless otherwise noted. Please refer to Typical Applications for circuit designs.



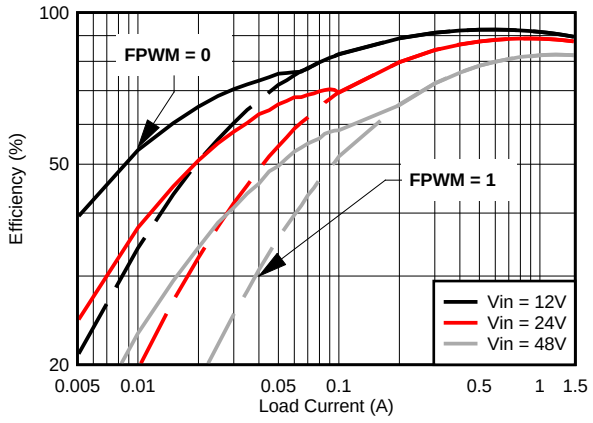
V_{OUT} = 10 V R_{ON} = 200 kΩ
L = 47 µH

Figure 1. Efficiency at 500 kHz



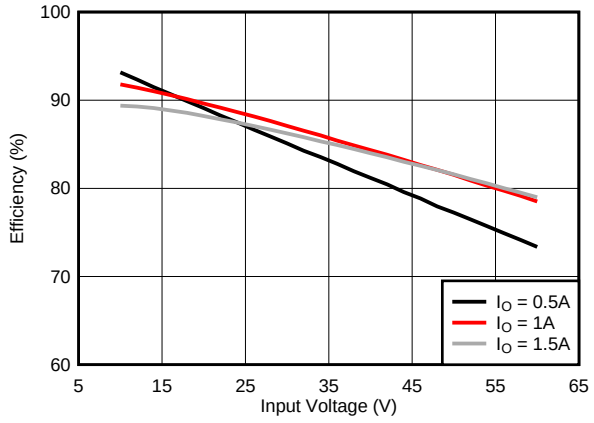
V_{OUT} = 5 V R_{ON} = 215 kΩ
L = 100 µH

Figure 2. Efficiency at 250 kHz



V_{OUT} = 5 V R_{ON} = 169 kΩ
L = 47 µH

Figure 3. Efficiency CCM vs DCM at 300 kHz



V_{OUT} = 5 V R_{ON} = 169 kΩ
L = 47 µH

Figure 4. Efficiency vs Input Voltage at 300 kHz

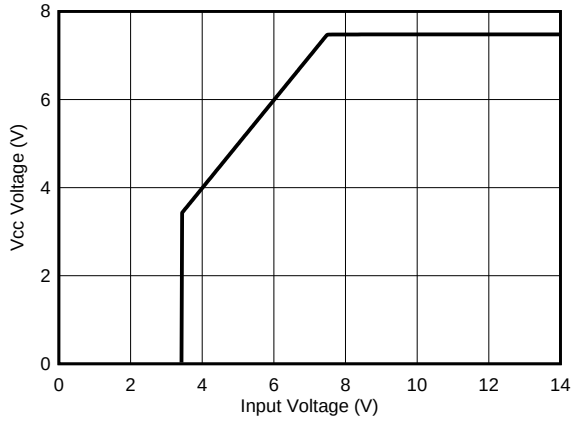
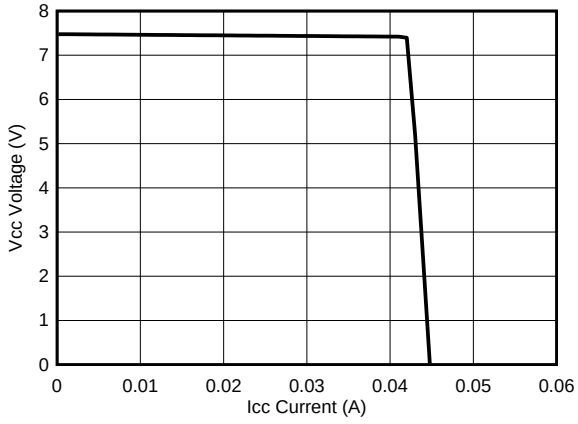


Figure 5. V_{CC} vs V_{IN}



V_{IN} = 24 V

Figure 6. V_{CC} vs I_{CC}

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Typical Characteristics (continued)

T_A = 25°C, unless otherwise noted. Please refer to Typical Applications for circuit designs.

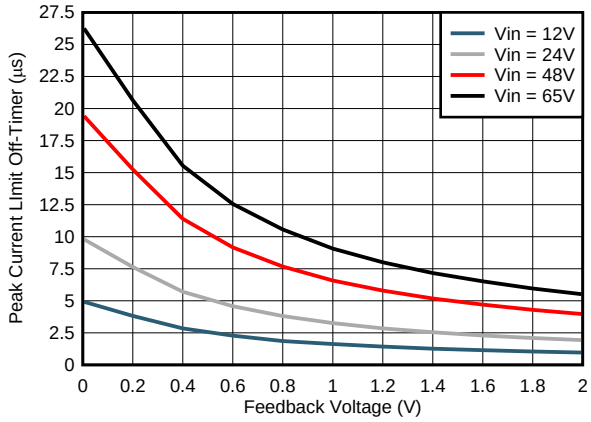

Figure 7. T_{OFF} (I_{LIM}) vs V_{FB}

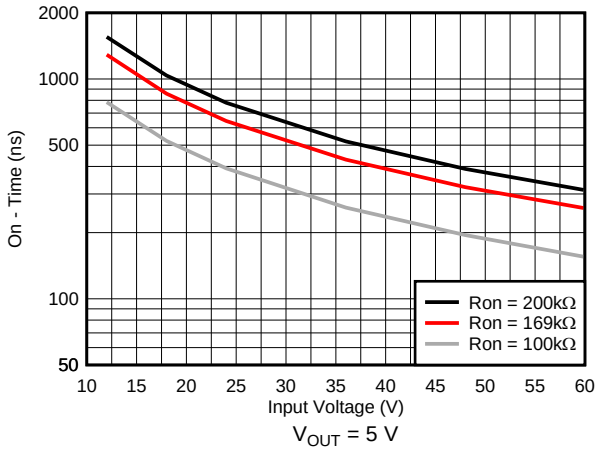

Figure 8. T_{ON} vs V_{IN}

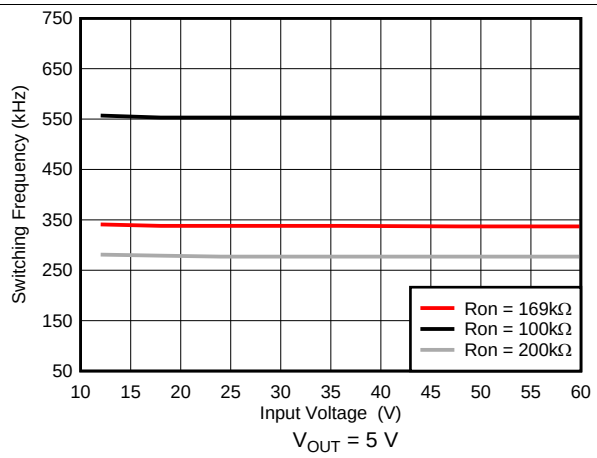

Figure 9. Switching Frequency vs V_{IN}

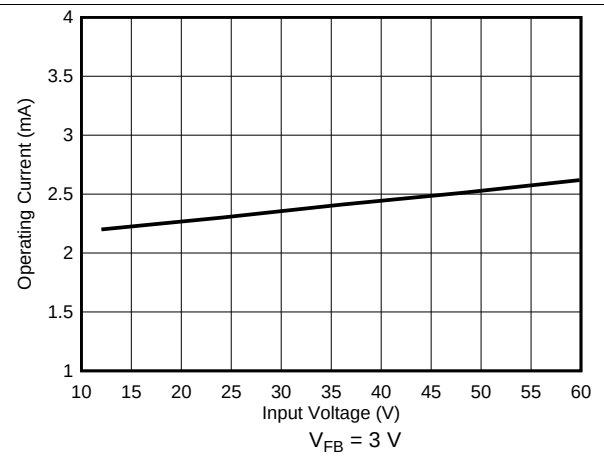

Figure 10. I_{IN} vs V_{IN} (Operating, Non-Switching)

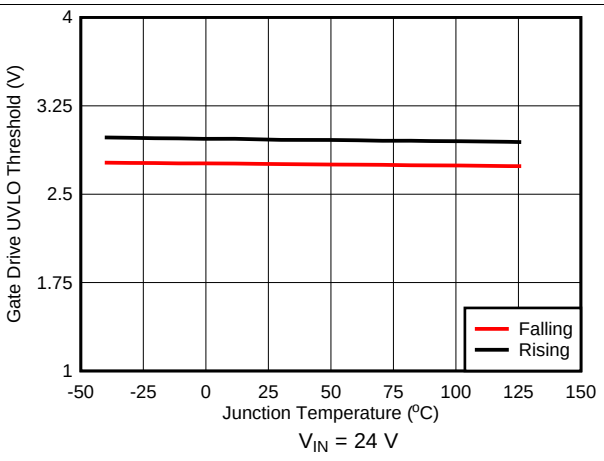

Figure 11. Gate Drive UVLO vs Temperature

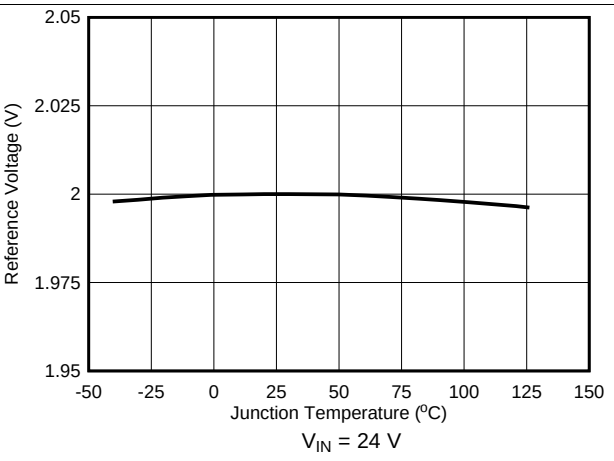

Figure 12. Reference Voltage vs Temperature

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Typical Characteristics (continued)

T_A = 25°C, unless otherwise noted. Please refer to Typical Applications for circuit designs.

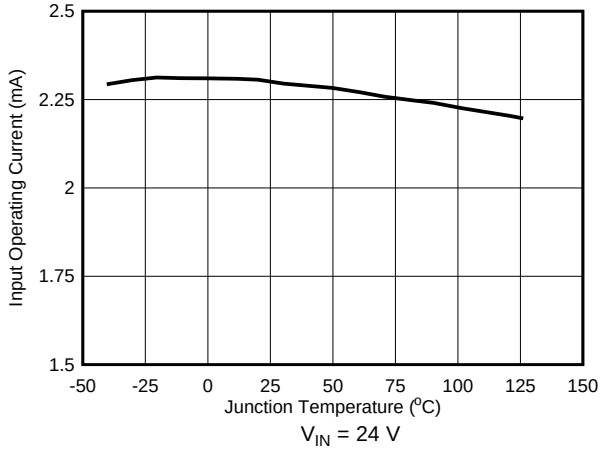

Figure 13. Input Operating Current vs Temperature

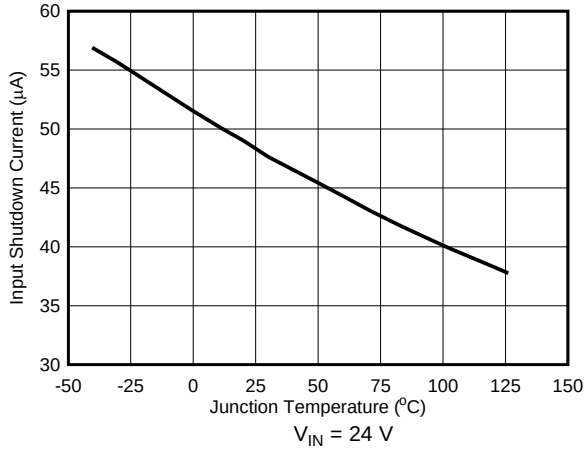

Figure 14. Input Shutdown Current vs Temperature

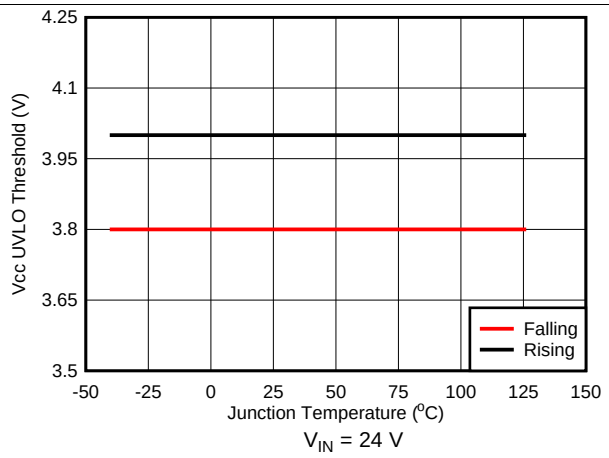

Figure 15. V_{CC} UVLO vs Temperature

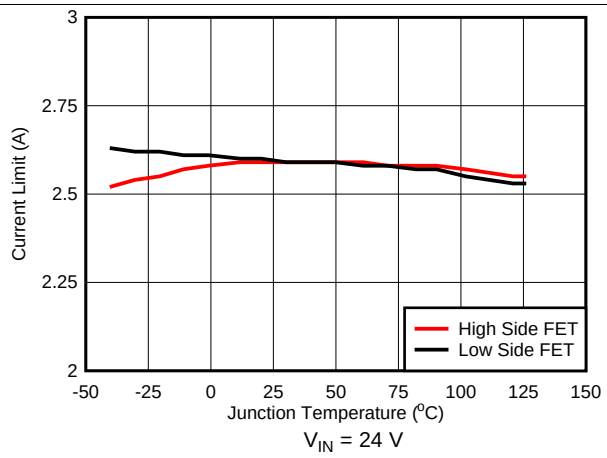

Figure 16. Current Limit vs Temperature

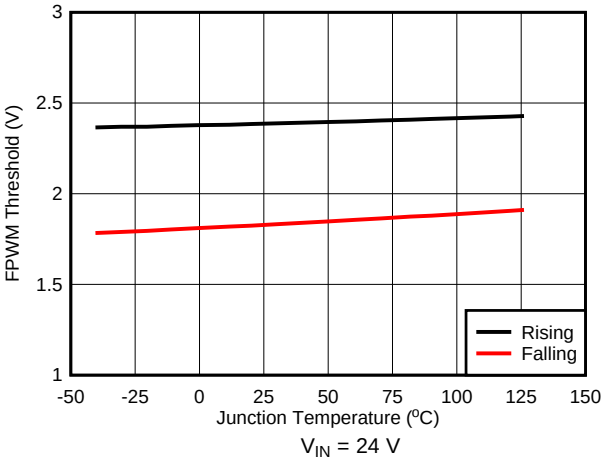

Figure 17. FPWM Threshold vs Temperature

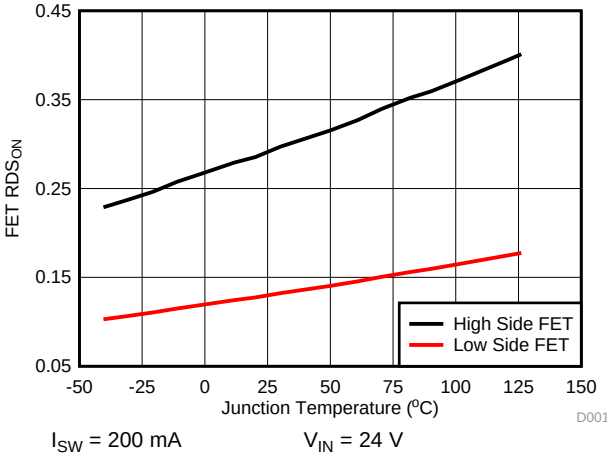

Figure 18. Switch Resistance vs Temperature

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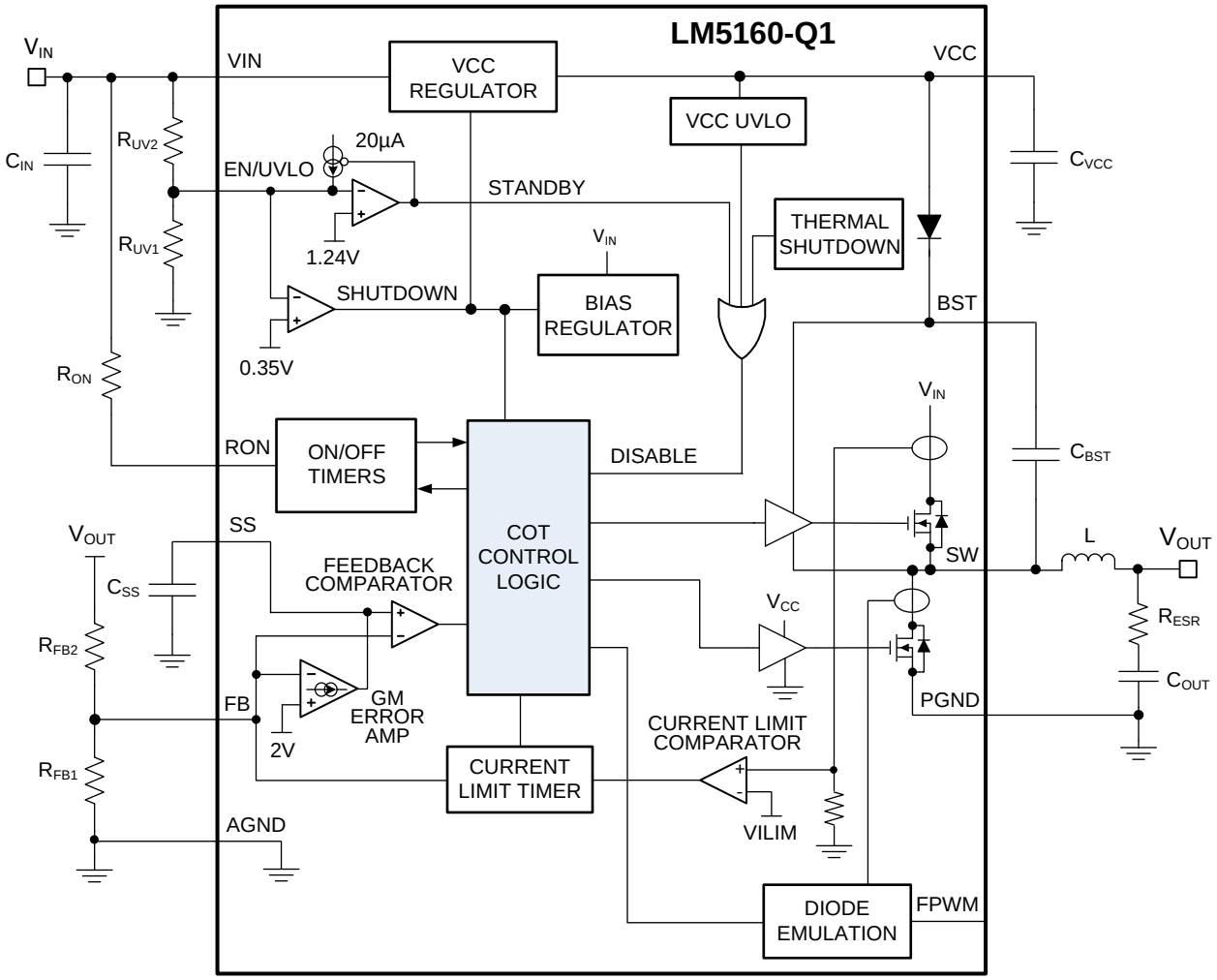
7 Detailed Description

7.1 Overview

The LM5160-Q1 step-down synchronous switching regulator features all the functions needed to implement a low-cost, efficient buck converter capable of supplying 2 A to the load. This high voltage regulator contains 65-V N-channel buck and synchronous rectifier switches and is available in a 14-pin HTSSOP package with 0.65-mm pin pitch. The regulator operation is based on an adaptive constant on-time control architecture where the on-time is inversely proportional to input voltage V_{IN}. This feature maintains a relatively constant operating frequency with load and input voltage variations. A constant on-time switching regulator requires no loop compensation resulting in fast load transient response. Peak current limit detection circuit is implemented with a forced off-time during current limiting which is inversely proportional to voltage at the feedback pin, V_{FB} and directly proportional to V_{IN}. Varying the current limit off-time with V_{FB} and V_{IN} ensures short-circuit protection with minimal current limit foldback. The LM5160-Q1 can be applied in numerous end equipment systems requiring efficient step-down regulation from higher input voltages. This regulator is well-suited for 24-V industrial systems as well as 48-V telecom and PoE voltage ranges. The LM5160-Q1 integrates an undervoltage lockout (EN/UVLO) circuit to prevent faulty operation of the device at low input voltages and features intelligent current limit and thermal shutdown to protect the device during overload or short circuit.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Control Circuit

The LM5160-Q1 step-down switching regulator employs a control principle based on a comparator and a one-shot timer, with the output voltage feedback (FB) compared to the voltage at the soft-start (SS) pin (V_{SS}). If the FB voltage is below V_{SS}, the internal buck switch is turned on for a conduction time determined by the input voltage and the one-shot programming resistor (R_{ON}). Following the on-time, the buck switch must stay off for the off-time forced by the minimum off-time one-shot. The buck switch remains off until the FB voltage falls below the SS voltage again, when it turns back on for another on-time interval.

During a rapid start-up or when the load current increases suddenly, the regulator operates with minimum off-time per cycle. When regulating the output in steady-state operation, the off-time automatically adjusts to produce the SW voltage duty cycle required for output voltage regulation.

When in regulation, the LM5160-Q1 operates in continuous conduction mode at heavy load currents. If FPWM is connected to ground or left floating, the regulator operates in discontinuous conduction mode at light load with the synchronous rectifier FET in diode emulation. With sufficient load, the LM5160-Q1 operates in continuous conduction mode with the inductor current never reaching zero during the off-time of the high-side FET. In this mode the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. The operating frequency is programmed by the resistor connected from VIN to RON and can be calculated from Equation 1 with R_{ON} expressed in Ohms.

$$F_{sw} = \frac{V_{OUT}}{R_{ON} \times 1 \times 10^{-10}} \text{ Hz} \tag{1}$$

In discontinuous conduction mode, current through the inductor ramps up from zero to a peak value during the on-time, then ramps back to zero before the end of the off-time. The next on-time interval starts when the voltage at FB falls below V_{SS}. When the inductor current is zero during the high-side FET off-time, the load current is supplied by the output capacitor. In this mode, the operating switching frequency is lower than the continuous conduction mode switching frequency and the frequency varies with load. Discontinuous conduction mode maintains conversion efficiency at light loads because the switching losses reduce with the decrease in load and frequency.

The output voltage is set by two external resistors (R_{FB1}, R_{FB2}). Calculate the regulated output voltage from Equation 2.

$$V_{OUT} = \frac{V_{REF} \times (R_{FB2} + R_{FB1})}{R_{FB1}} \text{ V} \tag{2}$$

where

- V_{REF} = 2 V (typical) is the feedback reference voltage.

7.3.2 VCC Regulator

The LM5160-Q1 contains an internal high-voltage linear regulator with a nominal output voltage of 7.5 V (typical). The VCC regulator is internally current limited to 30 mA (minimum). This regulator supplies power to internal circuit blocks including the synchronous FET gate driver and the logic circuits. When the VCC voltage reaches the undervoltage lockout ($V_{CC(UV)}$) threshold of 3.98 V (typical), the IC is enabled. An external capacitor at the VCC pin stabilizes the regulator and supplies transient VCC current to the gate drivers. An internal diode connected from VCC to BST replenishes the charge in the high-side gate drive bootstrap capacitor when the SW voltage is low.

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Feature Description (continued)

7.3.3 Regulation Comparator

The feedback voltage at the FB pin is compared to the SS pin voltage V_{SS}. In normal operation when the output voltage is in regulation, an on-time interval is initiated when the voltage at FB pin falls below V_{SS}. The high-side buck switch stays on for a pre-defined on-time causing the FB voltage to rise. After the on-time interval expires, the high-side switch remains off until the FB voltage falls below V_{SS}. During start-up, the FB voltage is below V_{SS} at the end of each on-time interval and the high-side switch turns on again after the minimum forced off-time of 170 ns (typical). When the output is shorted to ground (V_{FB} = 0 V), the high-side peak current limit is triggered, the high-side FET is turned off and remains off for a period determined by the current limit off-timer. See *Current Limit* for additional information.

7.3.4 Soft Start

The soft-start feature of the LM5160-Q1 allows the converter to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. When the EN/UVLO voltage is above the EN/UVLO standby threshold $V_{UVLO(TH)}$ = 1.24 V (typical) and the VCC voltage exceeds the VCC undervoltage threshold, $V_{CC(UV)}$ = 3.98 V (typical) , an internal 10-µA current source charges the external capacitor at the SS pin (C_{SS}) from 0 V to 2 V. The voltage at SS is the noninverting input of the internal FB comparator. The soft-start interval ends when the SS capacitor is charged to the 2-V reference level. The ramping voltage at SS produces a controlled, monotonic output voltage start-up. Use a minimum soft-start capacitance of 1 nF for all applications.

7.3.5 Error Amplifier

The LM5160-Q1 provides a transconductance (G_M) error amplifier that minimizes the difference between the reference voltage (V_{REF}) and the average feedback (FB) voltage. This amplifier reduces the load and line regulation errors that are common in constant on-time regulators. The soft-start capacitor C_{SS} provides compensation for this error correction loop. The soft-start capacitor must be greater than 1 nF to ensure stability.

7.3.6 On-Time Generator

The on-time of the LM5160-Q1 high-side MOSFET is determined by the R_{ON} resistor and is inversely proportional to the input voltage (V_{IN}). The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. Calculate the on-time from Equation 3 with R_{ON} expressed in Ohms.

$$T_{ON} = \frac{R_{ON} \times 1 \times 10^{-10}}{V_{IN}} \text{ s} \tag{3}$$

To set a specific continuous conduction mode switching frequency (F_{SW} expressed in Hz), determine the R_{ON} resistor from Equation 4.

$$R_{ON} = \frac{V_{OUT}}{F_{SW} \times 1 \times 10^{-10}} \ \Omega \tag{4}$$

R_{ON} must be selected for a minimum on-time (at maximum V_{IN}) greater than 150 ns for proper operation. This minimum on-time requirement limits the maximum switching frequency of applications with relatively high V_{IN} and low V_{OUT}.

7.3.7 Current Limit

The LM5160-Q1 provides an intelligent current limit off-timer that adjusts the off-time to reduce the foldback in the current limit. If the peak value of the current in the buck switch exceeds 2.5 A (typical), the present on-time interval is immediately terminated and a non-resettable off-timer is initiated. The length of the off-time is controlled by the FB voltage and the input voltage V_{IN}. As an example, when V_{FB} = 0 V and V_{IN} = 24 V, the off-time is set to 10 µs. This condition occurs if the output is shorted or during the initial phase of start-up. In cases of output overload where the FB voltage is greater than zero volts (a soft short), the current limit off-time is reduced. Decreasing the off-time during less severe overloads reduces the current limit foldback, overload recovery time, and start-up time. Calculate the current limit off-time using Equation 5.

$$T_{OFF(CL)} = \frac{5V_{IN}}{24V_{FB} + 12} \ \mu\text{s} \tag{5}$$

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Feature Description (continued)

7.3.8 N-Channel Buck Switch and Driver

The LM5160-Q1 integrates an N-channel buck switch and associated floating high-side gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage bootstrap diode. A 10-nF or larger ceramic capacitor connected between BST and SW provides the voltage to the high-side driver during the buck switch on-time. During the off-time, the SW node is pulled down to approximately 0 V and the bootstrap capacitor charges from VCC through the internal bootstrap diode. The minimum off-time of 170 ns (typical) provides a minimum time each cycle to recharge the bootstrap capacitor.

7.3.9 Synchronous Rectifier

The LM5160-Q1 provides an internal low-side synchronous rectifier N-channel FET. This low-side FET provides a low resistance path for the inductor current when the high-side FET is turned off.

With the FPWM pin connected to ground or left floating, the LM5160-Q1 synchronous rectifier operates in diode emulation mode. Diode emulation enables the pulse-skipping during light load conditions. This leads to a reduction in the average switching frequency at light loads. Switching losses and FET gate driver losses, both of which are proportional to switching frequency, are significantly reduced and efficiency is improved. This pulse-skipping mode also reduces the circulating inductor currents and losses associated with a continuous conduction mode (CCM).

When FPWM is pulled high, diode emulation is disabled. The inductor current can flow in either direction through the low-side FET, resulting in CCM operation with nearly constant switching frequency. A negative sink current limit circuit limits the current that can flow into SW and through the low-side FET to ground. In a buck regulator application, large negative current typically only flows from V_{OUT} to SW if V_{OUT} is lifted above the output regulation setpoint.

7.3.10 Enable / Undervoltage Lockout (EN/UVLO)

The LM5160-Q1 contains a dual-level undervoltage lockout (EN/UVLO) circuit. When the EN/UVLO voltage is below 0.35 V, the regulator is in a low-current shutdown mode. When the EN/UVLO voltage is greater than 0.35 V (typical) but less than 1.24 V (typical), the regulator is in standby mode. In standby mode, the VCC bias regulator is active but converter switching remains disabled. When the voltage at the VCC exceeds the VCC rising threshold, $V_{CC(UV)}$ = 3.98 V (typical), and the EN/UVLO voltage is greater than 1.24 V, normal switching operation begins. Use an external resistor voltage divider from VIN to GND to set the minimum operating voltage of the regulator.

EN/UVLO hysteresis is implemented with an internal 20 µA (typical) current source ($I_{UVLO(HYS)}$) that is switched on or off into the impedance of the EN/UVLO pin resistor divider. When the EN/UVLO threshold is exceeded, the current source is activated to effectively raise the voltage at the EN/UVLO pin. The hysteresis is equal to the value of this current times the upper resistance of the resistor divider, R_{UV2}. See *Functional Block Diagram*.

7.3.11 Thermal Protection

The LM5160-Q1 must be operated such that the junction temperature does not exceed 150°C during normal operation. An internal thermal shutdown circuit is provided to protect the LM5160-Q1 in the event of higher than normal junction temperature. When activated, typically at 175°C, the controller is forced into a low-power reset state, disabling the high-side buck switch and the VCC regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature falls below 155°C (typical hysteresis of 20°C), the VCC regulator is enabled and operation resumes.

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7.4 Device Functional Modes

7.4.1 Forced Pulse Width Modulation (FPWM) Mode

The *Synchronous Rectifier* section gives a brief introduction to the LM5160-Q1 diode emulation feature. The FPWM pin allows the power supply designer to select either CCM or DCM operation at light loads. When FPWM is connected to ground or left floating (FPWM = 0), a pulse-skipping mode and a zero-cross current detector circuit are enabled. The zero-cross detector turns off the low-side FET when the inductor current falls to zero (I_{ZX}, see *Electrical Characteristics*). This feature allows the LM5160-Q1 regulator to operate in DCM mode at light loads. In the DCM state, the switching frequency decreases with lighter loads.

If FPWM is pulled high (FPWM connected to VCC), the LM5160-Q1 operates in CCM even at light loads. This option allows the synchronous rectifier FET to conduct until the start of the next high-side switch cycle. The inductor current drops to zero and then reverse direction (negative direction through inductor), passing from drain to source of the low-side FET. The current flows continuously until the FB comparator initiates another high-side switch on-time. CCM operation reduces efficiency at light load but improves the transient response to step load changes and provides nearly constant switching frequency.

Table 1. FPWM Pin Mode Summary

FPWM PIN CONNECTION	LOGIC STAGE	DESCRIPTION
GND or Floating (High Z)	0	The FPWM pin is grounded or left floating. DCM enabled at light loads.
V_{CC}	1	The FPWM pin is connected to VCC. The LM5160-Q1 then operates in CCM mode at light loads.

7.4.2 Undervoltage Detector

The following table summarizes the dual threshold levels of the undervoltage lockout (EN/UVLO) circuit explained in *Enable / Undervoltage Lockout (EN/UVLO)*.

Table 2. UVLO Pin Mode Summary

EN/UVLO PIN VOLTAGE	VCC REGULATOR	MODE	DESCRIPTION
< 0.35 V	Off	Shutdown	V_{CC} regulator disabled. High-side and low-side FETs disabled.
0.35 V to 1.24 V	On	Standby	V_{CC} regulator enabled. High-side and low-side FETs disabled.
> 1.24 V	$V_{CC} < V_{CC(UV)}$	Standby	V_{CC} regulator enabled. High-side and low-side FETs disabled.
	$V_{CC} > V_{CC(UV)}$	Operating	V_{CC} regulator enabled. Switching enabled.

If input UVLO is not required, EN/UVLO can be driven by a logic signal as an enable input or connected directly to VIN. If EN/UVLO is directly connected to VIN, the regulator begins switching when $V_{CC(UV)}$ = 3.98 V (typical) is satisfied.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5160-Q1 is a synchronous buck or Fly-Buck DC/DC converter designed to operate over wide input voltage and output current ranges. LM5160-Q1 quick-start calculator tools are available for download to design a single-output synchronous buck converter or an isolated dual-output Fly-Buck converter. For a detailed design guide of the Fly-Buck converter, refer to *AN-2292 Designing an Isolated Buck (Fly-Buck) Converter* application report (SNVA674). Alternatively, use online WEBENCH software to create a complete buck or Fly-Buck design and generate the bill of materials, estimated efficiency, solution size and cost of the complete solution.

Typical Applications describes a few application circuits using the LM5160-Q1 with detailed, step-by-step design procedures.

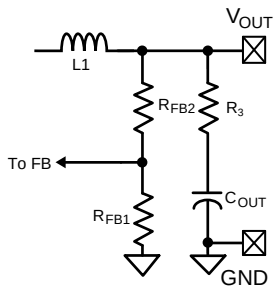
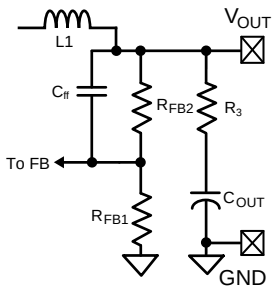
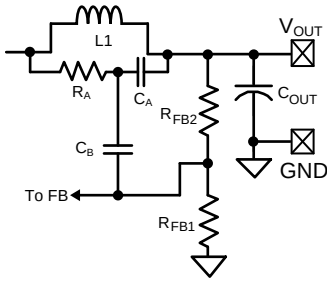
8.1.1 Ripple Configuration

The LM5160-Q1 uses an adaptive constant on-time (COT) control scheme in which the PWM on-time is set by a one-shot timer and the off-time is set by the feedback voltage (V_{FB}) falling below the reference voltage. Therefore, for stable operation, the feedback voltage must decrease monotonically in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during the off-time must be large enough to dominate any noise present at the feedback node.

Table 3 presents three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple from the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor ripple current charging or discharging the output capacitor.
2. Resistive ripple caused by the inductor ripple current flowing through the ESR of the output capacitor and R3.

Table 3. Ripple Configurations

TYPE 1	TYPE 2	TYPE 3
Lowest Cost	Reduced Ripple	Minimum Ripple
		
$R_3 \geq \frac{25\ mV \times V_O}{V_{REF} \times \Delta I_{L1,min}}$ (6)	$C_{ff} \geq \frac{5}{F_{SW} \times (R_{FB2} \text{ II } R_{FB1})}$ $R_3 \geq \frac{25\ mV}{\Delta I_{L1,min}}$ (7)	$R_A C_A \leq \frac{(V_{IN,min} - V_O) \times T_{ON(@\ V_{IN,min})}}{25mV}$ (8)

The capacitive ripple is out-of-phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at output (V_{OUT}) for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses a ripple injection circuit with R_A, C_A and the switch-node (SW) voltage to generate a triangular ramp. This ramp is then AC-coupled into the feedback node (FB) using coupling capacitor C_B. Because this circuit does not use the output voltage ripple, it is suited for applications where low output voltage ripple is imperative. For more information on each ripple generation method, refer to the *AN-1481 Controlling Output Ripple & Achiev ESR Indep Constant On-Time Regulator Designs* application note.

8.2 Typical Applications

TIDesigns

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation and test results of an LM5160-powered implementation, refer to *Wide-Input Isolated IGBT Gate-Drive Fly-Buck Power Supply for Three-Phase Inverters* reference design.

8.2.1 LM5160-Q1 Synchronous Buck (10-V to 60-V Input, 5-V Output, 1.5-A Load)

A typical application example is a synchronous buck converter operating from a wide input voltage range of 10 V to 65 V and providing a stable 5-V output voltage with output current capability of 1.5 A. Figure 19 shows the complete schematic for a typical synchronous buck application circuit. The components are labeled by numbers instead of the descriptive name used in the previous sections. For example, R3 represents R_{ON} and so forth.

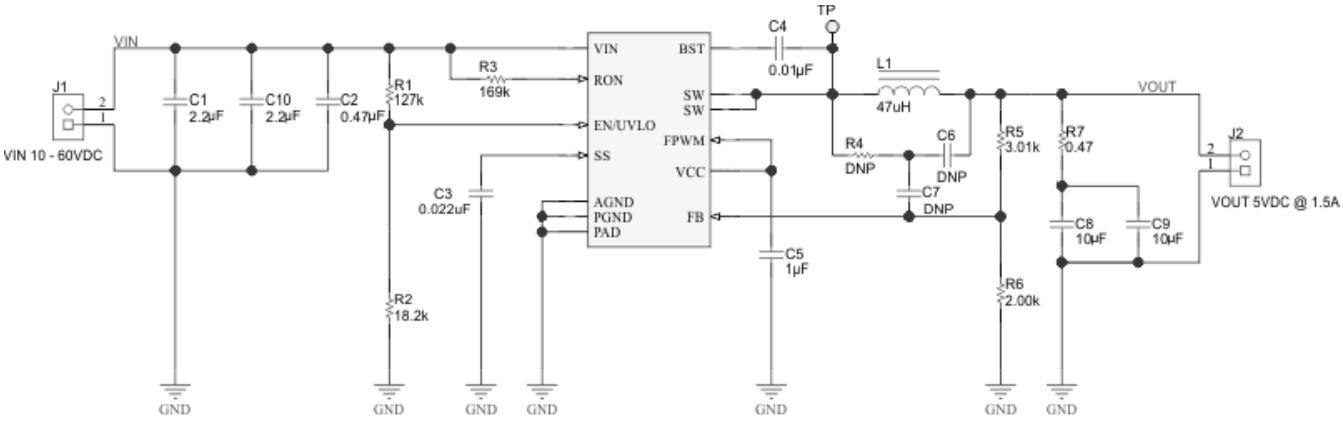


Figure 19. LM5160-Q1 Synchronous Buck Application Circuit

NOTE

This and subsequent design examples are provided herein to showcase the LM5160-Q1 converter in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor may be required at the input to ensure stability, particularly at low input voltage and high output current operating conditions. See *Power Supply Recommendations* for more detail.

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8.2.1.1 Design Requirements

Table 4 summarizes the operating parameters:

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10 V to 65 V
Output	5 V
Load current	1.5 A
Nominal switching frequency	300 kHz
Light-load operating mode	CCM, FPWM = VCC

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5160-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Feedback Resistor Divider - R_{FB1}, R_{FB2}

With the required output voltage setpoint at 5 V and V_{FB} = 2 V (typical), calculate the ratio of R6 (R_{FB1}) to R5 (R_{FB2}) using Equation 9.

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{V_{REF}} - 1 \tag{9}$$

The resistor ratio calculates to be 3:2. Choose standard values of R6 (R_{FB1}) = 2 kΩ and R5 (R_{FB2}) = 3.01 kΩ. Higher or lower values can be used as long as a ratio of the 3:2 is maintained.

8.2.1.2.3 Switching Frequency - R_{ON}

The duty cycle required to maintain output regulation at the minimum input voltage restricts the maximum switching frequency of the LM5160-Q1. The maximum value of the minimum forced off-time, $T_{OFF,min}$, limits the duty cycle and therefore the switching frequency. Calculate the maximum frequency that avoids output dropout at minimum input voltage using Equation 10.

$$F_{SW,\,max\,(@\,V_{IN,\,min})} = \frac{V_{IN,\,min} - V_{OUT}}{V_{IN,\,min} \times T_{OFF,\,min}(ns)} \tag{10}$$

For this design example, the maximum frequency based on the minimum off-time limitation of $T_{OFF,min}$ (typical) = 170 ns is calculated as $F_{SW,max(@VIN,min)}$ = 2.9 MHz. This value is well above 1 MHz, the maximum possible operating frequency of the LM5160-Q1.

At maximum input voltage the maximum switching frequency of the LM5160-Q1 is restricted by the minimum on-time, $T_{ON,min}$ which limits the minimum duty cycle of the converter. Calculate the maximum frequency at maximum input voltage using Equation 11.

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$$F_{SW,\,max\,(@\,V_{IN,\,max})} = \frac{V_{OUT}}{V_{IN,\,max} \times T_{ON,\,min}(ns)} \quad (11)$$

Using Equation 11 and $T_{ON,min}$ (typical) = 150 ns, the maximum achievable switching frequency is $F_{SW,max(@VIN,min)}$ = 514 kHz. Taking this value as the maximum possible switching frequency over the input voltage range for this application, choose a nominal switching frequency of F_{SW} = 300 kHz for this design. The value of resistor R_{ON} sets the nominal switching frequency based on Equation 12.

$$R_{ON} = \frac{V_{OUT}}{F_{SW} \times 1 \times 10^{-10}}\ \Omega \quad (12)$$

For this particular application with F_{SW} = 300 kHz, R_{ON} calculates to be 167 kΩ. Selecting a standard value for R3 (R_{ON}) = 169 kΩ (±1%) results in a nominal frequency of 296 kHz. The resistor value may need to adjusted further in order to achieve the required switching frequency as the switching frequency in COT converters varies slightly (±10%) with input voltage and/or output current. Operation at a lower nominal switching frequency results in higher efficiency but increases the inductor and capacitor values leading to a larger total solution size.

8.2.1.2.4 Inductor - L

Select the inductor to limit the inductor ripple current between 20 and 40 percent of the maximum load current. Calculate the minimum value of the inductance required in this application from Equation 13.

$$L_{min} = \frac{V_O \times (V_{IN,\,max} - V_O)}{V_{IN,\,max} \times F_{SW} \times I_{O,\,max} \times 0.4} \quad (13)$$

Based on Equation 13, determine the minimum value of the inductance as 26 µH for V_{IN} = 65 V (maximum) and inductor ripple current equal to 40 percent of the maximum load current. Allowing some margin for inductance variation with current, select a higher standard value of L1 (L) = 47 µH for this design.

The peak inductor current at maximum load must be smaller than the minimum current limit threshold of the high-side FET, as given in *Electrical Characteristics* table. Determine the inductor ripple current at any input voltage using Equation 14.

$$\Delta I_L = \frac{V_O \times (V_{IN} - V_O)}{V_{IN} \times F_{SW} \times L} \quad (14)$$

Calculate the peak-to-peak inductor ripple current as 180 mA and 332 mA at the minimum and maximum input voltages, respectively. Determine the maximum peak inductor current in the buck FET using Equation 15.

$$I_{L(peak)} = I_{O,\,max} + \frac{\Delta I_{L,\,max}}{2} \quad (15)$$

In this design with an output current of 1.5 A, the maximum peak inductor current is calculated to be approximately 1.67 A, which is less than the high-side FET minimum current limit threshold.

The saturation current of the inductor must also be carefully considered. The peak value of the inductor current is bound by the high-side FET current limit during overload or short circuit conditions. Based on the high-side FET current limit specification in *Electrical Characteristics*, select an inductor with saturation current rating above 2.875 A.

8.2.1.2.5 Output Capacitor - C_{OUT}

Select the output capacitor to limit the capacitive ripple at the output of the regulator. Maximum capacitive ripple is observed at maximum input voltage. The output capacitance required for a ripple voltage ΔV_O across the capacitor is given by Equation 16.

$$C_{OUT} = \frac{\Delta I_{L,\,max}}{8 \times F_{SW} \times \Delta V_{O,\,ripple}} \quad (16)$$

Substituting $\Delta V_{O,\ ripple}$ = 10 mV gives C_{OUT} = 14 µF. Two standard 10-µF ceramic capacitors in parallel (C8, C9) are selected. An X7R type capacitor with a voltage rating 16 V or higher must be used for C_{OUT} (C8, C9) to limit the reduction of capacitance due to DC bias voltage.

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8.2.1.2.6 Series Ripple Resistor - R_{ESR}

Select the series resistor such that sufficient ripple is injected at the feedback node (FB). The ripple voltage produced by R_{ESR} is proportional to the inductor ripple current. Therefore, select R_{ESR} based on the lowest inductor ripple current occurring at minimum input voltage. Calculate R_{ESR} usingEquation 17.

$$R_{ESR} \geq \frac{25\ mV \times V_O}{V_{REF} \times \Delta I_{L,\,min}} \tag{17}$$

With V_O = 5 V, V_{REF} = 2 V and $\Delta I_{L,\ min}$ = 180 mA (at $V_{IN,\ min}$= 10 V) as calculated in Equation 14, Equation 17 requires an R_{ESR} greater than or equal to 0.35 Ω. Selecting R7 (R_{ESR}) = 0.47 Ω results in approximately 150 mV of maximum output voltage ripple at $V_{IN,max}$. For applications requiring lower output voltage ripple, use Type II or Type III ripple injection circuits as described in *Ripple Configuration*.

8.2.1.2.7 VCC and Bootstrap Capacitors - C_{VCC}, C_{BST}

The VCC capacitor charges the bootstrap capacitor during the off-time of the high-side switch and powers internal logic circuits and the low-side sync FET gate driver. The bootstrap capacitor biases the high-side gate driver during the high-side FET on-time. Recommended values for C5 (C_{VCC}) and C4 (C_{BST}) are 1 µF and 10 nF, respectively. Both must be high-quality X7R ceramic capacitors.

8.2.1.2.8 Input Capacitor - C_{IN}

The input capacitor must be large enough to limit the input voltage ripple to an acceptable level. Equation 18 provides the input capacitance C_{IN} required for a worst-case input ripple of $\Delta V_{IN,\ ripple}$.

$$C_{IN} = \frac{I_{O,\,max} \times D \times (1-D)}{\Delta V_{IN,\,ripple} \times F_{SW}} \tag{18}$$

C_{IN} (C1, C10) supplies most of the switch current during the on-time to limit the voltage ripple at the VIN pin. At maximum load current, when the buck switch turns on, the current into the VIN pin quickly increases to the valley current of the inductor ripple and then ramps up to the peak of the inductor ripple during the on-time of the high-side FET. The average current during the on-time is the output load current. For a worst-case calculation, C_{IN} must supply this average load current during the maximum on-time, without letting the voltage at VIN drop more than the desired input ripple. For this design, the input voltage drop is limited to 0.5 V and the value of C_{IN} is calculated using Equation 18.

Based on Equation 18, the value of the input capacitor is determined as approximately 2.5 µF at D = 0.5. Taking into account the decrease in capacitance with applied voltage, two standard value 2.2-µF, 100-V, X7R ceramic capacitors are selected for C1 and C10. The input capacitors must be rated for the maximum input voltage under all operating and transient conditions.

A third input capacitor C2 may be needed in this design as a bypass path for the high-frequency components of input switching current. The value of C2 is 0.1 µF and this bypass capacitor must be placed directly across VIN and PGND (pins 3 and 2) near the IC. The C_{IN} values and location are critical to reducing switching noise and transients.

8.2.1.2.9 Soft-Start Capacitor - C_{SS}

The capacitor at the SS pin determines the soft-start time, that is, the time for the output voltage to reach its final steady-state value. Determine the SS capacitor value from Equation 19:

$$C_{SS} = \frac{I_{SS} \times T_{Startup}}{V_{SS}} \tag{19}$$

With C3 (C_{SS}) set at 22 nF and V_{SS} = 2 V, I_{SS} = 10 µA, $T_{Startup}$ is approximately 4 ms.

8.2.1.2.10 EN/UVLO Resistors - R_{UV1}, R_{UV2}

The UVLO resistors R1 (R_{UV2}) and R2 (R_{UV1}) set the input undervoltage lockout threshold and hysteresis according to Equation 20 and Equation 21.

$$V_{IN(HYS)} = I_{UVLO(HYS)} \times R_{UV2} \tag{20}$$

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$$V_{IN,\,UVLO(rising)} = V_{UVLO(TH)}\left(1+\frac{R_{UV2}}{R_{UV1}}\right) \quad (21)$$

From the *Electrical Characteristics* table, $I_{UVLO(HYS)}$ = 20 µA (typical). To design for a V_{IN} rising threshold ($V_{IN,\,UVLO(rising)}$) of 10 V and hysteresis of 2.5 V, Equation 20 and Equation 21 yield R_{UV1} = 17.98 kΩ and R_{UV2} = 125 kΩ. Selecting 1% standard values of R2 (R_{UV1}) = 18.2 kΩ and R1 (R_{UV2}) = 127 kΩ result in UVLO rising threshold and hysteresis voltages of 9.89 V and 2.54 V, respectively.

8.2.1.3 Application Curves

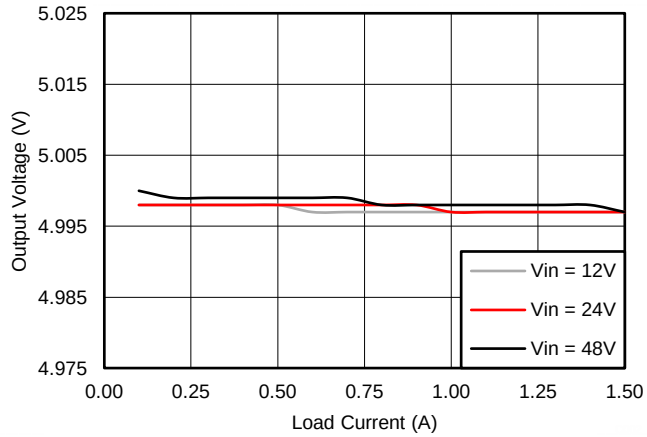

Figure 20. Load Regulation

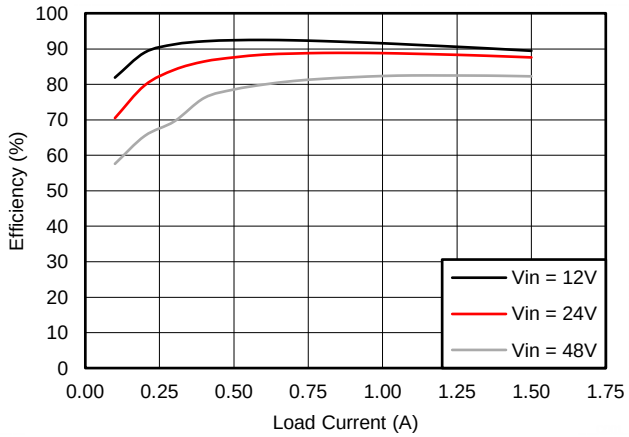

Figure 21. Efficiency vs I_{OUT}

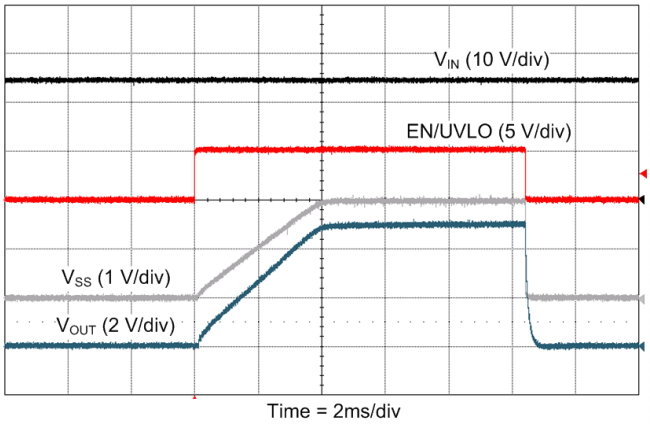

Figure 22. EN/UVLO Start-Up at V_{IN}= 24 V and I_{OUT} = 1 A

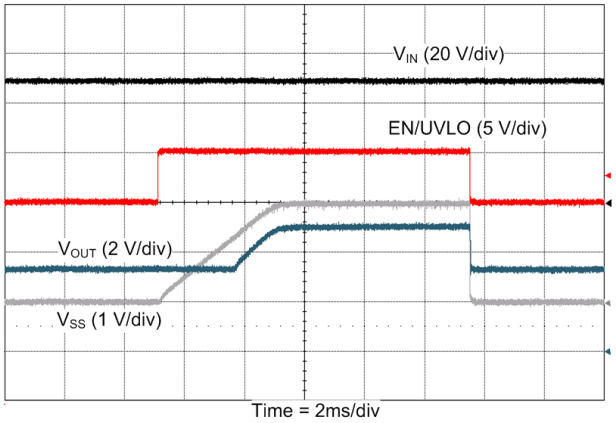

Figure 23. Prebias Start-Up at V_{IN}= 48 V and R_{LOAD} = 3 Ω

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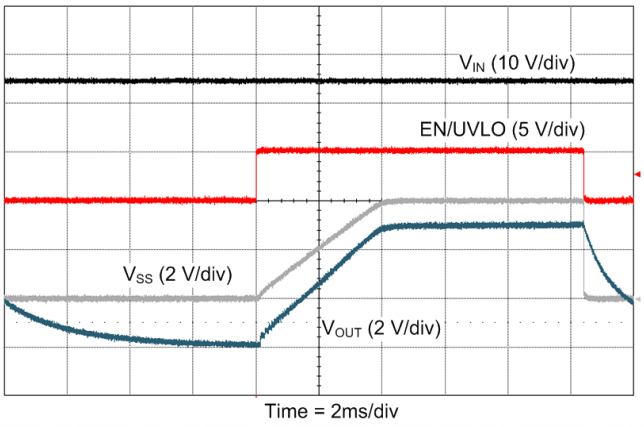

Figure 24. EN/UVLO Start-Up at V_{IN}= 24 V and R_{LOAD} = 100 Ω

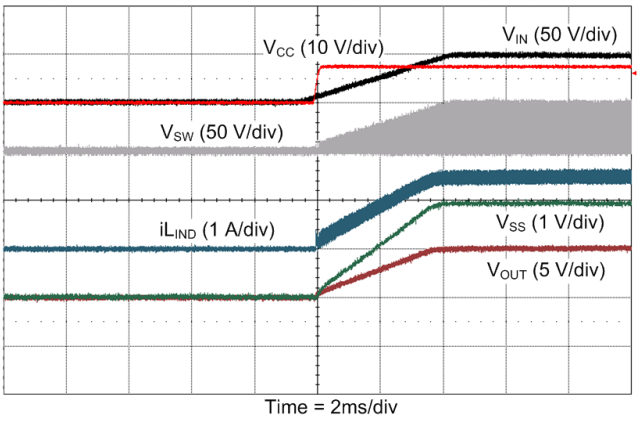

Figure 25. Start-Up at V_{IN}= 48 V and R_{LOAD} = 10 Ω

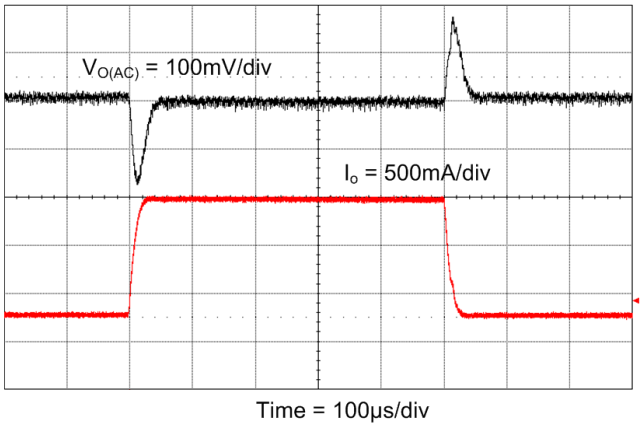

Figure 26. Load Transient (300 mA – 1.5 A) at V_{IN} = 24 V With Type 3 Ripple Configuration

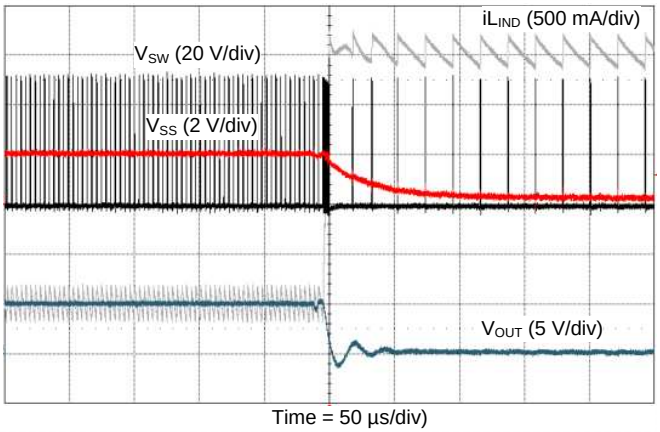

Figure 27. Output Short-Circuit at V_{IN} = 48 V

8.2.2 LM5160-Q1 Isolated Fly-Buck (18-V to 32-V Input, 12-V, 4.5-W Isolated Output)

For technical solutions, industry trends, and insights for designing and managing power supplies, please refer to TI's *Power House* blog series.

Below is an application example of an isolated Fly-Buck converter that operates over an input voltage range of 18 V to 32 V. It provides a stable 12-V isolated output voltage with an output power capability of 4.5 W. Figure 28 shows the complete schematic of the Fly-Buck application circuit.

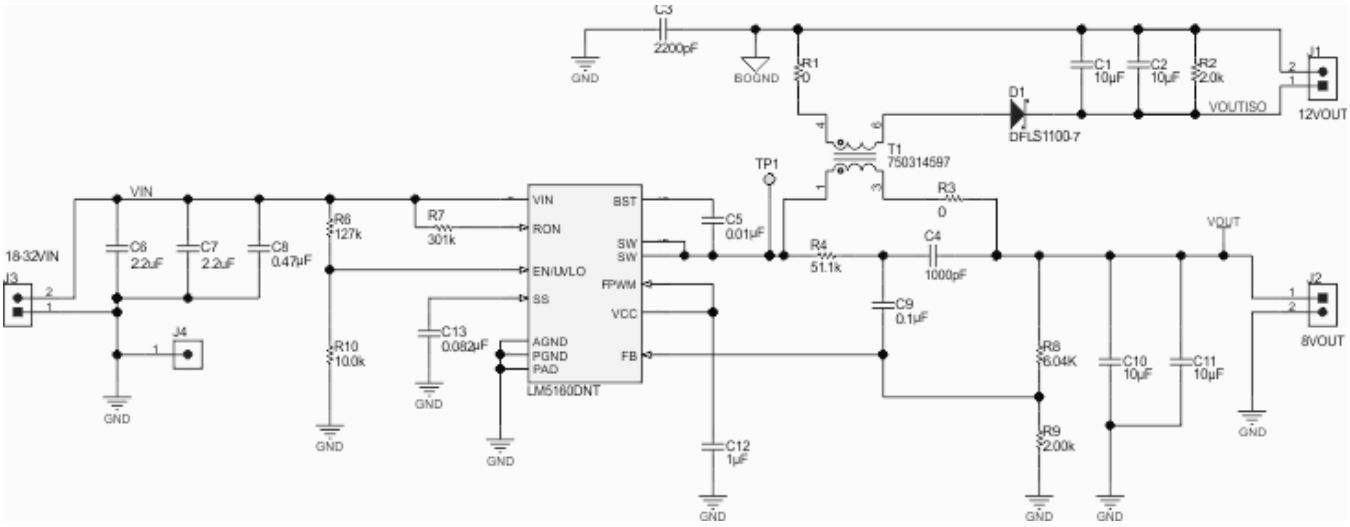

Figure 28. LM5160-Q1 12-V, 4.5-W Fly-Buck Converter Schematic

8.2.2.1 LM5160-Q1 Fly-Buck Design Requirements

This LM5160-Q1 Fly-Buck application example is designed to operate from a 24-V DC supply with line variations from 18 V to 32 V. The example provides a space-optimized and efficient 12-V isolated output solution with secondary load current capability from 0 mA to 400 mA. The primary side remains unloaded in this application. The switching frequency is set at 300 kHz (nominal). This design achieves greater than 88% peak efficiency.

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	18 V to 32 V
Isolated output	12 V
Isolated load current range	0 mA to 400 mA
Nominal switching frequency	300 kHz
Peak Efficiency	88%

8.2.2.2 Detailed Design Procedure

The Fly-Buck converter design procedure closely follows the buck converter design outlined in *LM5160-Q1 Synchronous Buck (10-V to 60-V Input, 5-V Output, 1.5-A Load)*. The selection of primary output voltage, transformer turns ratio, rectifier diode, and output capacitors are covered here.

8.2.2.2.1 Selection of V_{OUT1} and Turns Ratio

The primary-side output voltage of a Fly-Buck converter must be no more than one half of the minimum input voltage. For a minimum V_{IN} of 18 V, the primary output voltage (V_{OUT}) must be no higher than 9 V. To generate an isolated output voltage of $V_{OUT(ISO)}$ = 12 V, a transformer turns ratio of 1 : 1.5 (N1 : N2) is selected. Using this turns ratio, calculate the required primary output voltage V_{OUT} using Equation 22.

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$$V_{OUT} = \frac{V_{OUT(ISO)} + 0.7\ V}{1.5} = 8.47\ V \quad (22)$$

The 0.7 V subtracted from $V_{OUT(ISO)}$ represents the forward voltage drop of the secondary rectifier diode. Fine tuning the primary side V_{OUT1} may be required to account for voltage errors due to the leakage inductance of the transformer and the resistance of the transformer windings and the low-side MOSFET of the LM5160-Q1.

8.2.2.2.2 Secondary Rectifier Diode

The secondary rectifier diode must block the maximum input voltage multiplied by the transformer turns ratio. Determine the minimum diode reverse voltage $V_{R(diode)}$ rating from Equation 23.

$$V_{R(diode)} = V_{IN(max)} \times \frac{N2}{N1} + V_{OUT(ISO)} = 32\ V \times 1.5 + 12\ V = 60\ V \quad (23)$$

Select a diode with 60 V or higher reverse voltage rating for this application. If the input voltage (V_{IN}) has transients above the normal operating maximum input voltage of 32 V, then the worst-case transient input voltage must be used in the diode voltage calculation given by Equation 23.

8.2.2.2.3 External Ripple Circuit

A Type 3 ripple circuit is required for Fly-Buck converter applications. The design procedure for ripple components is identical to that in a buck converter. See *Ripple Configuration* for ripple design information.

8.2.2.2.4 Output Capacitor - C_{OUT2}

The Fly-Buck output capacitor conducts higher ripple current than a buck converter output capacitor. Calculate the capacitive ripple for the isolated output capacitor based on the time the rectifier diode is off. During this time the entire output current is supplied by the output capacitor. Calculate the required capacitance for a worst-case V_{OUT2} ($V_{OUT(ISO)}$) ripple voltage using Equation 24.

$$C_{OUT2} = \frac{I_{OUT2}}{\Delta V_{OUT2}} \left(\frac{V_{OUT1}}{V_{IN(MIN)}} \right) \times \frac{1}{f_{sw}} \quad (24)$$

where

- ΔV_{OUT2} is the target ripple at the secondary output.

Equation 24 is an approximation and ignores the ripple components associated with ESR and ESL of the output capacitor. For a ΔV_{OUT2} = 100 mV, Equation 24 requires C_{OUT2} = 6.5 µF. When selecting a ceramic capacitor, consider its voltage coefficient to ensure sufficient capacitance at the output voltage operating point.

8.2.2.3 Application Curves

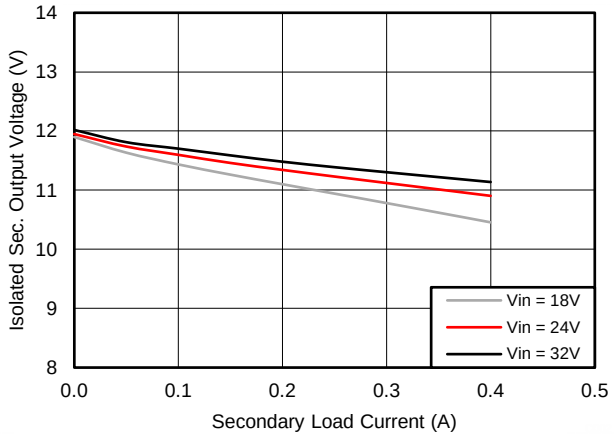

Figure 29. Load Regulation

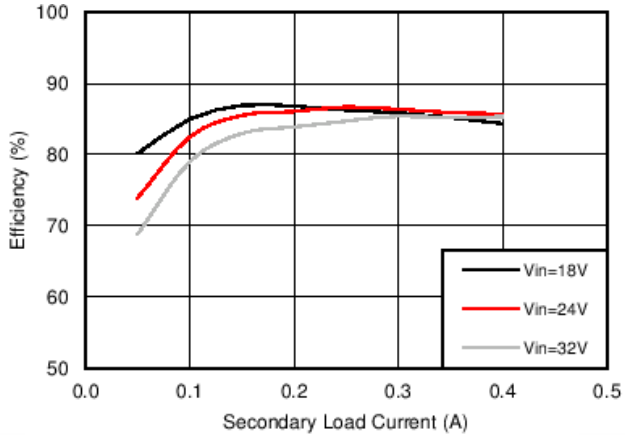

Figure 30. Efficiency vs I_{OUT2}

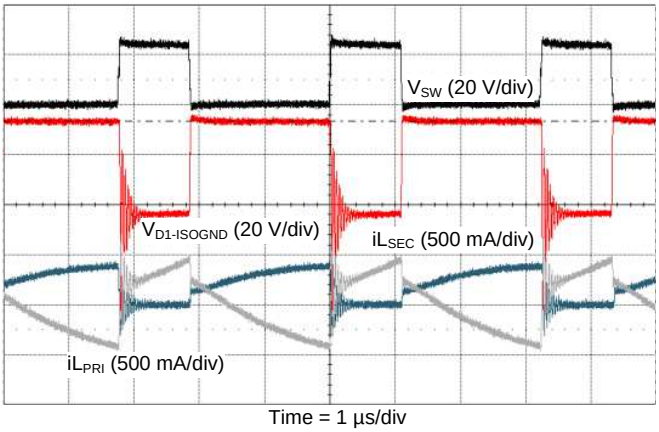

Figure 31. Primary Switch Node at V_{IN} = 24 V and I_{OUT2} = 200 mA

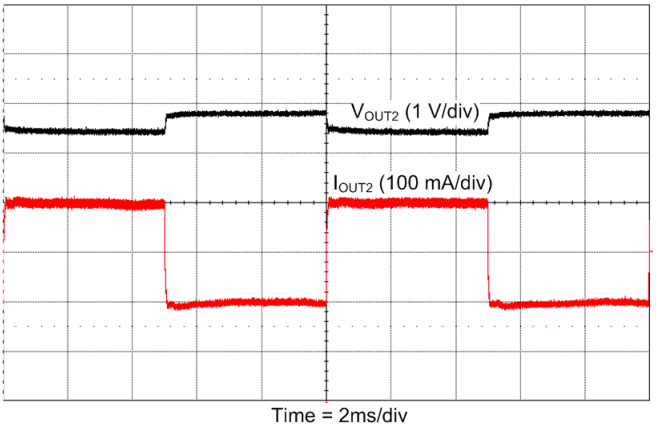

Figure 32. Load Transient at I_{OUT2} = 100 mA - 300mA

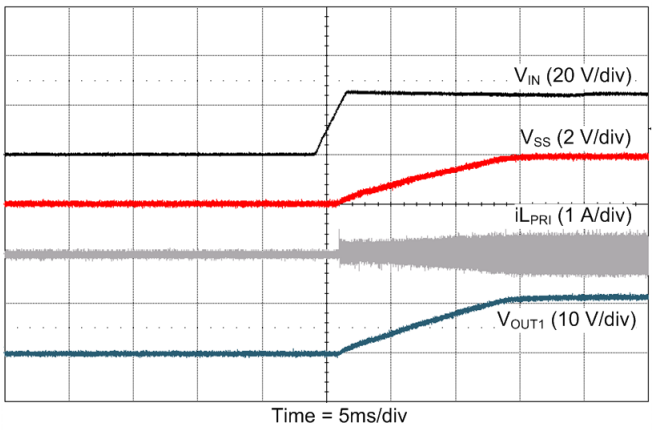

Figure 33. VIN Start-Up at I_{OUT2} = 200 mA

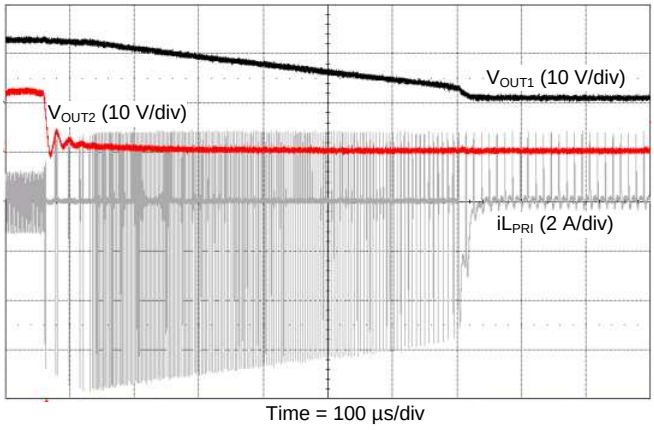

Figure 34. Secondary Short at I_{OUT2} = 600mA and I_{OUT1} = 200mA

8.3 Do's and Don'ts

As mentioned earlier in *Soft Start*, the SS capacitor C_{SS} must always be more than 1 nF in both buck and Fly-Buck converter applications. Apart from determining the start-up time, this capacitor serves as the external compensation of the internal G_M error amplifier. A minimum value of 1 nF is necessary to maintain stability. The SS pin must not be left floating.

The VCC pin of the LM5160-Q1 must not be biased with an external voltage source. When an improved efficiency requirement warrants an external V_{CC} bias, the LM5160A must be used.

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9 Power Supply Recommendations

The LM5160-Q1 DC/DC converter is designed to operate from a wide input voltage range of 4.5 V to 65 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with Equation 25.

$$I_{IN} = \frac{P_{OUT}}{V_{IN} \cdot \eta} \quad (25)$$

where

- η is the efficiency

If the regulator is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables may have an adverse affect on converter operation, particularly during operation at low input voltage. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled on and off. The parasitic resistance causes the input voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide input parallel damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The application report *Simple Success with Conducted EMI for DC-DC Converters* (SNVA489) provides helpful suggestions when designing an input filter for any switching regulator.

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10 Layout

10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. In particular, observe the following guidelines:

- C_{IN}: The loop consisting of input capacitor (C_{IN}), VIN pin and PGND pin carries the switching current. The input capacitor must be placed close to the IC, directly across VIN and PGND pins, and the connections to these two pins must be direct to minimize the switching power loop area. In general, it is not possible to place all of input capacitances near the IC. A good layout practice includes placing the bulk capacitor(s) as close as possible to the VIN pin (see Figure 35). A bypass capacitor measuring 0.1 µF must be placed directly across VIN and PGND (pin 3 and 2, respectively), as close as possible to the IC while complying with all layout design rules.
- C_{VCC} and C_{BST}: The VCC and bootstrap (BST) bypass capacitors supply switching currents to the high-side and low-side gate drivers. These two capacitors must also be placed as close to the IC as possible, and the connecting trace length and loop area must be minimized (see Figure 35).
- The feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of the LM5160-Q1. Therefore, take care while routing the feedback trace to avoid coupling any noise into this pin. In particular, the feedback trace must be short and not run close to magnetic components, or parallel to any other switching trace.
- SW trace: The SW node switches rapidly between VIN and GND every cycle and is therefore a source of noise. The SW node copper area must be minimized. In particular, the SW node must not be inadvertently connected to a copper plane or pour.

10.2 Layout Example

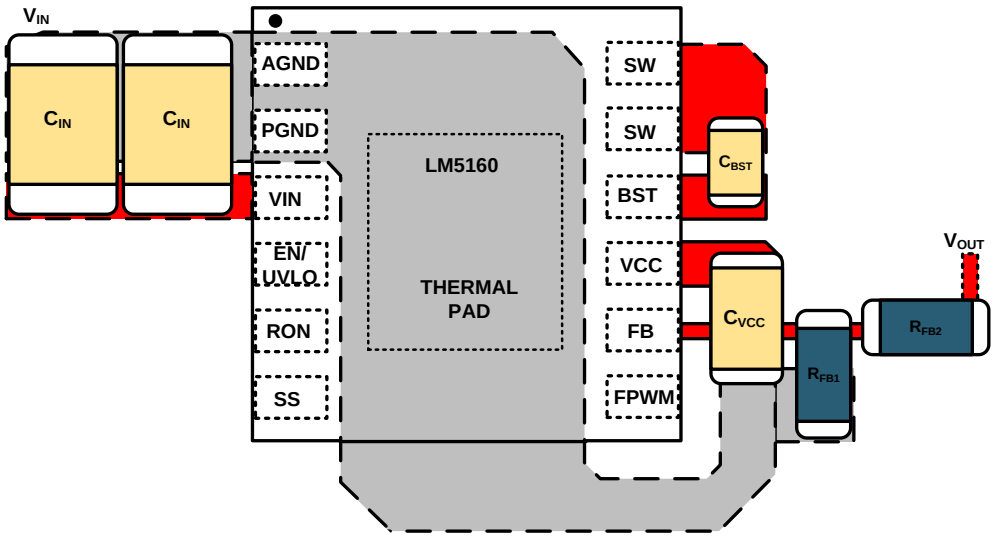

Figure 35. Placement of Bypass Capacitors

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11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.1.2 开发支持

相关开发支持，请参见以下文档：

- *LM5160 降压转换器快速入门计算器*
- *LM5160 Fly-Buck 转换器快速入门计算器*
- 《LM5160 PSpice 瞬态模型》
- 《LM5160 未加密 PSpice 瞬态模型》
- 《LM5160 TINA-TI Fly-Buck 参考设计》
- 有关 TI 的参考设计库，请访问 TIDesigns
- 有关 TI WEBENCH 设计环境，请访问 WEBENCH® 设计中心
- 要查看本产品的相关器件，请参阅 LM5161-Q1 100V 1A 同步降压转换器

11.1.2.1 使用 WEBENCH® 工具创建定制设计

请单击此处，使用 LM5160-Q1 器件及其 WEBENCH® 电源设计器创建定制设计。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.2 文档支持

11.2.1 相关文档

如需相关文档，请参阅以下内容：

- *《LM5160A、LM5160 降压 EVM 用户指南》*(SNVU441)
- *《LM5160 Fly-Buck（隔离降压）用户指南》*(SNVU408)
- *《AN-2292：设计隔离式降压 (Fly-buck) 转换器》*(SNVA674)
- *《AN-1481：在恒定导通时间稳压器设计中控制输出纹波并获得 ESR 非相关性》*(SNVA166)
- TI Designs：
  - *《适用于空气断路器的高分辨率、快速启动模拟前端参考设计》*(TIDUB80)
  - *《适用于三相逆变器的宽输入隔离式 IGBT 栅极驱动 Fly-Buck 电源》*(TIDU670)
  - *《适用于 25W PLC 控制器单元的输入保护和备用电源参考设计》*(TIDUCC7)
  - *《采用 24V 交流电源的非隔离式 RS-485 转 Wi-Fi 桥接器》*(TIDUA48)
  - *《采用 24V 交流电源的隔离式 RS-485 转 Wi-Fi 桥接器参考设计》*(TIDUA49)
  - *《具有超小型耦合电感器的双路输出隔离式 Fly-Buck 参考设计》*(TIDUC31)
  - *《2.5W 双极隔离型 Fly-Buck 超紧凑参考设计》*(TIDUCA3)
  - *《适用于模拟输入模块的小型隔离式直流/直流转换器参考设计》*(TIDUBR7)

文档支持 (接下页)

- *《适用于超声波的 2.3nV/√Hz 差动、时间增益控制 (TGC) DAC 参考设计》*(TIDUD38)
- *《用于确定绝缘电阻的泄漏电流测量参考设计》*(TIDU873)
- *《适用于 PoE 应用的第 3 类隔离式 Fly-Buck 电源模块参考设计》*(TIDU779)
- *《适用于 HEV/EV 牵引逆变器的 IGBT 模块热保护参考设计》*(TIDUBJ2)

- 白皮书：
  - *《使用 Fly-Buck 转换器设计隔离式动态轨》*
  - *《评估适用于具有成本效益的严苛应用的宽 V_{IN}、低 EMI 同步降压 电路》*
  - *《电源的传导 EMI 规格概述》*
  - *《电源的辐射 EMI 规格概述》*
- Power House 博客：
  - *Fly-Buck：常见问题解答 (FAQ)*
  - *借助 Fly-Buck 拓扑降低 EMI 并实现安静切换*
  - *Fly-Buck 转换器 PCB 布局提示*
  - *Fly-Buck 在何种情况下会成为满足您隔离式电源需求的最佳选择？*
  - *如何利用 Fly-Buck 转换器实现 EMC 和隔离设计*
  - *在 WEBENCH® 电源设计器创建 Fly-Buck 转换器*
- *《AN-2162：轻松解决直流/直流转换器的传导 EMI 问题》*(SNVA489)
- *《汽车启动仿真器用户指南》*(SLVU984)
- *《使用新的热指标》*(SBVA025)
- *《半导体和 IC 封装热指标》*(SPRA953)

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.5 商标

Fly-Buck, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
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11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5160QPWPQ1	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1
LM5160QPWPQ1.A	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1
LM5160QPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1
LM5160QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1
LM5160QPWPTQ1	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1
LM5160QPWPTQ1.A	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LM5160-Q1 :

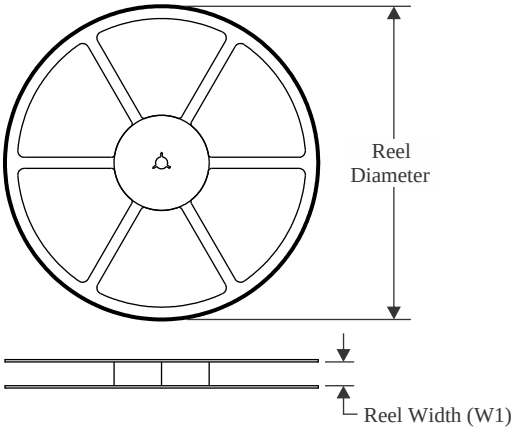
- Catalog : LM5160

NOTE: Qualified Version Definitions:

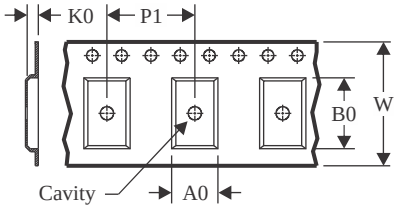
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

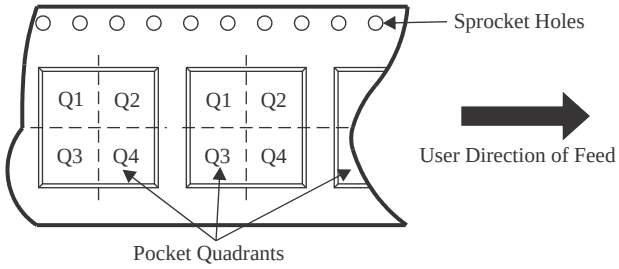


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

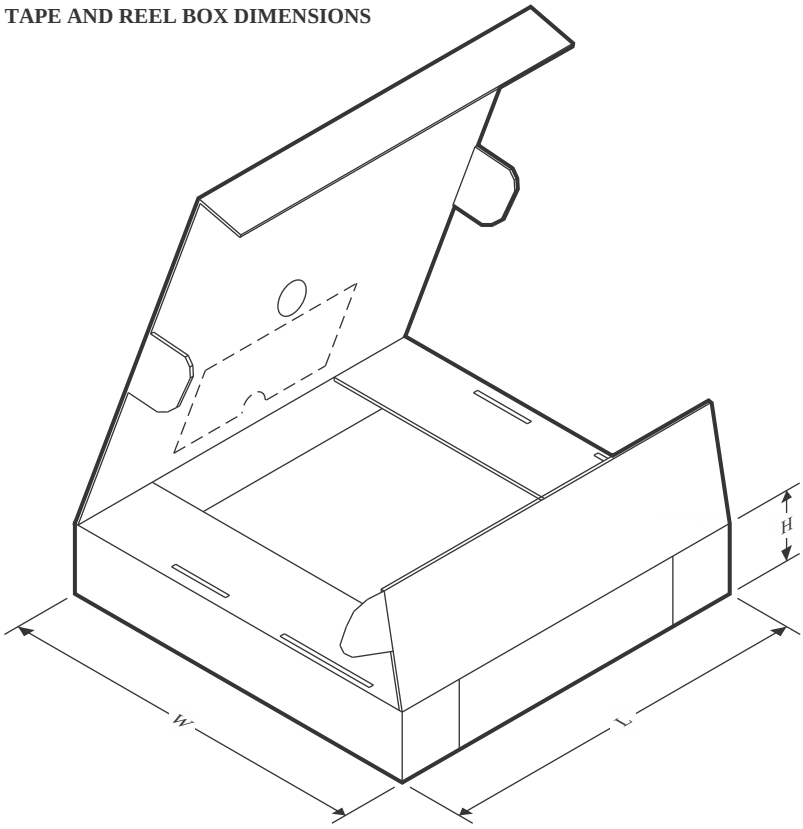
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5160QPWPRQ1	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5160QPWPTQ1	HTSSOP	PWP	14	250	177.8	12.4	6.9	5.6	1.6	8.0	12.0	Q1

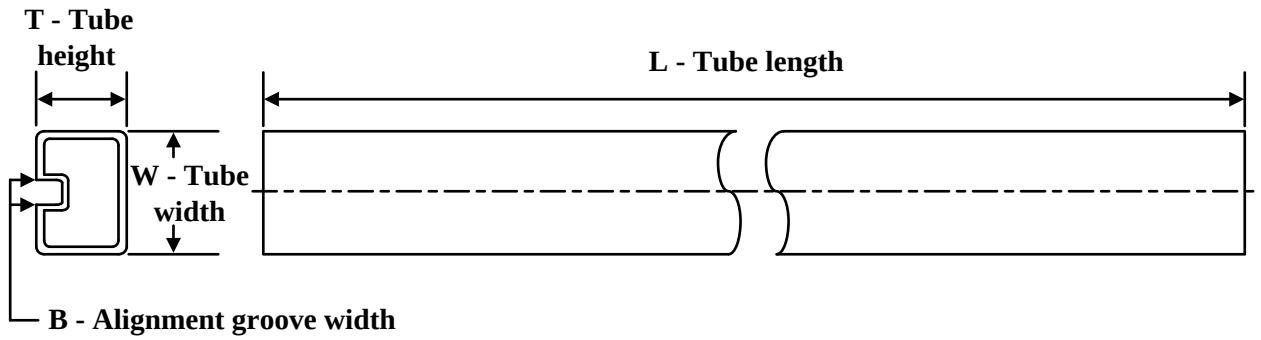
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

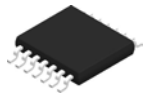
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5160QPWPRQ1	HTSSOP	PWP	14	2500	356.0	356.0	36.0
LM5160QPWPTQ1	HTSSOP	PWP	14	250	208.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5160QPWPQ1	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5160QPWPQ1.A	PWP	HTSSOP	14	94	495	8	2514.6	4.06

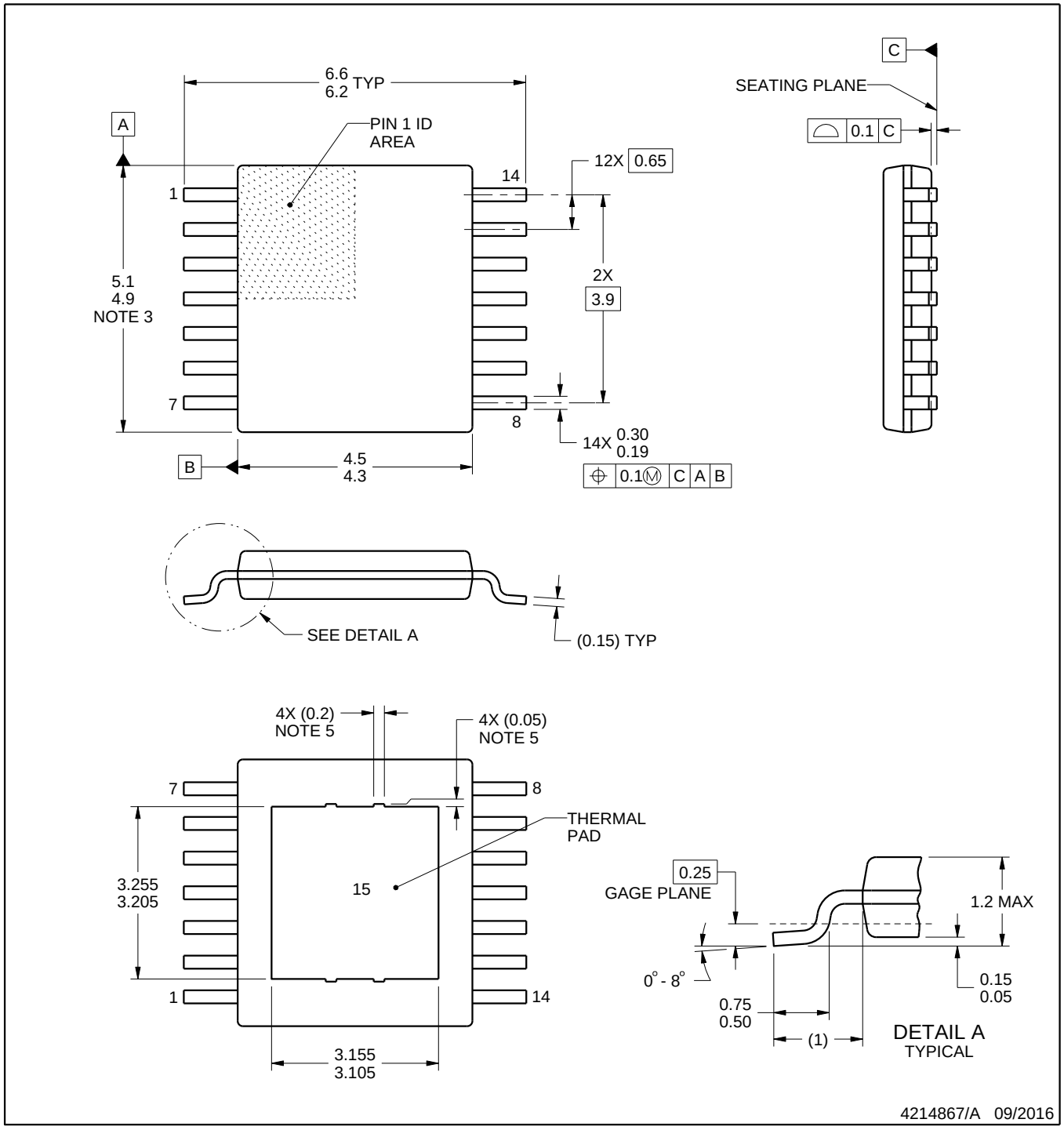


PACKAGE OUTLINE

PWP0014A

PowerPAD™ TSSOP - 1.2 mm max height

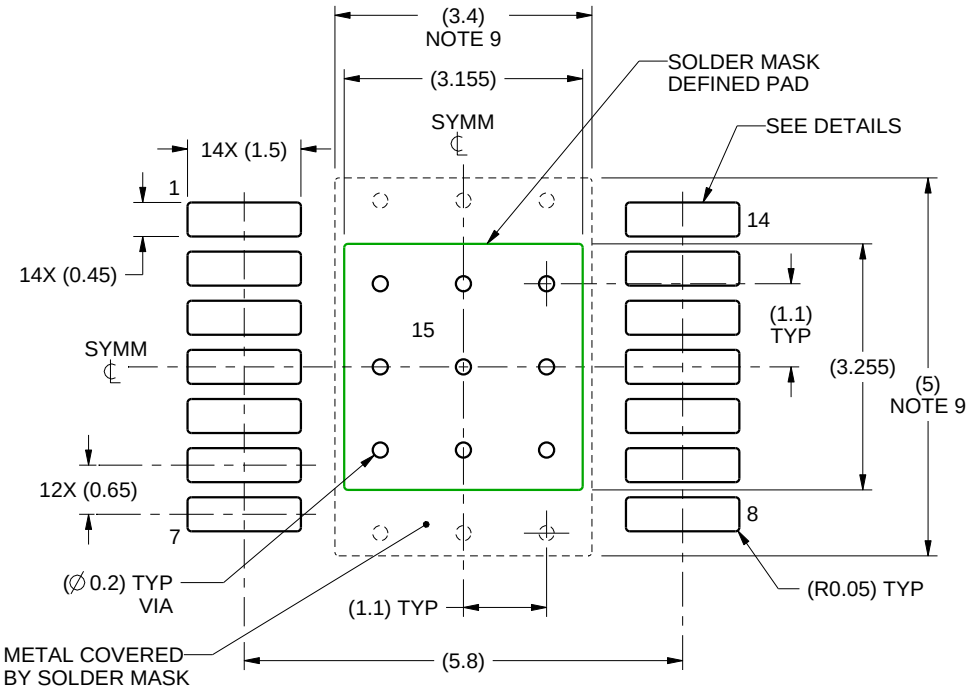
PLASTIC SMALL OUTLINE



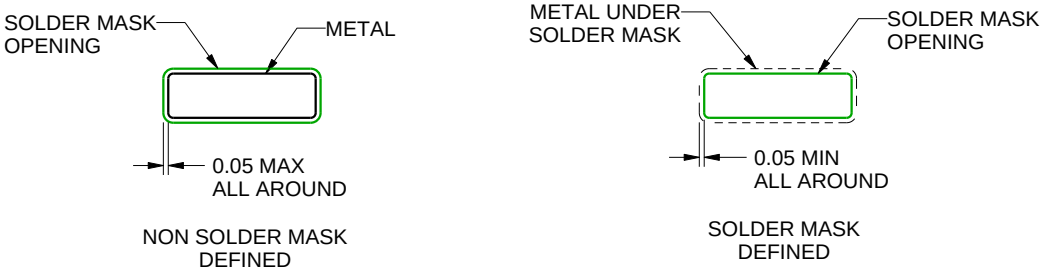
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

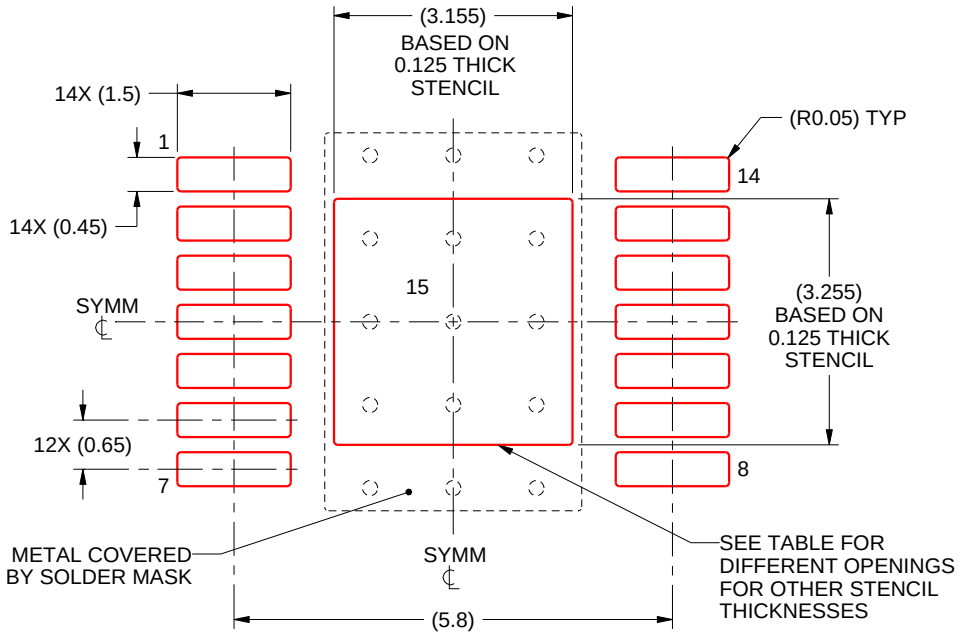


SOLDER MASK DETAILS
PADS 1-14

4214867/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.53 X 3.64
0.125	3.155 X 3.255 (SHOWN)
0.15	2.88 X 2.97
0.175	2.67 X 2.75

4214867/A 09/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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