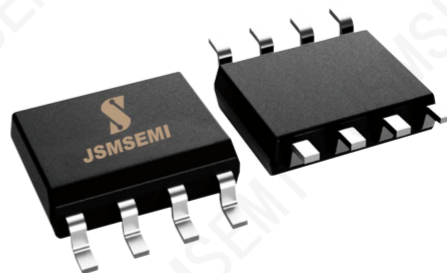


Description

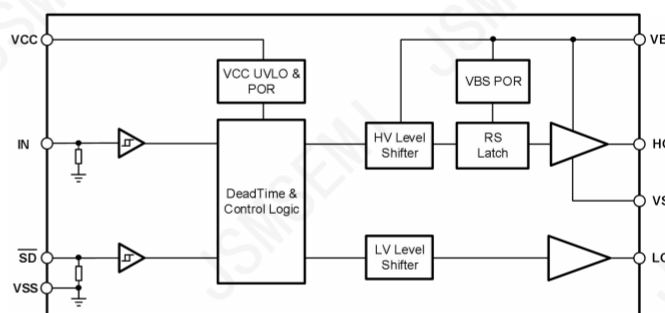
The IR2104STRPBF is a high voltage high speed power MOSFET drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700 V. It can work in the temperature range of -40°C to 125°C.



Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +700 V
- 3.3V, 5V and 15V input logic compatible
- Tolerant to negative transient voltage
- dV/dt immune
- Allowable negative Vs capability: -9V
- Gate drive supply range from 10V to 20V
- Shut down input turns off both channels
- Cross-conduction prevention
- Internal 540ns deadtime
- Matched propagation delay for both channels
- Typically output Source/Sink current capability: 300mA/600mA
- Wide operating temperature range -40°C ~125°C
- RoSH compatible

Functional Block Diagram



Application

- Motor Control
- Air Conditioners/Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

Function Pin Description

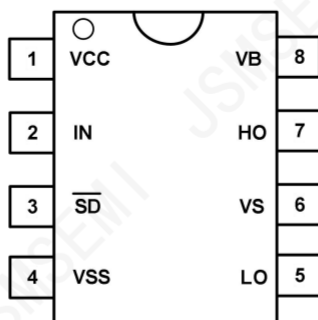


Figure4-18-Pin SOIC8 Top view

Table4-1 Lead Definitions

Number	Symbol	Description
1	V _{CC}	Low side and logic fixed supply
2	IN	Logic input for high side and low side gate driver outputs, in phase with HO
3	SD	Logic input for shutdown
4	V _{SS}	Low side return
5	LO	Low side gate drive output
6	V _S	High side floating supply return
7	HO	High side gate drive output
8	V _B	High side floating supply

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
IR2104STRPBF	SOIC-8	JSM2104S	-55 to 150°C	1	T&R,4000	RoHS

Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V _B	High side floating supply	-0.3	725	V
V _S	High side floating supply return	V _B - 25	V _B + 0.3	
V _{HO}	High side gate drive output	V _S - 0.3	V _B + 0.3	
V _{CC}	Low side and main power supply	-0.3	25	
V _{LO}	Low side gate drive output	-0.3	V _{CC} + 0.3	
V _{IN}	Logic input of IN & SD	-0.3	V _{CC} + 0.3	
dV _S /dt	Allowable Offset Supply Voltage Transient	—	50	V/ns

ESDrating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	1500	—	V
	CDM Model	500	—	V

Ratedpower

Symbol	Definition	MIN.	MAX.	Units
P _D	Package Power Dissipation @ TA ≤25°C	—	625	mW

Thermalinformation

Symbol	Definition	MIN.	MAX.	Units
R _{thJA}	Thermal Resistance, Junction to Ambient	--	200	°C/W
T _J	Junction Temperature	—	150	°C
T _S	Storage Temperature	-55	150	
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	

RecommendedOperatingConditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V _B	High side floating supply	V _S + 10	V _S + 20	V
V _S	High side floating supply return	-9	700	
V _{HO}	High side gate drive output	V _S	V _B	
V _{CC}	Low side and main power supply	10	20	
V _{LO}	Low side gate drive output	0	V _{CC}	
V _{IN}	Logic input of IN & SD	0	V _{CC}	
T _A	Ambient temperature	-40	125	°C

Note1: Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design..

Note2: When the input pulse width is less than 1us, the input pulse cannot be transmitted normally .

Electrical Characteristics

Valid for temperature range at $T_A = 25^\circ\text{C}$, $V_{CC}=V_B = 15\text{V}$, $C_L=1\text{nF}$, unless otherwise specified

Dynamical electrical characteristics

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	130	200	ns	$V_S=0\text{V}$
t_{OFF}	Turn-off propagation delay	—	130	200	ns	$V_S=700\text{V}$
t_R	Turn-on rise time	—	75	130	ns	
t_F	Turn-off fall time	—	35	70	ns	
t_{OFF}	Shutdown propagation delay	—	130	200	ns	
DT	Deadtime	400	520	650	ns	
MT	Delay matching	—	—	50	ns	
MDT	Deadtime matching	—	—	60	ns	

Static electrical characteristics

Valid for temperature range at $T_A = 25^\circ\text{C}$, $V_{CC}=V_B = 15\text{V}$, $C_L=1\text{nF}$, unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{CCUV+}	VCC supply UVLO threshold	8	8.9	9.8	V	
V_{CCUV-}		7.4	8.2	9.0	V	
$V_{CCUVHYS}$	hysteresis of V_{CC} UVLO	—	0.7	—	V	
I_{LK}	High-side floating supply leakage current	—	—	50	μA	$V_B=V_S=700\text{V}$
I_{QBS}	Quiescent V_B supply current	—	50	100	μA	$V_{IN}=0\text{V}$ or 5V
I_{QCC}	Quiescent VCC supply current	—	120	240	μA	$V_{IN}=0\text{V}$ or 5V
V_{IH}	Logic "1" (IN&SD) input voltage	2.5	—	—	V	$V_{CC}=10\text{V}$ to 20V
V_{IL}	Logic "0" (IN&SD) input voltage	—	—	0.8	V	$V_{CC}=10\text{V}$ to 20V
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	0.1	V	$I_O=0\text{A}$
V_{OL}	Low level output voltage, V_O	—	—	0.1	V	$I_O=0\text{A}$
I_{IN+}	Logic "1" Input bias current	—	5	10	μA	$I_N=5\text{V}$, $S_D=5\text{V}$
I_{IN-}	Logic "0" Input bias current	—	—	2	μA	$I_N=0\text{V}$, $S_D=0\text{V}$
$O+$	Output high short circuit pulsed current	200	300	—	mA	$V_O=0\text{V}$ $PW \leq 10\mu\text{s}$
$O-$	Output low short circuit pulsed current	400	600	—	mA	$V_O=15\text{V}$ $PW \leq 10\mu\text{s}$

Function Description

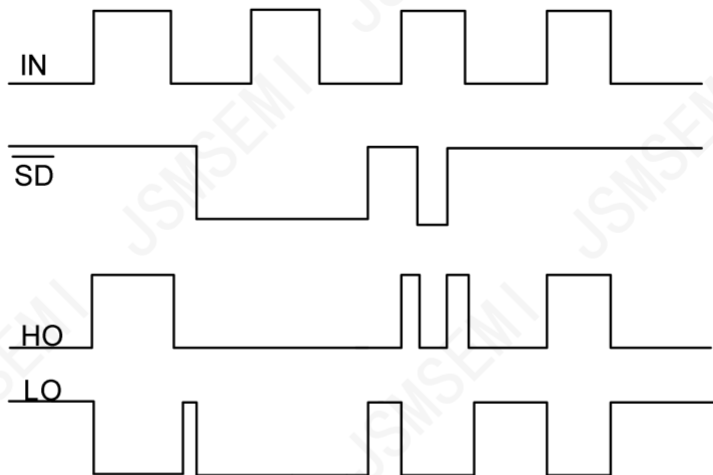


Figure 6-1 IR2104STRPBF Input and output timing waveform

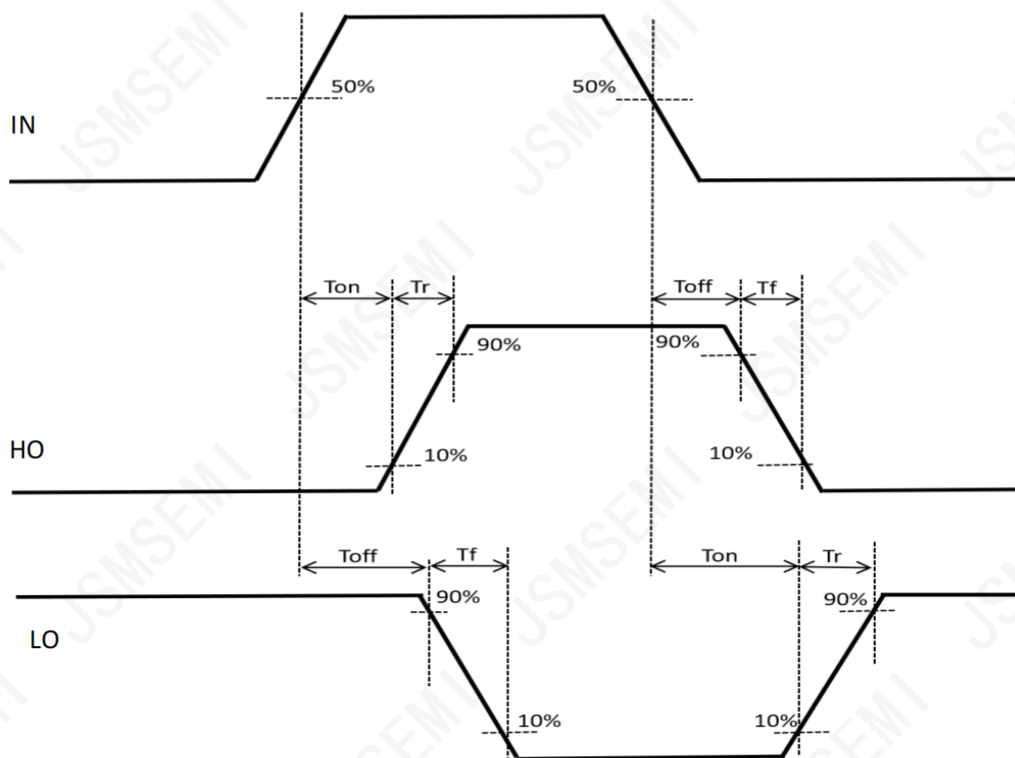


Figure 6-2 Propagation Time Waveform Definition

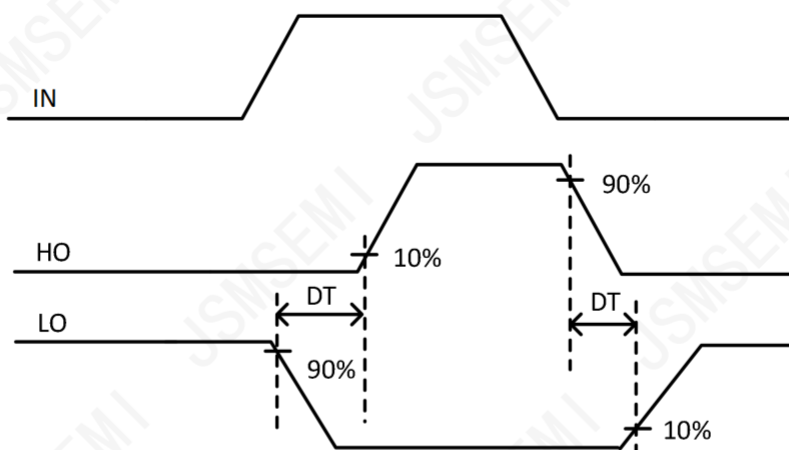


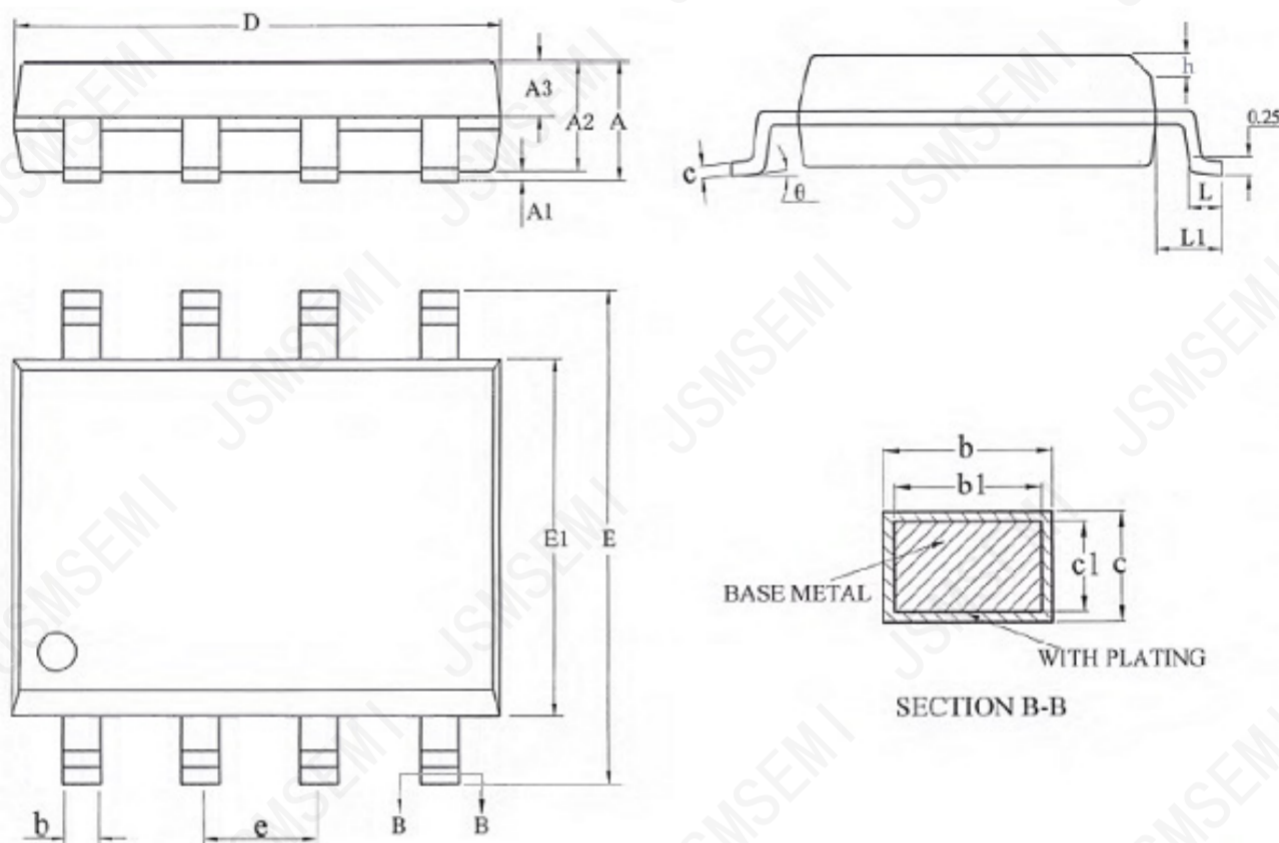
Figure6. Cross Conduction Prevention Delay Time Waveform Definition

The block diagram illustrates the internal architecture of the IR2104STRPBF MOSFET driver. It features a central 'DeadTime & Control Logic' block. The input stage includes an 'IN' pin with a pull-up resistor to VCC and a pull-down resistor to VSS, followed by an inverter. The output stage includes an 'HO' pin with a pull-up resistor to VCC and a pull-down resistor to VSS, followed by an inverter. The 'DeadTime & Control Logic' block is connected to the 'IN' pin and the 'HO' pin. It also receives 'VCC UVLO & POR' and 'VBS POR' signals. The 'DeadTime & Control Logic' block outputs to an 'HV Level Shifter' and an 'LV Level Shifter'. The 'HV Level Shifter' outputs to an 'RS Latch', which is connected to the 'HO' pin. The 'LV Level Shifter' outputs to the 'LO' pin. The 'RS Latch' is also connected to the 'HO' pin. The 'LO' pin is connected to the 'VS' pin. The 'VS' pin is connected to the 'VSS' pin. The 'VCC' pin is connected to the 'VBS' pin. The 'VSS' pin is connected to the 'VS' pin.

7/9

Package Information

SOIC-8 Package Outlines



SOIC-8 Package Dimensions

Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50		
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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