CD4049UB 和 CD4050B CMOS 六路反相缓冲器和转换器

1 特性

- CD4049UB 反相
- CD4050B 同相
- 用于驱动 2 个 TTL 负载的高灌电流
- 高电平至低电平逻辑转换
- 针对 20V 下的静态电流进行了 100% 测试
- 在整个封装温度范围内，18V 时的最大输入电流为 1μA，而在 18V 和 25°C 时为 100nA
- 5V、10V 和 15V 参数额定值

2 应用

- CMOS 至 DTL 或 TTL 十六进制转换器
- CMOS *灌电流* 或 *拉电流* 驱动器
- CMOS 高电平至低电平逻辑转换器

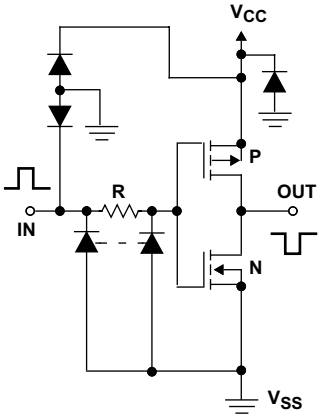
3 说明

CD4049UB 和 CD4050B 器件为反相和同相六路缓冲器，仅使用一个电源电压 (V_{CC}) 即可实现逻辑电平转换。使用这些器件进行逻辑电平转换时，输入信号高电平 (V_{IH}) 可以超过 V_{CC} 电源电压用于逻辑电平转换。这些器件可用作 CMOS 至 DTL 或 TTL 转换器，并可直接驱动两个 DTL 或 TTL 负载。V_{CC} = 5V，V_{OL} ≤ 0.4V 且 I_{OL} ≥ 3.3mA。

封装信息

器件型号	封装(1)	封装尺寸(2)
CD4049UBE、CD4050BE	N (PDIP, 16)	6.35mm × 19.30mm
CD4049UBD、CD4050BD	D（SOIC，16）	9.90mm × 3.91mm
CD4049UBDW、CD4050BDW	DW (SOIC, 16)	10.30mm × 7.50mm
CD4049UBNS、CD4050BNS	SO (16)	10.30mm × 5.30mm
CD4049UBPW、CD4050BPW	PW（TSSOP，16）	5.00mm × 4.40mm

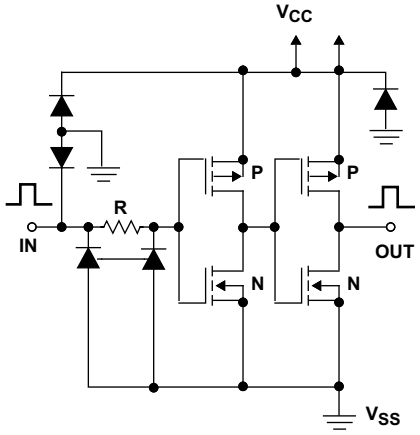
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



Copyright © 2016,
Texas Instruments Incorporated

6 个相同单位中的 1 个

CD4049UB 的原理图



Copyright © 2016, Texas Instruments Incorporated

6 个相同单位中的 1 个

CD4050B 的原理图

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

内容

1 特性.....1
2 应用.....1
3 说明.....1
4 引脚配置和功能.....3
5 规格.....5
5.1 绝对最大额定值.....5
5.2 ESD 等级.....5
5.3 建议运行条件.....6
5.4 热性能信息.....8
5.5 电气特性：DC.....8
5.6 电气特性：AC.....11
5.7 典型特性.....12
6 参数测量信息.....14
6.1 测试电路.....14
7 详细说明.....15
7.1 概述.....15
7.2 功能方框图.....15
7.3 特性说明.....15
7.4 器件功能模式.....16
8 应用和实施.....17
8.1 应用信息.....17
8.2 典型应用.....17
8.3 电源相关建议.....18
8.4 布局.....18
9 器件和文档支持.....19
9.1 文档支持.....19
9.2 接收文档更新通知.....19
9.3 支持资源.....19
9.4 商标.....19
9.5 静电放电警告.....19
9.6 术语表.....19
10 修订历史记录.....19
11 机械、封装和可订购信息.....19

Copyright © 2026 Texas Instruments Incorporated

4 引脚配置和功能

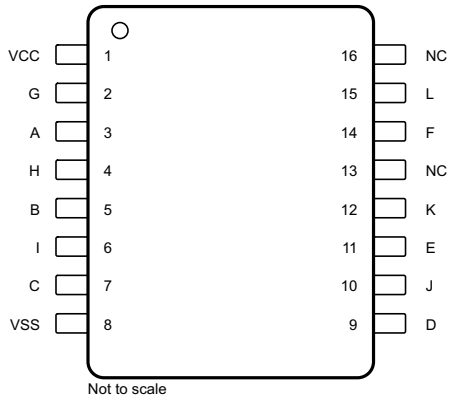


图 4-1. CD4049UB D、DW、N、NS 和 PW 封装 16 引脚 SOIC、PDIP、SO 和 TSSOP 顶视图

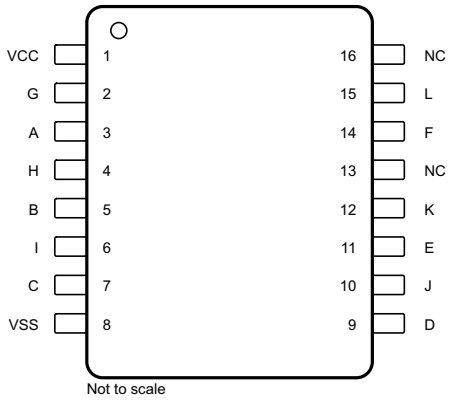


图 4-2. CD4050B D、DW、N、NS 和 PW 封装 1G6 引脚 SOIC、PDIP、SO 和 TSSOP 顶视图

引脚功能：CD4049UB

引脚		类型(1)	说明
名称	编号		
A	3	I	输入 (1)
B	5	I	输入 (2)
C	7	I	输入 (3)
D	9	I	输入 (4)
E	11	I	输入 (5)
F	14	I	输入 (6)
G	2	O	反相输出 1。G = $\overline{A}$
H	4	O	反相输出 2。H = $\overline{B}$
I	6	O	反相输出 3。I = $\overline{C}$
J	10	O	反相输出 4。J = $\overline{D}$
K	12	O	反相输出 5。K = $\overline{E}$
L	15	O	反相输出 6。L = $\overline{F}$
NC	13、16	—	无连接
VCC	1	—	电源引脚
VSS	8	—	负电源

(1) I = 输入，O = 输出

Copyright © 2026 Texas Instruments Incorporated

引脚功能：CD4050B

引脚		类型(1)	说明
名称	编号		
A	3	I	输入 (1)
B	5	I	输入 (2)
C	7	I	输入 (3)
D	9	I	输入 (4)
E	11	I	输入 (5)
F	14	I	输入 (6)
G	2	O	反相输出 1。G = A
H	4	O	反相输出 2。H = B
I	6	O	反相输出 3。I = C
J	10	O	反相输出 4。J = D
K	12	O	反相输出 5。K = E
L	15	O	反相输出 6。L = F
NC	13、16	—	无连接
VCC	1	—	电源引脚
VSS	8	—	负电源

(1) I = 输入，O = 输出

Copyright © 2026 Texas Instruments Incorporated

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

		最小值	最大值	单位
电源电压	VCC 至 VSS	-0.5	20	V
直流输入电流，I_{IK}	任意一个输入		±10	mA
引线温度（焊接，10s）	SOIC，仅引线尖端		265	°C
结温	T_J		150	°C
贮存温度	T_{stg}	-65	150	°C

(1) 超出*绝对最大额定值*范围操作可能会导致器件永久损坏。*绝对最大额定值* 并不表示器件在这些条件下或在*建议的工作条件* 以外的任何其他条件下能够正常运行。如果超出 *建议运行条件* 但在*绝对最大额定值* 范围内使用，器件可能不会完全正常运行，这可能影响器件的可靠性、功能和性能并缩短器件寿命。

5.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	±1500	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22C101(2)	±1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

Copyright © 2026 Texas Instruments Incorporated

5.3 建议运行条件

参数			最小值	典型值	最大值	单位
V_{CC}			3		18	V
T_A			-55		125	°C
I_{OL}（最小值） 输出低电平（灌）电流	V_{OUT} = 0.4V、V_{IN} = 0 或 5V、V_{CC} = 4.5V	T_A = -55°C	3.3			mA
		T_A = -40°C	3.1			
		T_A = 25°C	2.6	5.2		
		T_A = 85°C	2.1			
		T_A = 125°C	1.8			
	V_{OUT} = 0.4V、V_{IN} = 0 或 5V、V_{CC} = 5V	T_A = -55°C	4			
		T_A = -40°C	3.8			
		T_A = 25°C	3.2	6.4		
		T_A = 85°C	2.9			
		T_A = 125°C	2.4			
	V_{OUT} = 0.5V、V_{IN} = 0 或 10V、V_{CC} = 10V	T_A = -55°C	10			
		T_A = -40°C	9.6			
		T_A = 25°C	8	16		
		T_A = 85°C	6.6			
		T_A = 125°C	5.6			
	V_{OUT} = 1.5V、V_{IN} = 0 或 15V、V_{CC} = 15V	T_A = -55°C	26			
		T_A = -40°C	25			
		T_A = 25°C	24	48		
		T_A = 85°C	20			
		T_A = 125°C	18			
I_{OH}（最小值） 输出高电平（拉）电流	V_{OUT} = 4.6V、V_{IN} = 0 或 5V、V_{CC} = 5V	T_A = -55°C	-0.81			mA
		T_A = -40°C	-0.73			
		T_A = 25°C	-0.65	-1.2		
		T_A = 85°C	-0.58			
		T_A = 125°C	-0.48			
	V_{OUT} = 2.5V、V_{IN} = 0 或 5V、V_{CC} = 5V	T_A = -55°C	-2.6			
		T_A = -40°C	-2.4			
		T_A = 25°C	-2.1	-3.9		
		T_A = 85°C	-1.9			
		T_A = 125°C	-1.55			
	V_{OUT} = 9.5V、V_{IN} = 0 或 10V、V_{CC} = 10V	T_A = -55°C	-2			
		T_A = -40°C	-1.8			
		T_A = 25°C	-1.65	-3		
		T_A = 85°C	-1.35			
		T_A = 125°C	-1.18			
	V_{OUT} = 1.3V、V_{IN} = 0 或 15V、V_{CC} = 15V	T_A = -55°C	-5.2			
		T_A = -40°C	-4.8			
		T_A = 25°C	-4.3	-8		
		T_A = 85°C	-3.5			
		T_A = 125°C	-3.1			

Copyright © 2026 Texas Instruments Incorporated

参数				最小值 典型值 最大值	单位
V_{IL}（最大值）	输入低电压 (CD4049UB)	V_{OUT} = 4.5V，V_{CC} = 5V，整个温度范围		1	V
		V_{OUT} = 9V，V_{CC} = 10V，整个温度范围		2	
		V_{OUT} = 13.5V，V_{CC} = 15V，整个温度范围		2.5	
	输入低电压 (CD4050B)	V_{OUT} = 0.5V，V_{CC} = 5V，整个温度范围		1.5	
		V_{OUT} = 1V，V_{CC} = 10V，整个温度范围		3	
		V_{OUT} = 1.5V，V_{CC} = 15V，整个温度范围		4	
V_{IH}（最小值）	输入高电压 (CD4049UB)	V_{OUT} = 0.5V，V_{CC} = 5V	T_A = -55°C	4	V
			T_A = -40°C	4	
			T_A = 25°C	4	
			T_A = 85°C	4	
			T_A = 125°C	4	
		V_{OUT} = 1V，V_{CC} = 10V	T_A = -55°C	8	
			T_A = -40°C	8	
			T_A = 25°C	8	
			T_A = 85°C	8	
			T_A = 125°C	8	
		V_{OUT} = 1.5V，V_{CC} = 15V	T_A = -55°C	12.5	
			T_A = -40°C	12.5	
			T_A = 25°C	12.5	
			T_A = 85°C	12.5	
			T_A = 125°C	12.5	
V_{IH}	输入高电压 (CD4050B)	V_{OUT} = 4.5V，V_{CC} = 5V	T_A = -55°C	3.5	V
			T_A = -40°C	3.5	
			T_A = 25°C	3.5	
			T_A = 85°C	3.5	
			T_A = 125°C	3.5	
		V_{OUT} = 9V，V_{CC} = 10V	T_A = -55°C	7	
			T_A = -40°C	7	
			T_A = 25°C	7	
			T_A = 85°C	7	
			T_A = 125°C	7	
		V_{OUT} = 13.5V，V_{CC} = 15V	T_A = -55°C	11	
			T_A = -40°C	11	
			T_A = 25°C	11	
			T_A = 85°C	11	
			T_A = 125°C	11	

Copyright © 2026 Texas Instruments Incorporated

5.4 热性能信息

热指标(1)		CD4049UB					CD4050B					单位
		D (SOIC)	DW (SOIC)	E (PDIP)	NS (SO)	PW (TSSOP)	D (SOIC)	DW (SOIC)	E (PDIP)	NS (SO)	PW (TSSOP)	
		16 引脚	16 引脚	16 引脚	16 引脚	16 引脚	16 引脚	16 引脚	16 引脚	16 引脚	16 引脚	
$R_{\theta JA}$	结至环境热阻(2)	81.6	81.6	49.5	84.3	108.9	81.6	81.2	49.7	83.8	108.4	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	41.5	44.5	36.8	43	43.7	41.5	44.1	37	42.5	43.2	°C/W
$R_{\theta JB}$	结至电路板热阻	39	46.3	29.4	44.6	54	39	45.9	29.6	44.1	53.5	°C/W
ψ_{JT}	结至顶部特征参数	10.7	16.5	21.7	12.8	4.6	10.7	16.1	21.9	12.5	4.5	°C/W
ψ_{JB}	结至电路板特征参数	38.7	45.8	29.3	44.3	53.4	38.7	45.4	29.5	43.8	52.9	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用手册。
(2) 封装热阻抗根据 JESD 51-7 计算。

5.5 电气特性：DC

参数	测试条件		最小值	典型值	最大值	单位
I_{DD}（最大值） 静态器件电流	V_{IN} = 0 或 5V，V_{CC} = 5V	T_A = -55°C			1	μA
		T_A = -40°C			1	
		T_A = 25°C		0.02	1	
		T_A = 85°C			30	
		T_A = 125°C			30	
	V_{IN} = 0 或 10V，V_{CC} = 10V	T_A = -55°C			2	
		T_A = -40°C			2	
		T_A = 25°C		0.02	2	
		T_A = 85°C			60	
		T_A = 125°C			60	
	V_{IN} = 0 或 15V，V_{CC} = 4V	T_A = -55°C			4	
		T_A = -40°C			4	
		T_A = 25°C		0.02	4	
		T_A = 85°C			120	
		T_A = 125°C			120	
	V_{IN} = 0 或 20V，V_{CC} = 20V	T_A = -55°C			20	
		T_A = -40°C			20	
		T_A = 25°C		0.04	20	
		T_A = 85°C			600	
		T_A = 125°C			600	

Copyright © 2026 Texas Instruments Incorporated

参数	测试条件		最小值	典型值	最大值	单位
I_{OL}（最小值） 输出低电平（灌）电流	V_{OUT} = 0.4V、V_{IN} = 0 或 5V、V_{CC} = 4.5V	T_A = -55°C	3.3			mA
		T_A = -40°C	3.1			
		T_A = 25°C	2.6	5.2		
		T_A = 85°C	2.1			
		T_A = 125°C	1.8			
	V_{OUT} = 0.4V、V_{IN} = 0 或 5V、V_{CC} = 5V	T_A = -55°C	4			
		T_A = -40°C	3.8			
		T_A = 25°C	3.2	6.4		
		T_A = 85°C	2.9			
		T_A = 125°C	2.4			
	V_{OUT} = 0.5V、V_{IN} = 0 或 10V、V_{CC} = 10V	T_A = -55°C	10			
		T_A = -40°C	9.6			
		T_A = 25°C	8	16		
		T_A = 85°C	6.6			
		T_A = 125°C	5.6			
	V_{OUT} = 1.5V、V_{IN} = 0 或 15V、V_{CC} = 15V	T_A = -55°C	26			
		T_A = -40°C	25			
		T_A = 25°C	24	48		
		T_A = 85°C	20			
		T_A = 125°C	18			
V_{OL}（最大值） 输出电压低电平	V_{IN} = 0 或 5V，V_{CC} = 5V	T_A = -55°C			0.05	V
		T_A = -40°C			0.05	
		T_A = 25°C		0	0.05	
		T_A = 85°C			0.05	
		T_A = 125°C			0.05	
	V_{IN} = 0 或 10V，V_{CC} = 10V	T_A = -55°C			0.05	
		T_A = -40°C			0.05	
		T_A = 25°C		0	0.05	
		T_A = 85°C			0.05	
		T_A = 125°C			0.05	
	V_{IN} = 0 或 15V，V_{CC} = 15V	T_A = -55°C			0.05	
		T_A = -40°C			0.05	
		T_A = 25°C		0	0.05	
		T_A = 85°C			0.05	
		T_A = 125°C			0.05	

Copyright © 2026 Texas Instruments Incorporated

参数		测试条件		最小值	典型值	最大值	单位
V_{OH}（最小值）	输出电压高电平	V_{IN} = 0 或 5V，V_{CC} = 5V	T_A = -55°C	4.95			V
			T_A = -40°C	4.95			
			T_A = 25°C	4.95	5		
			T_A = 85°C	4.95			
			T_A = 125°C	4.95			
		V_{IN} = 0 或 10V，V_{CC} = 10V	T_A = -55°C	9.95			
			T_A = -40°C	9.95			
			T_A = 25°C	9.95	10		
			T_A = 85°C	9.95			
			T_A = 125°C	9.95			
		V_{IN} = 0 或 15V，V_{CC} = 15V	T_A = -55°C	14.95			
			T_A = -40°C	14.95			
			T_A = 25°C	14.95	15		
			T_A = 85°C	14.95			
			T_A = 125°C	14.95			
I_{IN}（最大值）	输入电流	V_{IN} = 0 或 18V，V_{CC} = 18V	T_A = -55°C			±0.1	μA
			T_A = -40°C			±0.1	
			T_A = 25°C		$\pm 10^{-5}$	±0.1	
			T_A = 85°C			±1	
			T_A = 125°C			±1	

Copyright © 2026 Texas Instruments Incorporated

5.6 电气特性：AC

T_A = 25°C、输入 t_r 和 t_f = 20ns、C_L = 50pF、R_L = 200kΩ（除非另有说明）

参数		测试条件	最小值	典型值	最大值	单位
t_{PLH}	传播延迟时间 低至高电平 (CD4049UB)	V_{IN} = 5V，V_{CC} = 5V		60	120	ns
		V_{IN} = 10V，V_{CC} = 10V		32	65	
		V_{IN} = 10V，V_{CC} = 5V		45	90	
		V_{IN} = 15V，V_{CC} = 15V		25	50	
		V_{IN} = 15V，V_{CC} = 5V		45	90	
	传播延迟时间 低至高电平 (CD4050B)	V_{IN} = 5V，V_{CC} = 5V		70	140	ns
		V_{IN} = 10V，V_{CC} = 10V		40	80	
		V_{IN} = 10V，V_{CC} = 5V		45	90	
		V_{IN} = 15V，V_{CC} = 15V		30	60	
		V_{IN} = 15V，V_{CC} = 5V		40	80	
t_{PHL}	传播延迟时间 高至低电平 (CD4049UB)	V_{IN} = 5V，V_{CC} = 5V		32	65	ns
		V_{IN} = 10V，V_{CC} = 10V		20	40	
		V_{IN} = 10V，V_{CC} = 5V		15	30	
		V_{IN} = 15V，V_{CC} = 15V		15	30	
		V_{IN} = 15V，V_{CC} = 5V		10	20	
	传播延迟时间 高至低电平 (CD4050B)	V_{IN} = 5V，V_{CC} = 5V		55	110	ns
		V_{IN} = 10V，V_{CC} = 10V		22	55	
		V_{IN} = 10V，V_{CC} = 5V		50	100	
		V_{IN} = 15V，V_{CC} = 15V		15	30	
		V_{IN} = 15V，V_{CC} = 5V		50	100	
t_{TLH}	转换时间 低至高电平	V_{IN} = 5V，V_{CC} = 5V		80	160	ns
		V_{IN} = 10V，V_{CC} = 10V		40	80	
		V_{IN} = 15V，V_{CC} = 15V		30	60	
t_{THL}	转换时间 高至低电平	V_{IN} = 5V，V_{CC} = 5V		30	60	ns
		V_{IN} = 10V，V_{CC} = 10V		20	40	
		V_{IN} = 15V，V_{CC} = 15V		15	30	
C_{IN}	输入电容 (CD4049UB)			15	22.5	pF
	输入电容 (CD4050B)			5	7.5	pF

Copyright © 2026 Texas Instruments Incorporated

5.7 典型特性

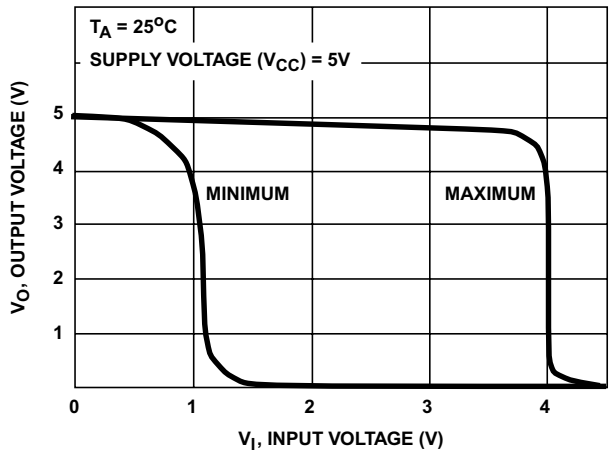


图 5-1. CD4049UB 的最小电压和最大电压传输特性

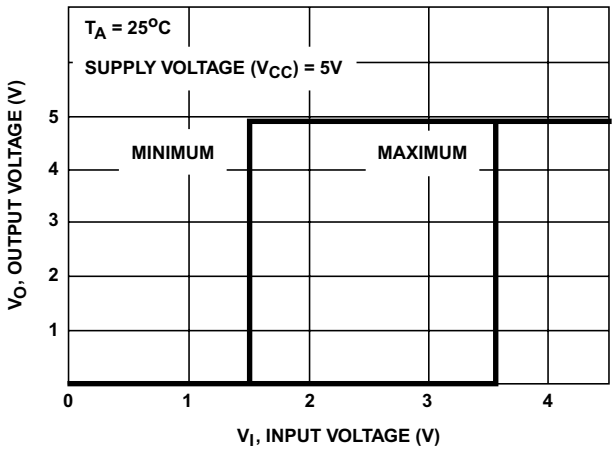


图 5-2. CD4050B 的最小电压和最大电压传输特性

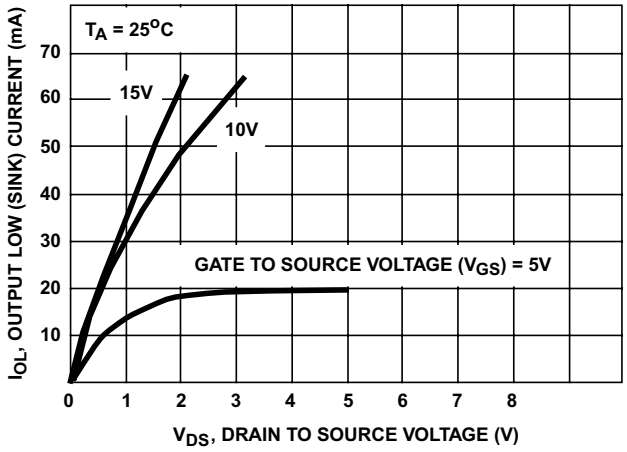


图 5-3. 典型输出低电平（灌）电流特性

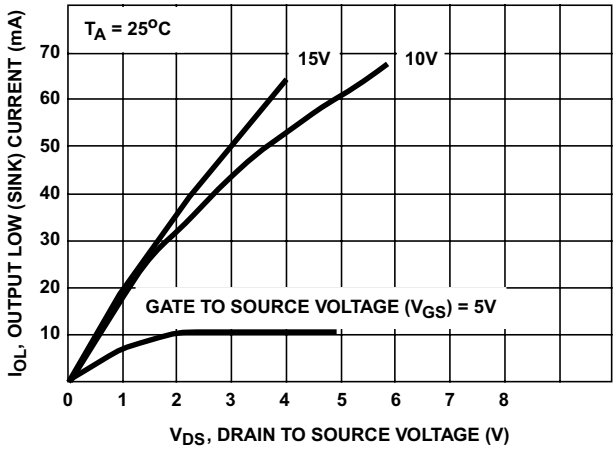


图 5-4. 最小输出低电平（灌）电流漏极特性

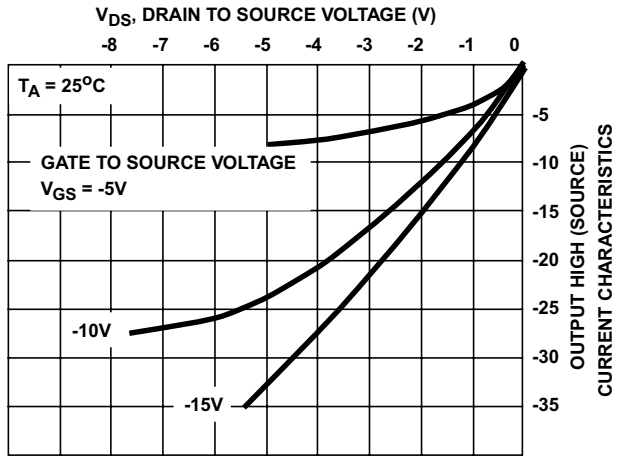


图 5-5. 典型输出高电平（拉）电流特性

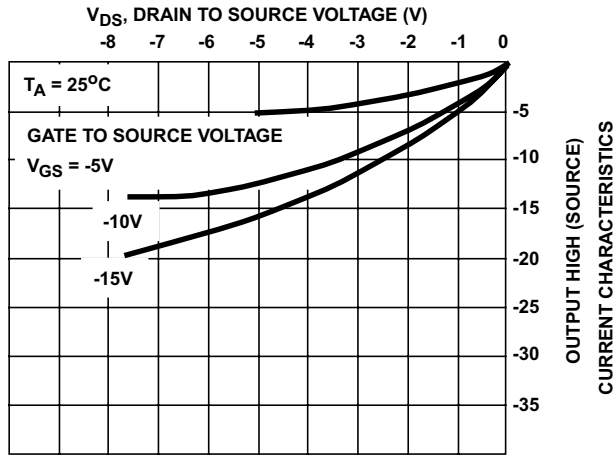


图 5-6. 最小输出高电平（拉）电流特性

Copyright © 2026 Texas Instruments Incorporated

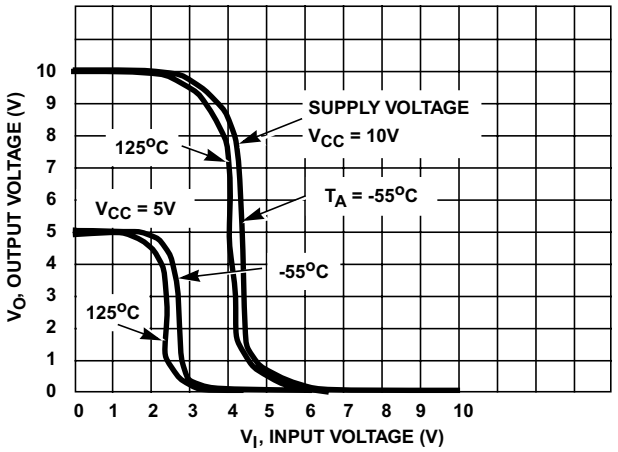


图 5-7. CD4049UB 随温度变化的典型电压传输特性

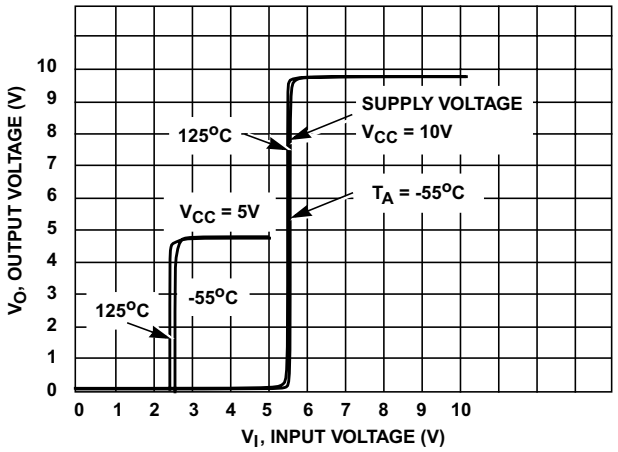


图 5-8. CD4050B 随温度变化的典型电压传输特性

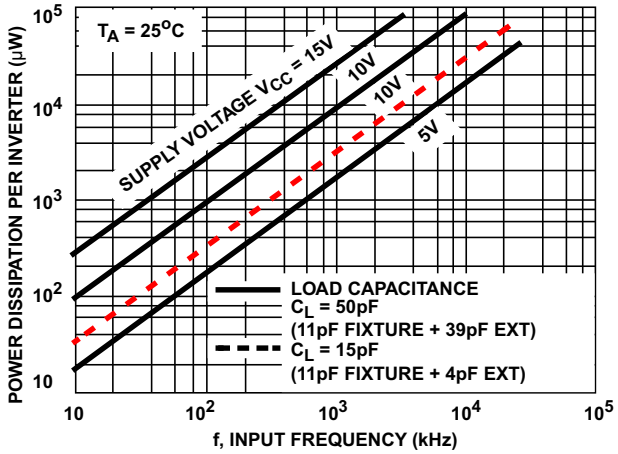


图 5-9. 典型功率耗散与频率特性间的关系

Copyright © 2026 Texas Instruments Incorporated

6 参数测量信息

6.1 测试电路

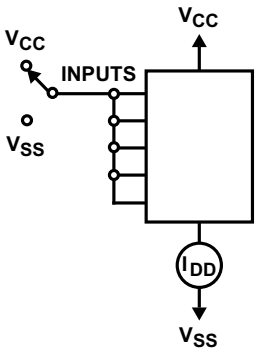
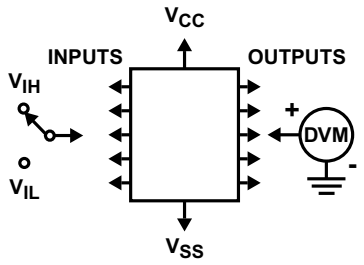
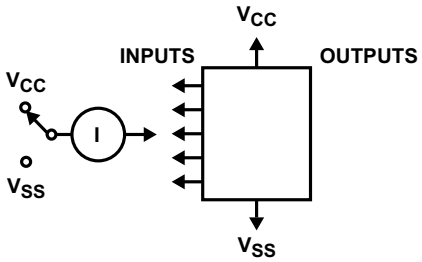


图 6-1. 静态器件电流测试电路



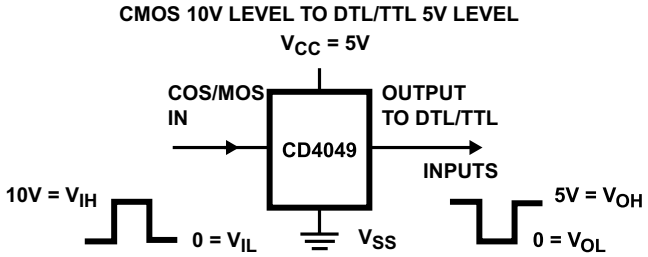
将任意一个输入与其他输入在 VCC 或 VSS 下进行测试。

图 6-2. 输入电压测试电路



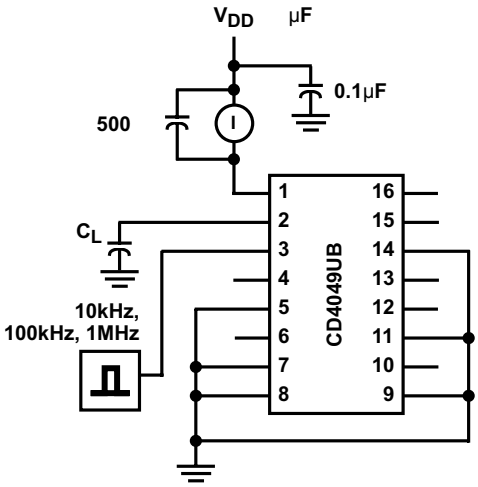
按顺序测量 VCC 和 VSS 的输入，将所有未使用的输入连接至 VCC 或 VSS。

图 6-3. 输入电流测试电路



IN 引脚：A、B、C、D、E 或 F
OUT 引脚：G、H、I、J、K 或 L
VCC 引脚
VSS 引脚

图 6-4. 逻辑电平转换应用



C_L 包括夹具电容。

图 6-5. 动态功率耗散测试电路

Copyright © 2026 Texas Instruments Incorporated

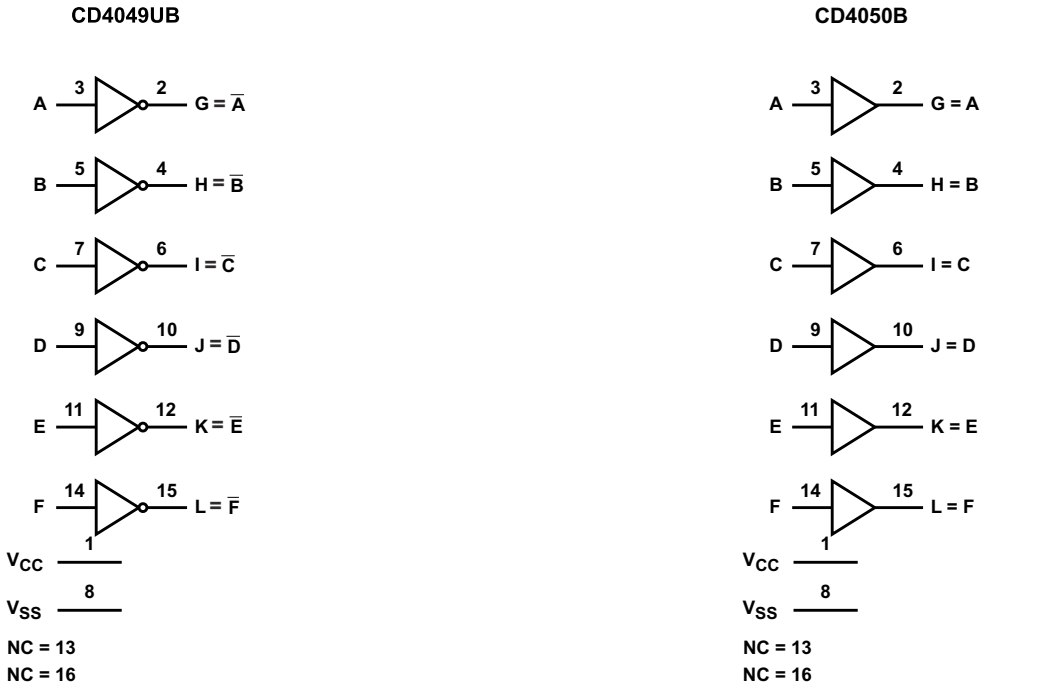
7 详细说明

7.1 概述

CD4049UB 器件是反相六路缓冲器；CD4050B 器件是同相六路缓冲器。这些器件进行逻辑电平转换，并具有可驱动两个 TTL 负载的高灌电流。这些器件在 18V 电压时和整个温度范围内均具有 1 μ A 的低输入电流。

CD4049UB 和 CD4050B 器件分别指定为 CD4009UB 和 CD4010B 器件的替代器件。由于 CD4049UB 和 CD4050B 只需要一个电源，因此它们优于 CD4009UB 和 CD4010B，并且在所有逆变器、电流驱动器或逻辑电平转换应用中，应使用它们来代替 CD4009UB 和 CD4010B。在这些应用中，CD4049UB 和 CD4050B 分别与 CD4009UB 和 CD4010B 引脚兼容，可以在现有设计和新设计中替换这些器件。CD4049UB 或 CD4050B 未在内部连接引脚 16 (NC)，因此与该端子的连接不会影响电路运行。TI 建议在不需要高灌电流或电压转换的应用场景中选用 CD4069UB 六路逆变器。

7.2 功能方框图



Copyright © 2016, Texas Instruments Incorporated

7.3 特性说明

CD4049UB 和 CD4050B 具有标准化的对称输出特性和 3V 至 18V 的宽工作电压范围，并在 20V 电压下进行静态电流测试。这些器件在 10V 时的转换时间为 t_{TLH} = 40ns 且 t_{THL} = 20ns（典型值）。将工作温度从 -55°C 调整为 125°C。

7.4 器件功能模式

表 7-1 显示了 CD4049UB 器件的功能模式。表 7-2 显示了 CD4050B 器件的功能模式。

表 7-1. CD4049UB 的功能表

输入 A、B、C、D、E、F	输出 G、H、I、J、K、L
H	L
L	H

表 7-2. CD4050B 的功能表

输入 A、B、C、D、E、F	输出 G、H、I、J、K、L
H	H
L	L

Copyright © 2026 Texas Instruments Incorporated

8 应用和实施

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户应负责确定各元件是否适用于其应用。客户应验证并测试其设计是否能够实现，以确保系统功能。

8.1 应用信息

CD4049UB 和 CD4050B 器件在整个封装温度范围内具有低输入电流特性，在 18V 时输入电流为 1 μA，在 25°C 和 18V 时输入电流为 100nA。在 3V 至 18V 的宽工作电压范围内，这些器件适用于高压应用场景。

8.2 典型应用

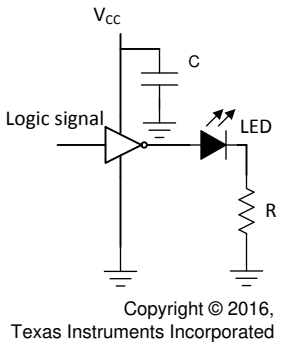


图 8-1. CD4049UB 应用

8.2.1 设计要求

CD4049UB 器件是业界超高的逻辑逆变器，可在建议条件下以 18V 电压运行。这些器件具有高灌电流能力。

8.2.2 详细设计过程

图 8-1 的建议输入条件包括上升时间和下降时间规格（请参阅 Δt/ΔV，具体如*建议运行条件所述*）以及指定的高电平和低电平（请参阅 V_{IH} 和 V_{IL}，具体如*建议运行条件所述*）。由于输入端存在连接至 VCC 的钳位二极管，使这些输入端不具备过压耐受能力且必须低于 V_{CC} 电平。

CD4049UB 应用场景的建议输出条件包括特定的负载电流。必须限制负载电流，以免超过器件的总功率（通过 VCC 或 GND 的持续电流）。这些限值如*绝对最大额定值*所述。输出不应被拉至高于 V_{CC}。

Copyright © 2026 Texas Instruments Incorporated

8.2.3 应用曲线

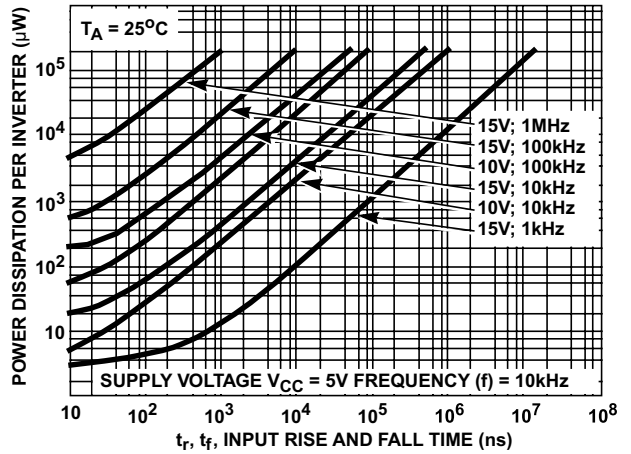


图 8-2. CD4049UB 每个逆变器的典型功率耗散与输入上升和下降时间之间的关系

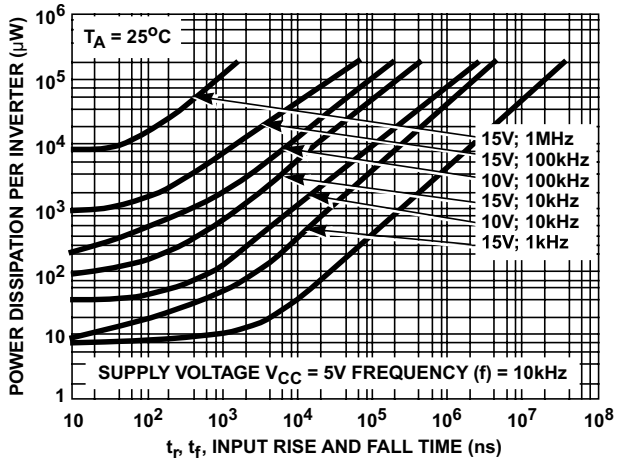


图 8-3. CD4050B 每个缓冲器的典型功率耗散与输入上升和下降时间之间的关系

8.3 电源相关建议

电源可以是*建议运行条件*中最小和最大电源电压额定值之间的任何电压。

每个 VCC 引脚必须具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，TI 建议使用 0.1µF 电容器。如果有多个 VCC 引脚，则 TI 建议每个电源引脚使用 0.01µF 或 0.022µF 电容器。可以并联多个旁路电容器以抑制不同的噪声频率。0.1µF 和 1µF 电容器通常并联使用。为了获得更佳效果，旁路电容器必须尽可能靠近电源引脚安装。

8.4 布局

8.4.1 布局指南

当使用多位逻辑器件时，输入不得悬空。

在许多情况下，未使用数字逻辑器件的全部或部分功能（例如，仅使用三输入与门的两个输入，或仅使用 4 个缓冲门中的 3 个）。此类输入引脚不得悬空，因为外部连接处的未定义电压会导致未定义的运行状态。在下一段所指明的所有情况下，都必须遵守这条规则。

数字逻辑器件的所有未使用输入必须连接至高或低偏置以防悬空。请参阅*慢速或浮点 CMOS 输入的影响*，了解有关浮点输入影响的更多信息。根据器件的功能情况，必须向任何特定未使用的输入施加逻辑电平。通常，它们会连接到 GND 或 VCC（具体取决于哪种更方便）。

8.4.2 布局示例

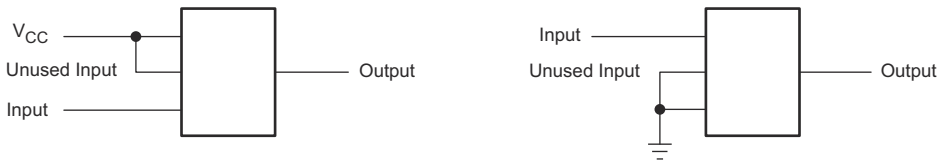


图 8-4. 布局图

Copyright © 2026 Texas Instruments Incorporated

9 器件和文档支持

9.1 文档支持

9.1.1 相关文档

请参阅以下相关文档：

- 德州仪器 (TI)，*CMOS 输入缓慢或悬空的影响* 应用手册

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。点击右上角的*提醒我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision K (June 2020) to Revision L (February 2026)	Page
• 更新了建议运行条件部分中的格式	6
• 更新了直流电气特性中的格式以确定最大值和最小值	8
• 将 V_{IH}、V_{IL}、I_{OH} 和 I_{OL} 移至建议运行条件部分	8

Changes from Revision J (September 2016) to Revision K (June 2020)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 使用正确的封装尺寸更新了*器件信息表*	1

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

Copyright © 2026 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4049UBD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4049UBM
CD4049UBDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM
CD4049UBDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM
CD4049UBDRE4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM
CD4049UBDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM
CD4049UBDT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4049UBM
CD4049UBDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM
CD4049UBDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM
CD4049UBDWG4	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM
CD4049UBE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4049UBE
CD4049UBE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4049UBE
CD4049UBEE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4049UBE
CD4049UBF	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4049UBF
CD4049UBF.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4049UBF
CD4049UBF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4049UBF3A
CD4049UBF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4049UBF3A
CD4049UBNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UB
CD4049UBNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UB
CD4049UBPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM049UB
CD4049UBPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CM049UB
CD4049UBPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM049UB
CD4050BD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4050BM
CD4050BDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050BM
CD4050BDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050BM
CD4050BDT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4050BM
CD4050BDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-55 to 125	CD4050BM
CD4050BDWR	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050BM
CD4050BDWR.A	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050BM
CD4050BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4050BE

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4050BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4050BE
CD4050BEE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4050BE
CD4050BF	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4050BF
CD4050BF.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4050BF
CD4050BF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4050BF3A
CD4050BF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4050BF3A
CD4050BNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050B
CD4050BNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050B
CD4050BPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM050B
CD4050BPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CM050B
CD4050BPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM050B
CD4050BPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM050B
JM38510/05553BEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05553BEA
JM38510/05553BEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05553BEA
JM38510/05554BEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05554BEA
JM38510/05554BEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05554BEA
M38510/05553BEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05553BEA
M38510/05554BEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05554BEA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4049UB, CD4049UB-MIL, CD4050B, CD4050B-MIL :

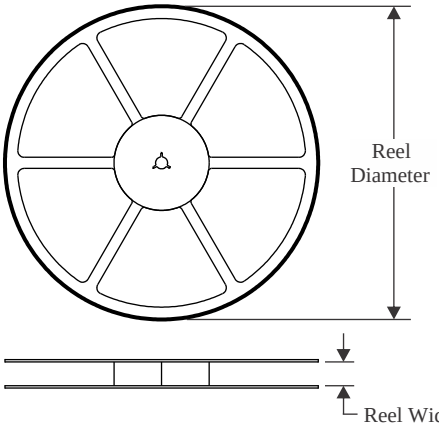
- Catalog : CD4049UB, CD4050B
- Military : CD4049UB-MIL, CD4050B-MIL

NOTE: Qualified Version Definitions:

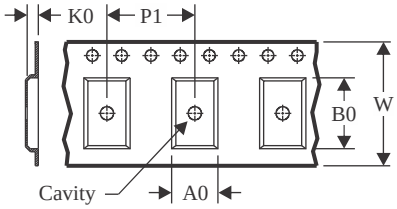
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

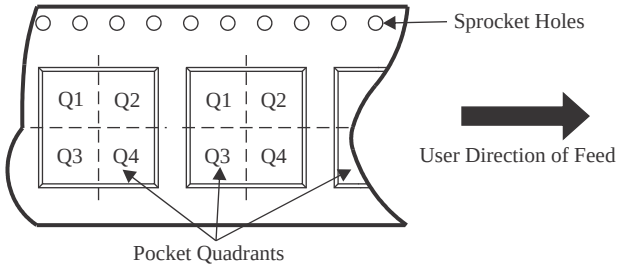


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

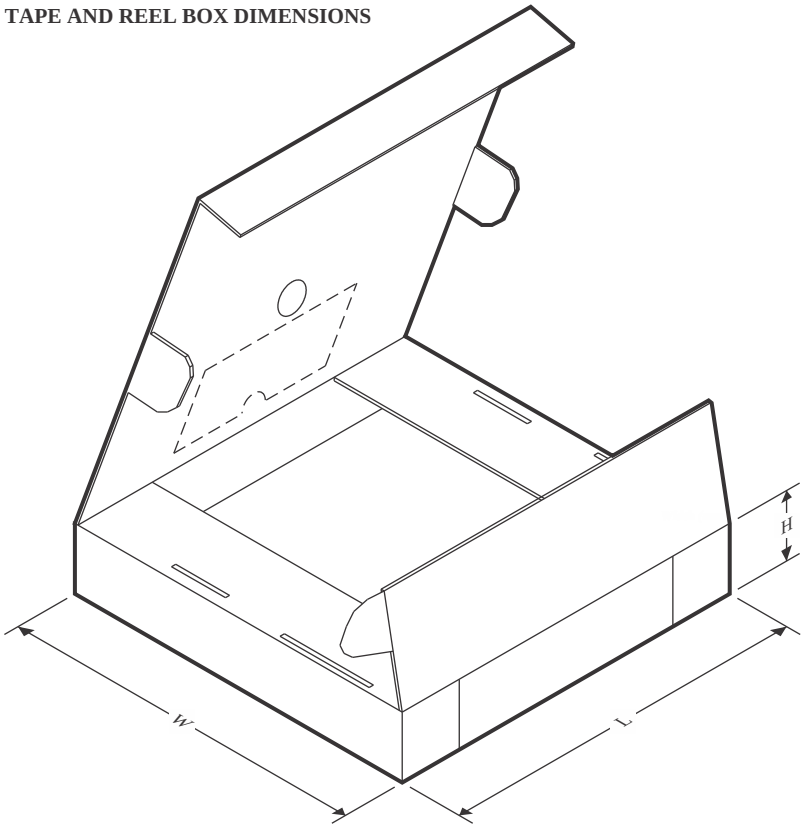
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4049UBDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4049UBNSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD4049UBPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4050BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4050BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
CD4050BNSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD4050BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4050BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4050BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

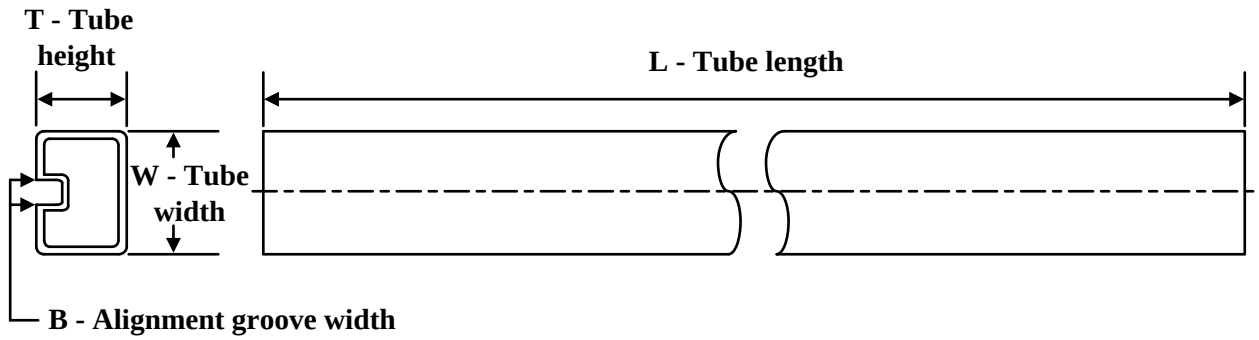
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

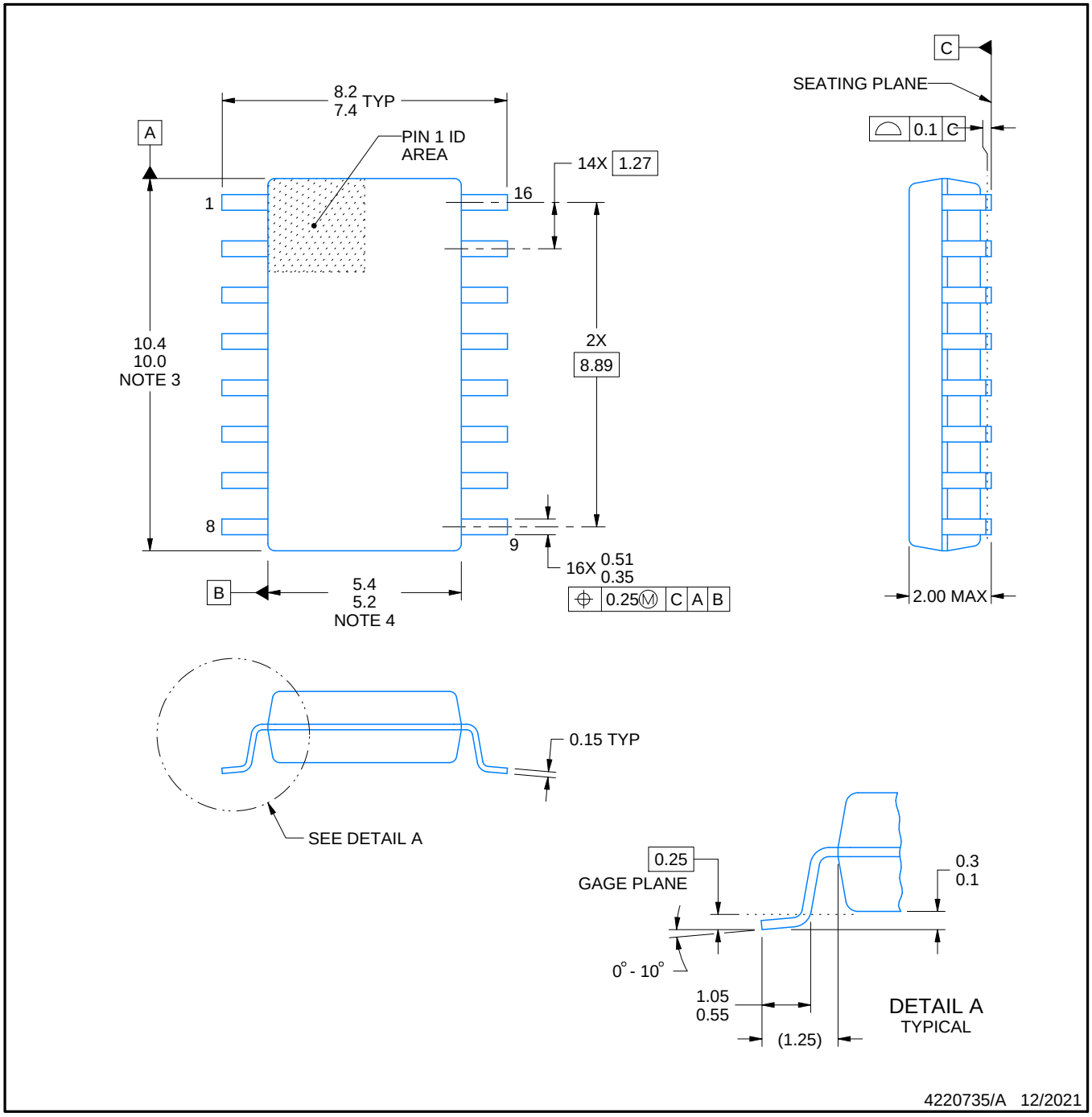
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4049UBDR	SOIC	D	16	2500	353.0	353.0	32.0
CD4049UBNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4049UBPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD4050BDR	SOIC	D	16	2500	353.0	353.0	32.0
CD4050BDWR	SOIC	DW	16	2000	350.0	350.0	43.0
CD4050BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4050BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD4050BPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD4050BPWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE



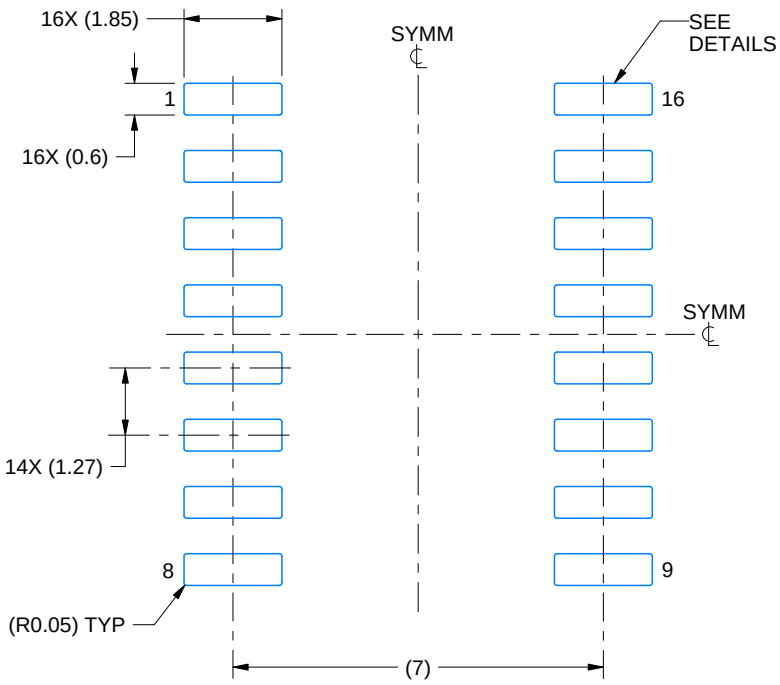
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4049UBDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
CD4049UBDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
CD4049UBDWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
CD4049UBE	N	PDIP	16	25	506	13.97	11230	4.32
CD4049UBE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4049UBEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4050BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4050BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4050BEE4	N	PDIP	16	25	506	13.97	11230	4.32

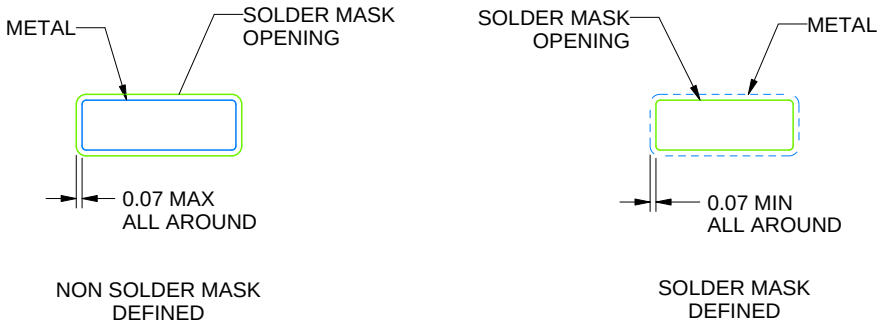


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

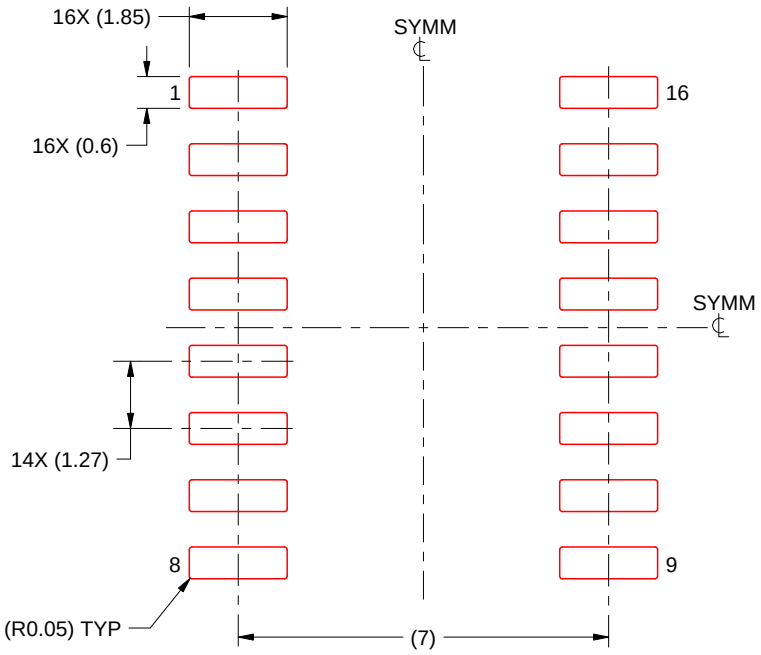


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



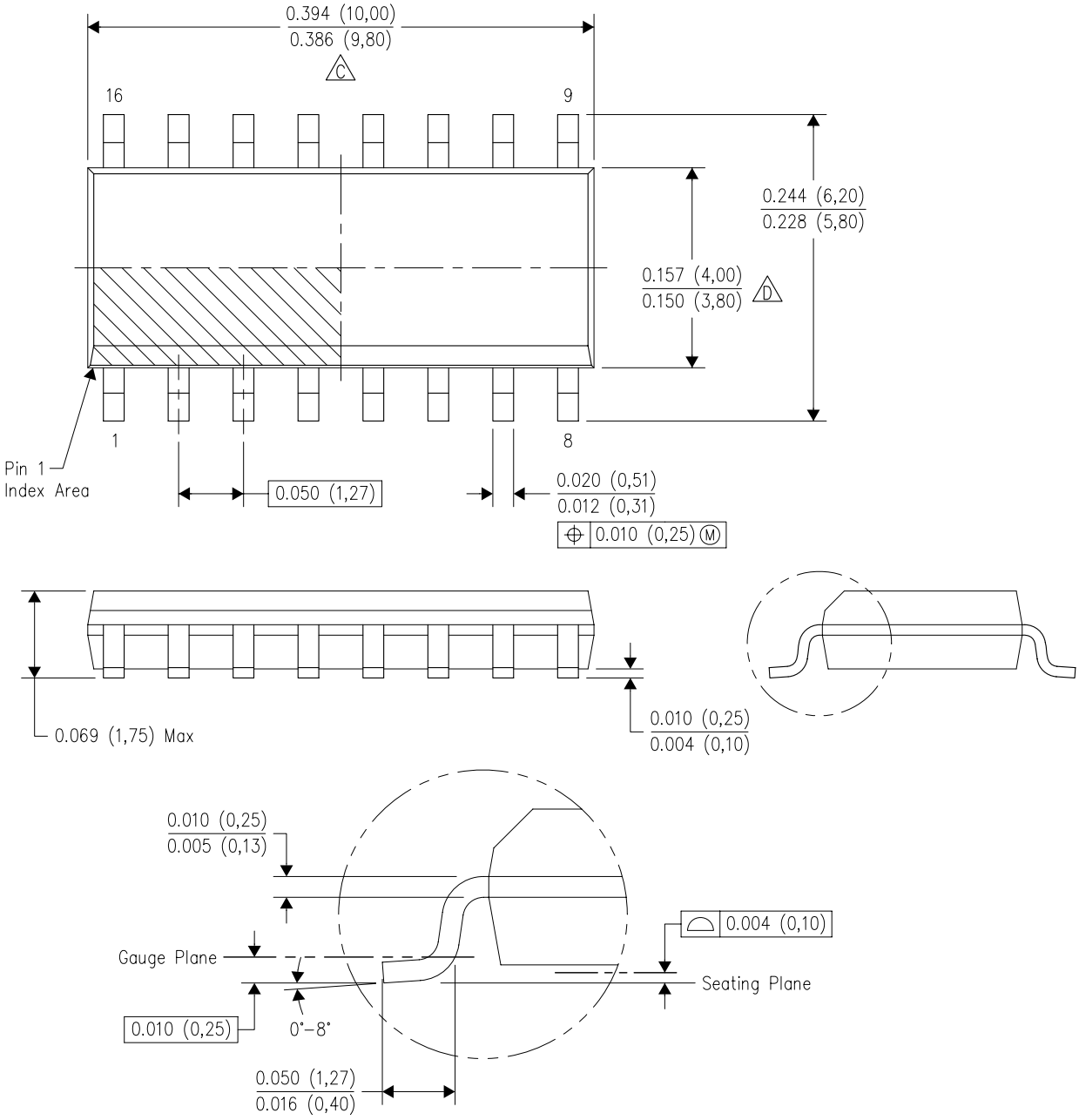
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

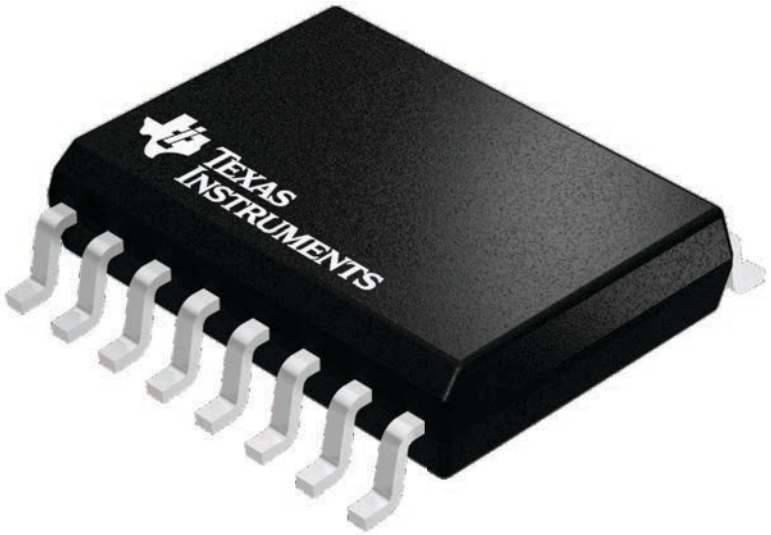
DW 16

SOIC - 2.65 mm max height

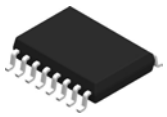
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

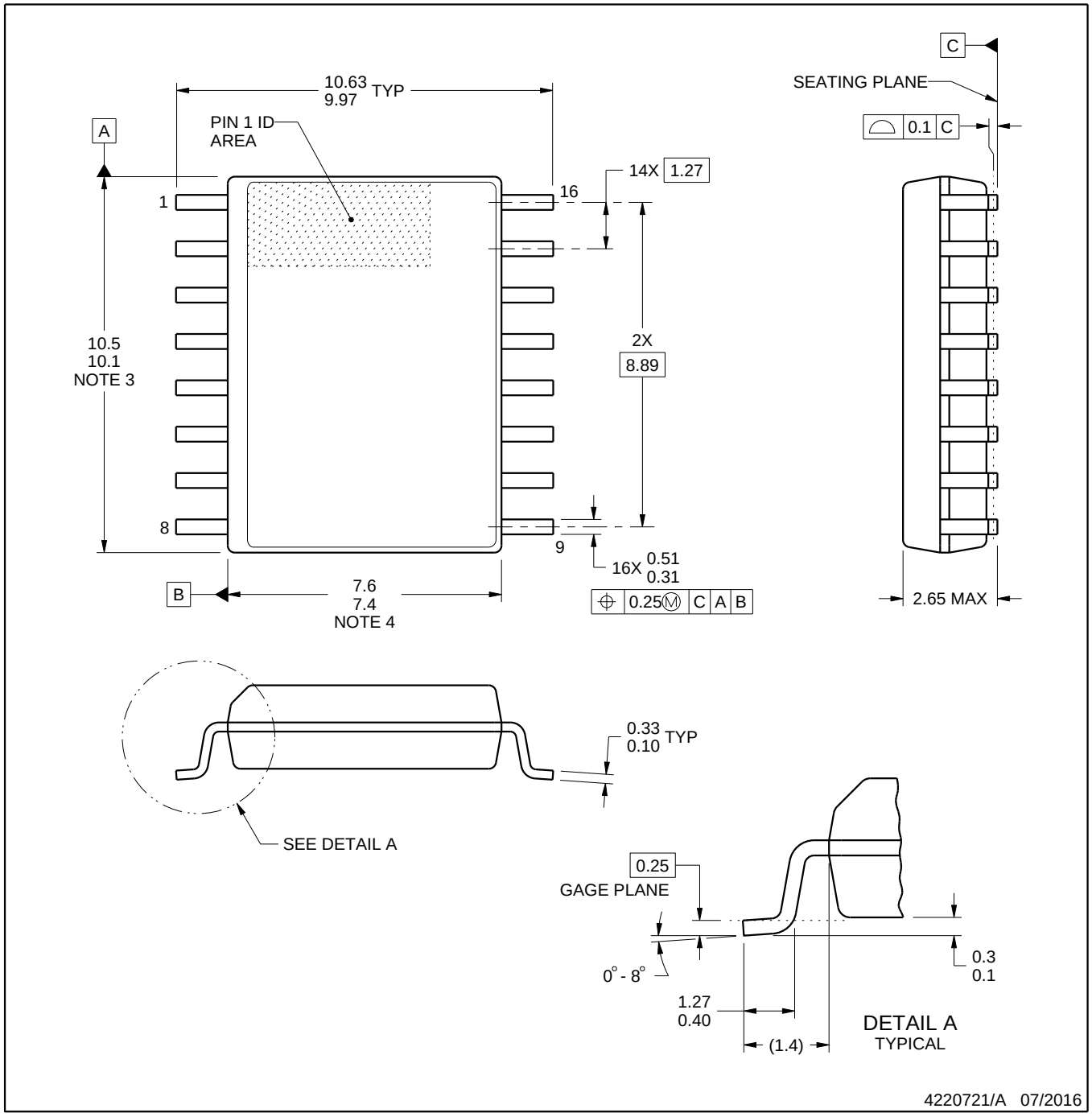


PACKAGE OUTLINE

DW0016A

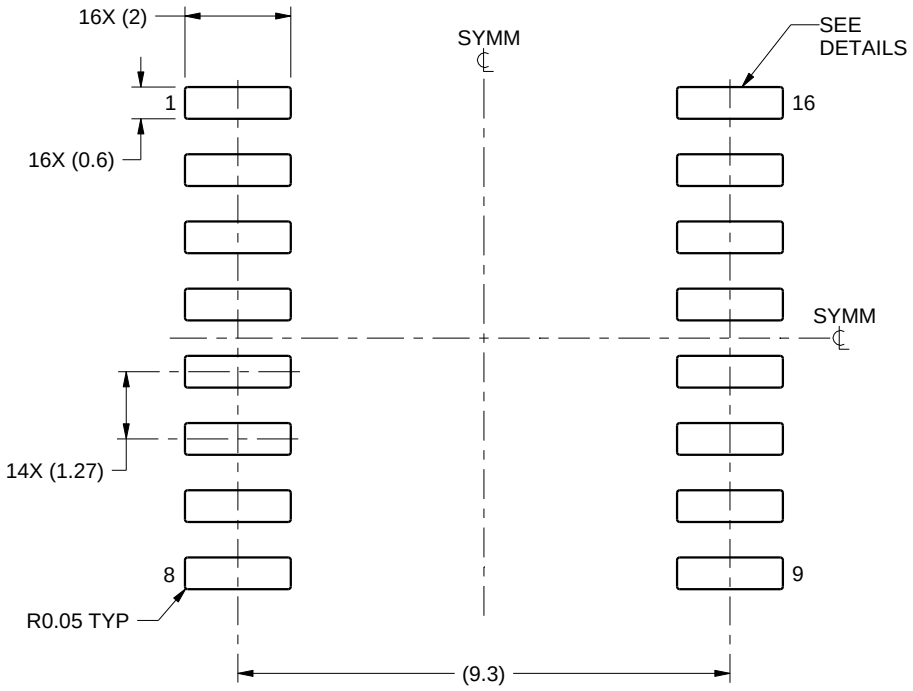
SOIC - 2.65 mm max height

SOIC

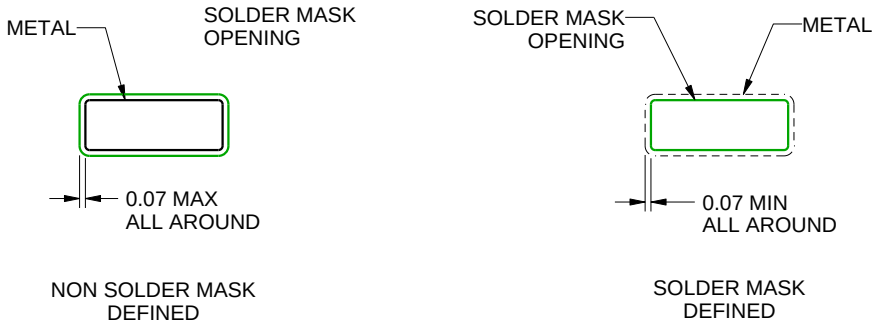


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

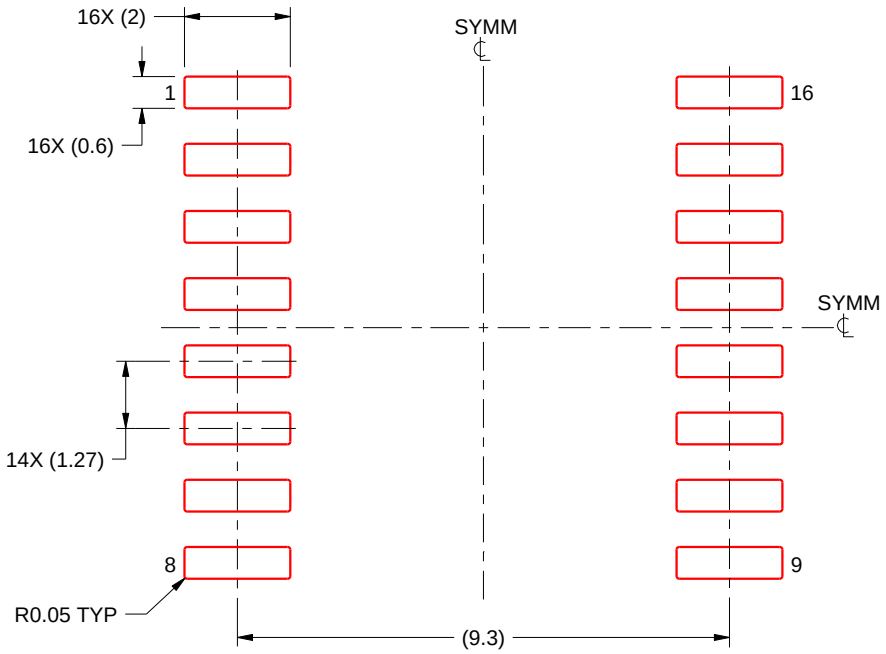


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

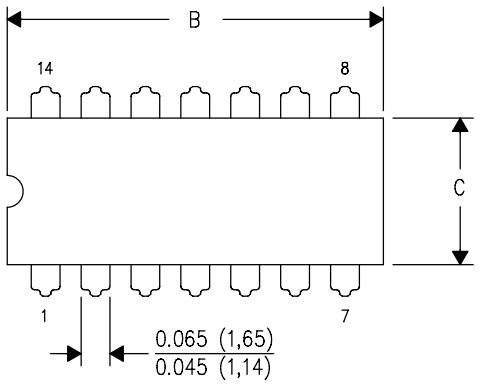
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

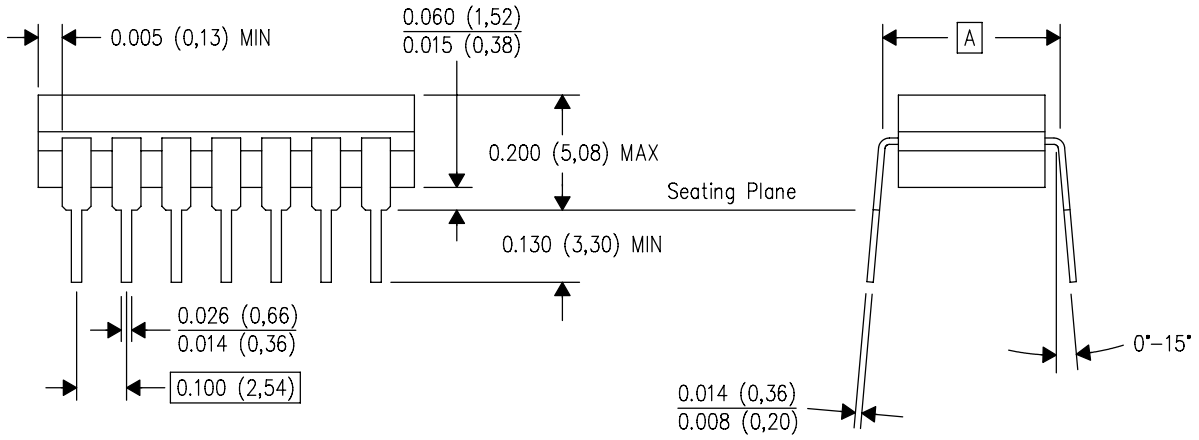
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

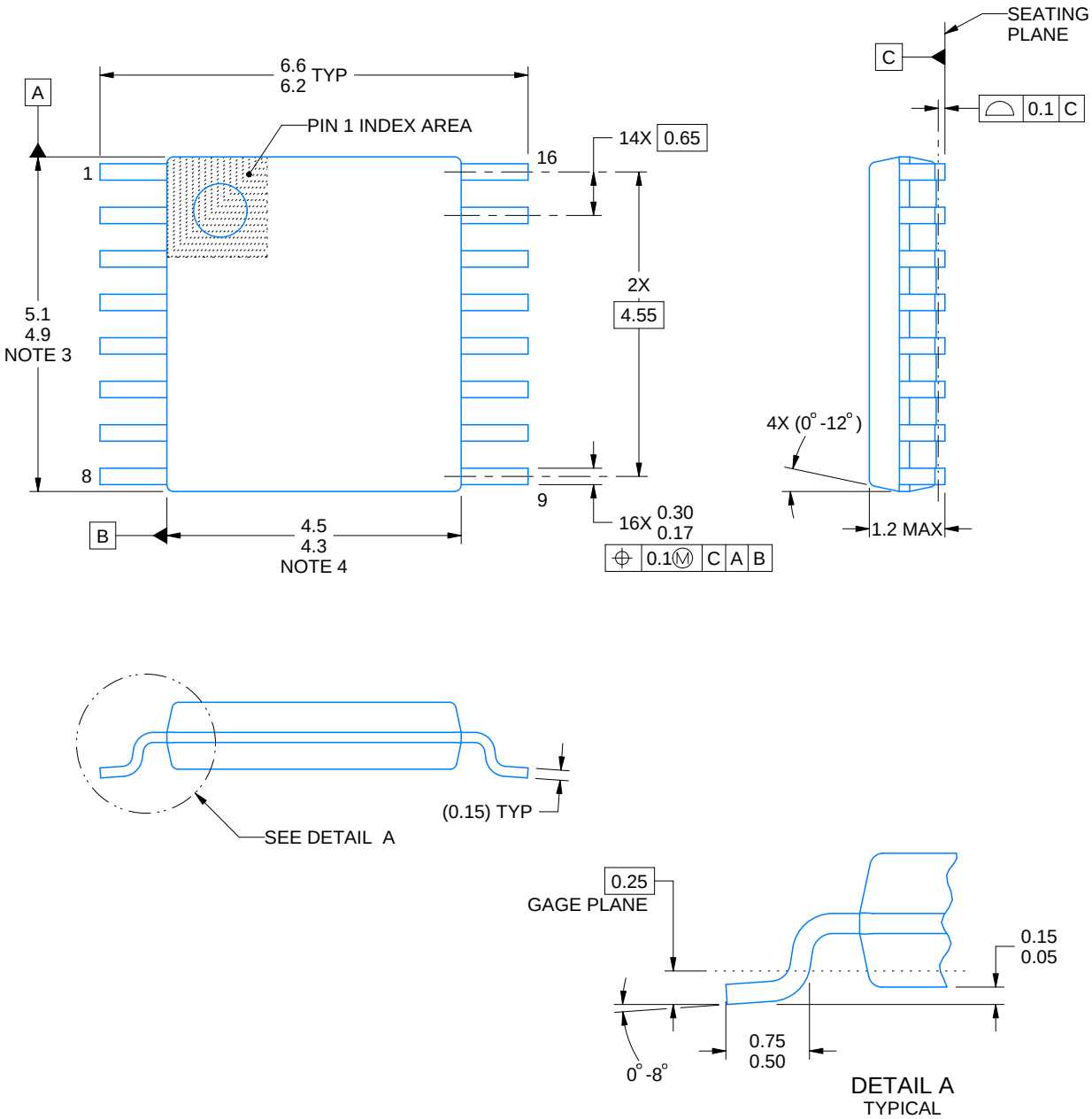
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

PW0016A

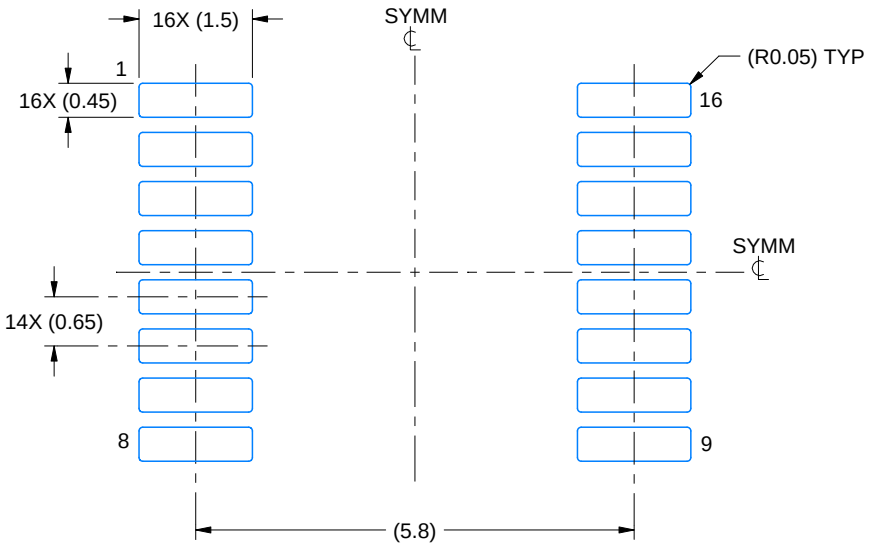
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

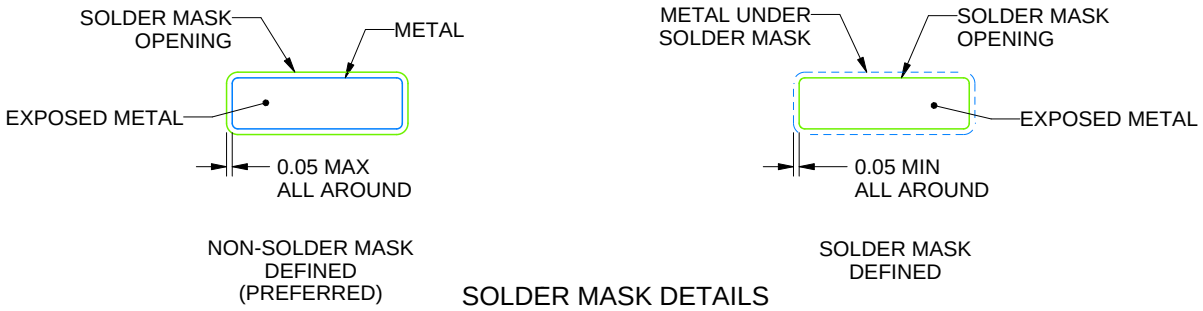


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

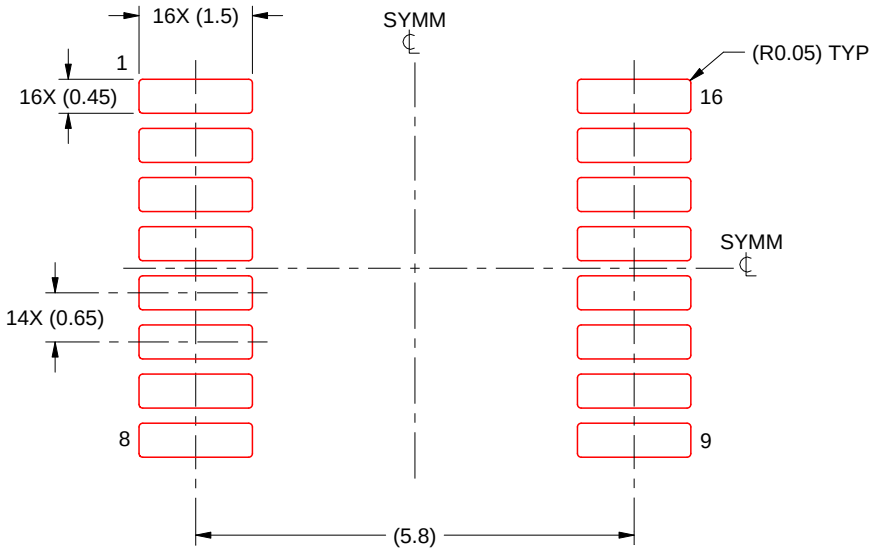


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

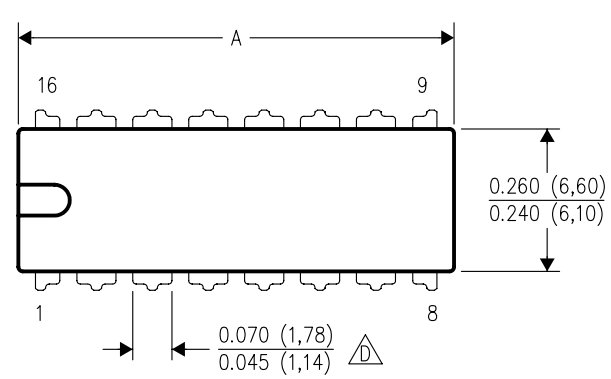
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

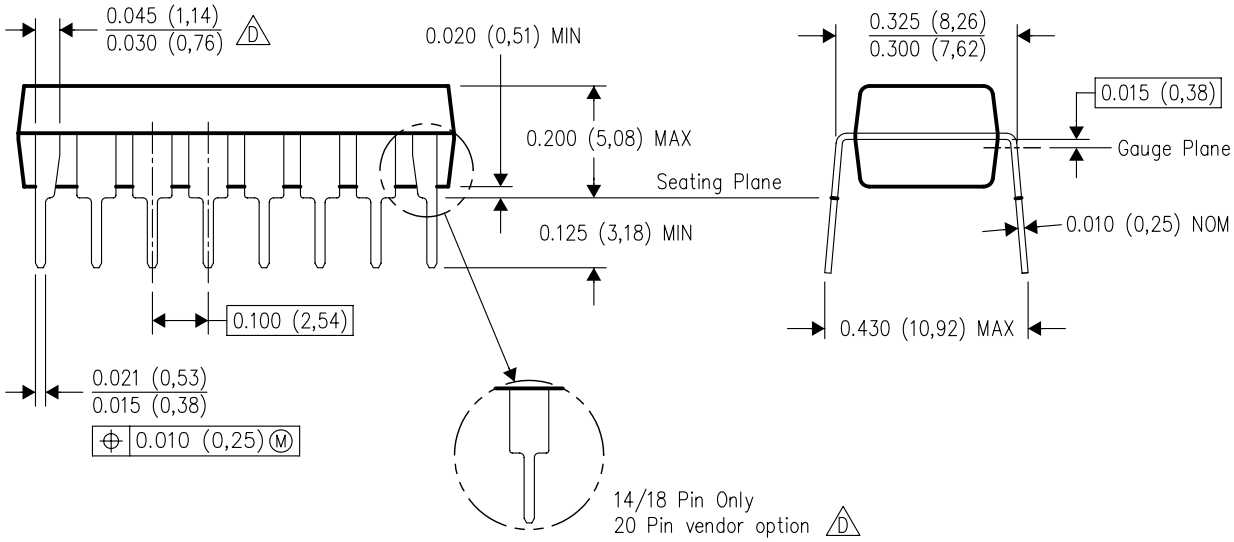
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月