

Control-Panel Workcell V2.0.1 — Board Capabilities

A Raspberry Pi Compute Module 5 carrier and smart power-distribution hub for Adom workcells. It takes four bench/PSU inputs, meters every rail with 20-bit precision, switches power and debug out to a docked Scaffold board (RP2350 + user breakouts), and provides the workcell's network, USB, CAN-FD, wireless, sensing, and indicator infrastructure.

Project	control-panel_workcell rev V2.0.1 (KiCad, 7 hierarchical sheets)
Compute	Raspberry Pi CM5 (CM5 Lite assumed — microSD boot, nRPIBOOT not broken out)
Board	172 × 72 mm, 6-layer (F / In1-In4 / B)
Status	DRC clean — 0 violations, 0 unconnected pads (report 2026-06-10)
Open hardware	OSHW logo on root sheet

1. Power input & distribution

Four independent supply inputs land on **J1** (WAGO 2604-1108, 8-position, dual contacts per pole) and are individually metered. Three of them are delivered to the docked Scaffold board through **J2** (Samtec ET60S-S03 — three 60 A-class power blades + 25 signal pins).

Rail plan (root-sheet table, IPC-2152 minimums @20 °C)

Rail	Voltage	Current	Function	Path
PS1	0–60 V	12 A (controlled)	USER — variable rail to Scaffold	J1 → 13 mΩ shunt → J2 blade P1
PS2	5 V	10 A (relayed)	USER — switched rail to Scaffold	J1 → 16 mΩ shunt → TPS22990 load switch → J2 blade P2
PS3	spare (rated 24 V)	spare	USER — future rail	J1 → (shunt unpopulated) → J2 blade P3
PS4	5 V	10 A (7 A realistic)	CONTROL — powers this board + CM5	J1 → 6.3 A fuse (Littelfuse Nano2 045106.3MRL) → 16 mΩ shunt → CM5 / regulators
+3V3	3.3 V	3 A	Board logic	AP3441 buck (U5) from PS4, enabled by CM5 <code>VBUS_EN</code> (pin 111)
M.2 3.3 V	3.3 V	3 A max	M.2 Key-E slot	AP3441 buck (U14) from PS4, enabled by CM5 <code>PCIE_PWR_EN</code> (pin 106)

PS2 switching ("relay"): CM5 `CAM_GPI01` (pin 100) → NSI8210 digital isolator (U6) → TPS22990 10 A load switch (3.9 mΩ R_{ON} , controlled 3 ms slew). The isolator lets PS2's return (`-PS2`) float up to 2.5 V from common ground. Readback channel senses the switched state.

Grounding: machine-pin jumpers select the scheme — jumper installed: common GND is bonded to EGND; uninstalled: supply grounds float. PS1/PS2/PS3 returns are carried as separate nets to the J2 blades.

Protection: PS4 — 6.3 A fuse + SMBJ6.0A TVS (D1) + PTVS7V5 on the protected node. USB VBUS — TPS25940 eFuse (see §4).

Power telemetry — 4× INA228 (20-bit, ±0.05 %)

All four on CM5 **I2C1** (`PWR_I2C-1` , GPIO2/3), alert pins unused; Kelvin-sensed 2512 3 W 1 % shunts with 0 Ω sense links and RC filtering:

Device	Rail	Address	Shunt	Range / resolution
U2	PS1	0x45	13 mΩ	0–12.6 A, floor 24 μA, 1.87 W @12 A
U3	PS2	0x44	16 mΩ	0–10.24 A, floor 19.5 μA, 1.6 W @10 A
U4	PS3	0x41	(fit with PS3)	bus-voltage monitoring ready
U1	PS4	0x40	16 mΩ	0–10.24 A

Each INA228 also reads its rail's bus voltage (0–85 V capable — covers PS1's 60 V range).

2. Compute — CM5 socket

- Two Hirose-style 100-pin connectors (**J4** = pins 1–100, **J7** = pins 101–200). Full pin map: see CM5_Pinout_Tree.md.
- **microSD** (Molex 503398-1892, J5) on the SDIO bus — SDR25 @50 MHz. SD power gated by an RT9742 current-limited switch (`SD_PWR_ON`). SD signals only exist on CM5 Lite (no eMMC); nRPIBOOT is not broken out, so plan on Lite modules + SD imaging.
- Power button (SW1), buffered power LED (Q1), activity LED, EEPROM write-protect jumper (JP5).
- No RTC backup battery (VBAT n.c.); HDMI, MIPI CSI/DSI, and fan header are unused — headless box.
- CM5 5 V input budget: CPU peak ~2.5 A, GPU unused (designer note).

3. Networking

Interface	Implementation
Gigabit Ethernet	CM5 PHY direct to HR911130A integrated-magnetics RJ45 (J6) with green/yellow speed LEDs + activity LED. Length-tuned (400 ps rule, critical length ≈33 mm).
Wi-Fi (PCIe)	M.2 Key-E slot (J8): PCIe Gen2 x1 (90 Ω matched), CLKREQ/WAKE/PERST, dedicated 3.3 V buck, M2×1.5 standoff. Intended module: Intel AX210 -class.
Bluetooth (USB)	AX210 BT runs over USB2: CM5 USB3-1 D± is routed through a TMUXHS221 2:1 mux — NC = Bluetooth, NO = USB-A connector . GPIO27 selects, GPIO17 enables. USB-A USB2 and Bluetooth are mutually exclusive.
CAN FD	MCP251863 (U15 — MCP2518FD controller + ATA6563 transceiver, 40 MHz crystal) on CM5 SPI4 (GPIO5–11, three interrupt lines). CANH/L exit on J3 (WAGO 2060-452, dual contacts per pole for daisy-chaining) with split-termination jumper JP6 (open = unterminated).

4. USB

Port	Lanes	Power	Notes
USB-C (J10)	CM5 USB3-0 SS pair via HD3SS3212 orientation mux + D±	Source: PS2 → TPS25940 eFuse (I_{LIM} 4.45 A, OVP 5.68 V, UVLO 4.29 V) → Q2 P-FET	TUSB321 CC controller strapped DFF (host) , 3.0 A advertised ; CM5 <code>USB_0TG</code> strapped host. ESD on all pairs.
USB-A 3.0 (J9)	CM5 USB3-1 SS pair direct; D± via TMUXHS221 (shared with Bluetooth)	VBUS from the same TPS25940 output	Full SuperSpeed regardless of mux; USB2 only when mux is set to NO
USB 2.0 (internal)	CM5 dedicated USB2 port (pins 103/105)	—	Hard-wired to the on-board PiProbe debug molecule

5. Scaffold dock (J2 — Samtec ET60S-S03)

The board's purpose: dock a **Scaffold board** carrying an RP2350 and user breakouts.

- **Power blades:** P1 = PS1 (0–60 V metered), P2 = PS2 (5 V, CM5-switched), P3 = PS3 (spare). Five contacts per blade polarity, separate returns.
- **Debug:** SWD (`DEBUG_SWD` / `DEBUG_SWCLK`) and UART (`DEBUG_TX` / `DEBUG_RX`) from the on-board PiProbe — the CM5 can flash/debug the Scaffold RP2350 with stock `openocd` / `picotool` tooling. `MCU_BOOT` (CAM_GPIO0) and `MCU_RST` (GPIO21) give the CM5 direct boot-strap/reset control of the RP2350.
- **Spare GPIO:** 4 lines (GPIO0/4/14/15) to J2 via jumpers JP1–JP4 — GPIO14/15 can instead be the Linux serial console (`enable_uart=1`).
- **Rails out:** +3v3 and +PS4 (5 V) service pins, plus grounds.

6. Embedded molecules (Adom standard slots)

Slot	Molecule	Bus	Function
N1	PiProbe v1.2 (RP2040, footprint-identical to the Raspberry Pi Debug Probe)	CM5 USB2	CMSIS-DAP SWD + UART bridge to the Scaffold RP2350; its own BOOTSEL/RST are CM5-controlled (GPIO22/23) so the CM5 can re-flash the probe itself
N2, N4	8×8 mm Bosch-standard sensor slots (swappable — e.g. BME690 gas/T/H/P, BMA accelerometer)	SENSOR_I2C-2 (GPIO12/13) + shared INT (GPIO16)	Environmental / motion sensing; any 8×8 molecule with the standard VCC/SCL/GND/SDA/INT1/INT2 pad ring fits
N3	I2S MEMS microphone carrier (mono, SEL = GND)	MIC_I2S-0 (GPIO18/19/20)	Audio capture

7. Indicators

- **TCA6424A** 24-bit I2C expander (U16, addr 0x22, on I2C0 / LED_I2C-0, reset from ID_SC).
- Drives **18 blue LEDs arranged in a ring** (placement angles −155°...170° — designer note: "pulse LEDs in cycle to view camera functionality") plus 4 status LEDs (2 red, 2 green: power/system states). 6 expander ports spare.
- RJ45 bezel LEDs driven directly by the CM5 Ethernet LED pins.

8. I2C / bus map (CM5 side)

Bus	CM5 pins	Devices
I2C0 (LED_I2C-0)	SCL0/SDA0 (80/82)	TCA6424A @0x22, CM5 ID EEPROM domain
I2C1 (PWR_I2C-1)	GPIO2/3 (56/58, internal 1.8 k pulls)	INA228 ×4 @0x40/0x41/0x44/0x45
I2C (SENSOR_I2C-2)	GPIO12/13 + INT GPIO16	Sensor molecule slots N2/N4
SPI4 (CAN_SPI-4)	GPIO5-11	MCP251863 CAN-FD
I2S0 (MIC_I2S-0)	GPIO18/19/20	MEMS mic slot N3
USB2	103/105	PiProbe
Free GPIO	GPIO26 only (pin 24)	—

9. Review notes (V2.0.1)

1. **Ethernet pair 2 polarity** — pin 9 (Pair2_N) → TRD2_P, pin 11 (Pair2_P) → TRD2_N. Benign in practice (GbE PHYs auto-correct per-pair polarity), but worth normalizing.
2. Input Power.kicad_sch **is orphaned** — present in the project folder but no longer in the sheet hierarchy (superseded by Input_Sense). Its INA228 address notes (" +5V_CAN", " +5V_DED", "VARIABLE") survive as stale text. Consider deleting to avoid confusion.
3. **No RTC battery / no nRPIBOOT** — fine for CM5 Lite + SD workflow, but eMMC modules can't be provisioned in-system and the RTC won't keep time across power loss.
4. **PS3 shunt deliberately unpopulated** — schematic note: "Add PS3 shunt when supply is populated." Document in the build/BOM notes so telemetry isn't silently dead on PS3.
5. DRC: clean (NPTH-in-courtyard, footprint-type and library-mismatch checks ignored by config).

Companion documents: [CM5_Pinout_Tree.md](#) (full 200-pin tree + tables), [cm5_pinout_tree.html](#) (interactive), [Control-Panel_Workcell_V2.0.1_Spec.pdf](#) (shareable spec).

CM5 Pinout Tree Map — Control-Panel Workcell V2.0.1

Compute Module 5 on two Hirose 100-pin board-to-board connectors: **J4** = CM5A (pins 1–100, low-speed/GPIO side), **J7** = CM5B (pins 101–200, high-speed side). Net names are the board schematic nets; generated from the routed PCB netlist (DRC-clean).

Tree map by subsystem

CM5 (J4 + J7, 200 pins)

Power (13 pins)

Unused

76 VBAT -> (n.c.)
99 PMIC_ENABLE -> (n.c.)

5 V input

77 +5v_(Input) -> +PS4_SENS
79 +5v_(Input) -> +PS4_SENS
81 +5v_(Input) -> +PS4_SENS
83 +5v_(Input) -> +PS4_SENS
85 +5v_(Input) -> +PS4_SENS
87 +5v_(Input) -> +PS4_SENS

GPIO_VREF

78 GPIO_VREF(1.8v/3.3v_Input) -> GPIO_VREF

3.3 V output

84 +3.3v_(Output) -> +3v3_CM5
86 +3.3v_(Output) -> +3v3_CM5

1.8 V output

88 +1.8v_(Output) -> (n.c.)
90 +1.8v_(Output) -> (n.c.)

Ground – 51 pins

pins 1-2, 7-8, 13-14, 22-23, 32-33, 42-43, 52-53, 59-60, 65-66, 71, 74, 98, 107-108, 113-114, 119-120, 125-126, 131-132, 137-138, 144, 150, 155-156, 161-162, 167-168, 173-174, 179-180, 185-186, 191-192, 197-198

Ethernet (GigE) (12 pins)

Pair 3

3 Ethernet_Pair3_P -> ETH.TRD3_P
5 Ethernet_Pair3_N -> ETH.TRD3_N

Pair 1

4 Ethernet_Pair1_P -> ETH.TRD1_P
6 Ethernet_Pair1_N -> ETH.TRD1_N

Pair 2

9 Ethernet_Pair2_N -> ETH.TRD2_P
11 Ethernet_Pair2_P -> ETH.TRD2_N

Pair 0

10 Ethernet_Pair0_N -> ETH.TRD0_N
12 Ethernet_Pair0_P -> ETH.TRD0_P

LEDs

15 Ethernet_nLED3(3.3v) -> ETH_LEDG
17 Ethernet_nLED2(3.3v) -> ETH_LEDY
21 LED_nACT -> LED_nACT

Unused

18 Ethernet_SYNC_OUT(3.3v) -> (n.c.)

microSD (CM5 Lite) (12 pins)

SDIO 4-bit

57 SD_CLK -> SD_CLK
61 SD_DAT3 -> SD_DAT3
62 SD_CMD -> SD_CMD
63 SD_DAT0 -> SD_DAT0
67 SD_DAT1 -> SD_DAT1
69 SD_DAT2 -> SD_DAT2

Unused

64 SD_DAT5 -> (n.c.)
68 SD_DAT4 -> (n.c.)
70 SD_DAT7 -> (n.c.)
72 SD_DAT6 -> (n.c.)
73 SD_VDD_Override -> (n.c.)

Power

75 SD_PWR_ON -> SD_PWR_ON

I2C buses (7 pins)

SENSOR_I2C-2 (GPIO13/12)

28 GPIO13 -> SENSOR_I2C-2.SCL
31 GPIO12 -> SENSOR_I2C-2.SDA

SENSOR_I2C-2 INT (GPIO16)

29 GPIO16 -> SENSOR_I2C-2.INT

PWR_I2C-1 (GPIO2/3)

56 GPIO3 -> PWR_I2C-1.SCL
58 GPIO2 -> PWR_I2C-1.SDA

LED_I2C-0 (SCL0/SDA0)

80 SCL0 -> LED_I2C-0.SCL
82 SDA0 -> LED_I2C-0.SDA

CAN FD (SPI4) (7 pins)

Interrupts

30 GPIO6 -> CAN_SPI-4.nINT0

	34	GPI05	-> CAN_SPI-4.nINT
	37	GPI07	-> CAN_SPI-4.nINT1
SPI			
	38	GPI011	-> CAN_SPI-4.SCK
	39	GPI08	-> CAN_SPI-4.nCS
	40	GPI09	-> CAN_SPI-4.SD0
	44	GPI010	-> CAN_SPI-4.SDI
I2S microphone (3 pins)			
MIC_I2S-0 (GPI019/20/18)			
	26	GPI019	-> MIC_I2S-0.WS
	27	GPI020	-> MIC_I2S-0.SD
	49	GPI018	-> MIC_I2S-0.SCK
USB 2.0 OTG (3 pins)			
USB_OTG_ID			
	101	USB_OTG_ID	-> USB_OTG
USB2 D±			
	103	USB2_N	-> DEBUG_USB2_N
	105	USB2_P	-> DEBUG_USB2_P
USB3-0 (USB-C J10) (6 pins)			
SuperSpeed + D±			
	128	USB3-0-RX_N	-> USER_USB3-0.RX_N
	130	USB3-0-RX_P	-> USER_USB3-0.RX_P
	134	USB3-0-D_P	-> USER_USB3-0.D_P
	136	USB3-0-D_N	-> USER_USB3-0.D_N
	140	USB3-0-TX_N	-> USER_USB3-0.TX_N
	142	USB3-0-TX_P	-> USER_USB3-0.TX_P
USB3-1 (USB-A J9) (6 pins)			
SuperSpeed + D±			
	157	USB3-1-RX_N	-> USER_USB3-1.RX_N
	159	USB3-1-RX_P	-> USER_USB3-1.RX_P
	163	USB3-1-D_P	-> MUX_USB3-1.D_P
	165	USB3-1-D_N	-> MUX_USB3-1.D_N
	169	USB3-1-TX_N	-> USER_USB3-1.TX_N
	171	USB3-1-TX_P	-> USER_USB3-1.TX_P
USB3-1 mux control (2 pins)			
MUX_USB3-1_SEL (GPI027)			
	48	GPI027	-> MUX_USB3-1_SEL
MUX_USB3-1_0En (GPI017)			
	50	GPI017	-> MUX_USB3-1_0En
PCIe Gen2 x1 (11 pins)			
Control			
	102	PCIe_nCLKREQ	-> PCIe.nCLKREQ
	104	PCIe_nWAKE	-> PCIe.nWAKE
	109	PCIe_nRST	-> PCIe_nRST
Power enable			
	106	PCIe_PWR_EN	-> PCIe.PWR_EN
Lanes			
	110	PCIe_CLK_P	-> WIFI_PCIe.CLK_P
	112	PCIe_CLK_N	-> WIFI_PCIe.CLK_N
	116	PCIe_RX_P	-> WIFI_PCIe.RX_P
	118	PCIe_RX_N	-> WIFI_PCIe.RX_N
	122	PCIe_TX_P	-> WIFI_PCIe.TX_P
	124	PCIe_TX_N	-> WIFI_PCIe.TX_N
VBUS_EN			
	111	VBUS_EN	-> 3v3_PWR_EN
M.2 / PCIe control (2 pins)			
BT_REG_ON (GPI025)			
	41	GPI025	-> PCIe.BT_REG_ON
WL_REG_ON (GPI024)			
	45	GPI024	-> PCIe.WL_REG_ON
PiProbe debug (2 pins)			
DEBUG_BOOT (GPI022)			
	46	GPI022	-> DEBUG_BOOT
DEBUG_RST (GPI023)			
	47	GPI023	-> DEBUG_RST
Scaffold dock (J2) (7 pins)			
MCU_RST (GPI021)			
	25	GPI021	-> MCU_RST
SPARE.I00 (ID_SD)			
	36	ID_SD	-> SPARE.I00
SPARE.I015 (GPI015)			
	51	GPI015	-> SPARE.I015
SPARE.I04 (GPI04)			
	54	GPI04	-> SPARE.I04
SPARE.I014 (GPI014)			
	55	GPI014	-> SPARE.I014
MCU_BOOT (CAM_GPI00)			
	97	CAM_GPI00	-> MCU_BOOT
PS2 enable (CAM_GPI01)			
	100	CAM_GPI01	-> +PS2_EN_I035
System (12 pins)			
Unused			
	16	FAN_TACH0	-> (n.c.)
	19	FAN_PWM	-> (n.c.)
	24	GPI026	-> (n.c.)
	89	WiFi_nDisable	-> (n.c.)
	91	BT_nDisable	-> (n.c.)
	93	nRPiB00T	-> (n.c.)
	94	CC1	-> (n.c.)

└─ 96	CC2	-> (n.c.)
└─ EEPROM_nWP		
└─ 20	EEPROM_nWP	-> EEPROM_nWP
└─ EXPD_NRST (ID_SC)		
└─ 35	ID_SC	-> EXPD_NRST.IO1
└─ PWR_BUT		
└─ 92	PWR_BUT	-> PWR_BUT
└─ LED_nPWR		
└─ 95	LED_nPWR	-> nPWR_LED
└─ HDMI (unused)	(24 pins)	
└─ pins	143, 145, 146, 147, 148, 149, 151, 152, 153, 154, 158, 160, 164, 166, 170, 172, 176, 178, 182, 184, 188, 190, 199, 200	
	(Headless design – HDMI0/HDMI1 not brought out)	
└─ MIPI CSI/DSI (unused)	(20 pins)	
└─ pins	115, 117, 121, 123, 127, 129, 133, 135, 139, 141, 175, 177, 181, 183, 187, 189, 193, 194, 195, 196	
	(No camera/display connectors fitted)	

Subsystem notes

Power

- **Unused** — VBAT RTC backup — not connected (no RTC battery)
- **Unused** — PMIC_ENABLE — not connected
- **5 V input** — Main 5 V from +PS4_SENS (PS4 input, fused 6.3 A, INA228-metered)
- **GPIO_VREF** — GPIO bank reference — strapped on CM5_GPIO sheet (3.3 V logic)
- **3.3 V output** — CM5 3.3 V out (600 mA max) — I2C pull-ups, misc logic
- **1.8 V output** — CM5 1.8 V out — unused

Ethernet (GigE)

- **Pair 3** — To HR911130A magjack J6 (TRD3)
- **Pair 1** — To HR911130A magjack J6 (TRD1)
- **Pair 2** — To HR911130A magjack J6 (TRD2) — note P/N crossed vs pin name
- **Pair 0** — To HR911130A magjack J6 (TRD0)
- **LEDs** — Green speed LED in RJ45 bezel
- **LEDs** — Yellow speed LED in RJ45 bezel
- **LEDs** — Activity LED (LED_nACT)
- **Unused** — Ethernet SYNC_OUT — not used

microSD (CM5 Lite)

- **SDIO 4-bit** — Molex 503398-1892 socket J5, SDR25 @50 MHz
- **Unused** — SD_DAT4-7 not used (4-bit bus)
- **Unused** — SD_VDD_Override not used
- **Power** — Enables RT9742 switch gating 3v3 to SD socket

I2C buses

- **SENSOR_I2C-2 (GPIO13/12)** — Sensor molecule bus: N2 + N4 8x8 Bosch-standard slots
- **SENSOR_I2C-2 INT (GPIO16)** — Shared interrupt from sensor slots
- **PWR_I2C-1 (GPIO2/3)** — Power telemetry bus: 4x INA228 @ 0x40/0x44/0x41/0x45 (internal 1.8k pulls on CM5)
- **LED_I2C-0 (SCL0/SDA0)** — TCA6424A LED expander @ 0x22 (+ CM5 ID EEPROM bus)

CAN FD (SPI4)

- **Interrupts** — MCP251863 nINT / nINT0(RX) / nINT1(TX)
- **SPI** — MCP251863 CAN-FD controller U15: SCK/nCS/SDO/SDI

I2S microphone

- **MIC_I2S-0 (GPIO19/20/18)** — N3 Carrier_I2S MEMS mic slot (mono, SEL=GND)

USB 2.0 OTG

- **USB_OTG ID** — OTG ID strap (0 = host) — CM5 USB2 hosts the PiProbe
- **USB2 D±** — Dedicated USB2 port -> PiProbe N1 (CMSIS-DAP + UART bridge)

USB3-0 (USB-C J10)

- **SuperSpeed + D±** — Via HD3SS3212 orientation mux; TUSB321 CC (DFP host, 3 A); VBUS from PS2 via TPS25940 eFuse + Q2

USB3-1 (USB-A J9)

- **SuperSpeed + D±** — SS lanes direct to USB-A; D± via TMUXHS221 mux (shared with M.2 Bluetooth USB)

USB3-1 mux control

- **MUX_USB3-1_SEL (GPIO27)** — TMUXHS221: routes CM5 USB3-1 D± to USB-A (NO) or M.2 Bluetooth (NC)
- **MUX_USB3-1_OEn (GPIO17)** — TMUXHS221 output enable, active low

PCIe Gen2 x1

- **Control** — nCLKREQ / nWAKE / nRST to M.2
- **Power enable** — Enables AP3441 buck U14 -> 3.3 V to M.2 slot
- **Lanes** — CLK/RX/TX pairs to M.2 Key-E slot J8 (Wi-Fi, e.g. AX210)
- **VBUS_EN** — Enables AP3441 buck U5 -> board +3v3 rail

M.2 / PCIe control

- **BT_REG_ON (GPIO25)** — Bluetooth regulator enable to M.2 Key-E
- **WL_REG_ON (GPIO24)** — Wi-Fi regulator enable to M.2 Key-E

PiProbe debug

- **DEBUG_BOOT (GPIO22)** — BOOTSEL strap of on-board PiProbe RP2040 (N1)
- **DEBUG_RST (GPIO23)** — Reset of on-board PiProbe RP2040 (N1)

Scaffold dock (J2)

- **MCU_RST (GPIO21)** — Direct reset of Scaffold RP2350 via J2.5
- **SPARE.IO0 (ID_SD)** — Spare GPIO to J2.1 via jumper JP1
- **SPARE.IO15 (GPIO15)** — Spare GPIO to J2.7 via JP4 (alt: UART0 RX console)
- **SPARE.IO4 (GPIO4)** — Spare GPIO to J2.2 via jumper JP2
- **SPARE.IO14 (GPIO14)** — Spare GPIO to J2.6 via JP3 (alt: UART0 TX console)
- **MCU_BOOT (CAM_GPIO0)** — Boot strap of Scaffold RP2350 via J2.4
- **PS2 enable (CAM_GPIO1)** — Drives NSi8210 isolator -> TPS22990 switch: PS2 rail to Scaffold blade P2

System

- **Unused** — Fan tach/PWM — not used
- **Unused** — GPIO26 — unconnected (only free GPIO)
- **Unused** — WiFi/BT nDisable — not used (M.2 module instead of onboard radio)
- **Unused** — nRPiBOOT — not broken out (CM5 Lite + SD workflow assumed)
- **Unused** — CM5 CC1/CC2 — unused, USB-C CC handled by TUSB321
- **EEPROM_nWP** — CM5 EEPROM write protect, jumper JP5 to GND
- **EXPD_NRST (ID_SC)** — TCA6424A LED expander reset (force_eeprom_read=0)
- **PWR_BUT** — Power button SW1 (SKRSPACE010)
- **LED_nPWR** — Power LED via Q1 SS8550 buffer

HDMI (unused)

- Headless design — HDMI0/HDMI1 not brought out

MIPI CSI/DSI (unused)

- No camera/display connectors fitted

Appendix: J4 — CM5A (pins 1-100)

Pin	CM5 function	Board net	Subsystem
1	GND	GND	Ground

Pin	CM5 function	Board net	Subsystem
2	GND	GND	Ground
3	Ethernet_Pair3_P	ETH.TRD3_P	Ethernet (GigE)
4	Ethernet_Pair1_P	ETH.TRD1_P	Ethernet (GigE)
5	Ethernet_Pair3_N	ETH.TRD3_N	Ethernet (GigE)
6	Ethernet_Pair1_N	ETH.TRD1_N	Ethernet (GigE)
7	GND	GND	Ground
8	GND	GND	Ground
9	Ethernet_Pair2_N	ETH.TRD2_P	Ethernet (GigE)
10	Ethernet_Pair0_N	ETH.TRD0_N	Ethernet (GigE)
11	Ethernet_Pair2_P	ETH.TRD2_N	Ethernet (GigE)
12	Ethernet_Pair0_P	ETH.TRD0_P	Ethernet (GigE)
13	GND	GND	Ground
14	GND	GND	Ground
15	Ethernet_nLED3(3.3v)	ETH_LEDG	Ethernet (GigE)
16	FAN_TACHO	*n.c.*	System
17	Ethernet_nLED2(3.3v)	ETH_LEDY	Ethernet (GigE)
18	Ethernet_SYNC_OUT(3.3v)	*n.c.*	Ethernet (GigE)
19	FAN_PWM	*n.c.*	System
20	EEPROM_nWP	EEPROM_nWP	System
21	LED_nACT	LED_nACT	Ethernet (GigE)
22	GND	GND	Ground
23	GND	GND	Ground
24	GPIO26	*n.c.*	System
25	GPIO21	MCU_RST	Scaffold dock (J2)
26	GPIO19	MIC_I2S-0.WS	I2S microphone
27	GPIO20	MIC_I2S-0.SD	I2S microphone
28	GPIO13	SENSOR_I2C-2.SCL	I2C buses
29	GPIO16	SENSOR_I2C-2.INT	I2C buses
30	GPIO6	CAN_SPI-4.nINT0	CAN FD (SPI4)
31	GPIO12	SENSOR_I2C-2.SDA	I2C buses
32	GND	GND	Ground
33	GND	GND	Ground
34	GPIO5	CAN_SPI-4.nINT	CAN FD (SPI4)
35	ID_SC	EXPD_NRST.I01	System
36	ID_SD	SPARE.I00	Scaffold dock (J2)
37	GPIO7	CAN_SPI-4.nINT1	CAN FD (SPI4)
38	GPIO11	CAN_SPI-4.SCK	CAN FD (SPI4)
39	GPIO8	CAN_SPI-4.nCS	CAN FD (SPI4)
40	GPIO9	CAN_SPI-4.SD0	CAN FD (SPI4)
41	GPIO25	PCIE.BT_REG_ON	M.2 / PCIe control
42	GND	GND	Ground
43	GND	GND	Ground
44	GPIO10	CAN_SPI-4.SDI	CAN FD (SPI4)
45	GPIO24	PCIE.WL_REG_ON	M.2 / PCIe control
46	GPIO22	DEBUG_BOOT	PiProbe debug

Pin	CM5 function	Board net	Subsystem
47	GPIO23	DEBUG_RST	PiProbe debug
48	GPIO27	MUX_USB3-1_SEL	USB3-1 mux control
49	GPIO18	MIC_I2S-0.SCK	I2S microphone
50	GPIO17	MUX_USB3-1_0En	USB3-1 mux control
51	GPIO15	SPARE.I015	Scaffold dock (J2)
52	GND	GND	Ground
53	GND	GND	Ground
54	GPIO4	SPARE.I04	Scaffold dock (J2)
55	GPIO14	SPARE.I014	Scaffold dock (J2)
56	GPIO3	PWR_I2C-1.SCL	I2C buses
57	SD_CLK	SD_CLK	microSD (CM5 Lite)
58	GPIO2	PWR_I2C-1.SDA	I2C buses
59	GND	GND	Ground
60	GND	GND	Ground
61	SD_DAT3	SD_DAT3	microSD (CM5 Lite)
62	SD_CMD	SD_CMD	microSD (CM5 Lite)
63	SD_DAT0	SD_DAT0	microSD (CM5 Lite)
64	SD_DAT5	*n.c.*	microSD (CM5 Lite)
65	GND	GND	Ground
66	GND	GND	Ground
67	SD_DAT1	SD_DAT1	microSD (CM5 Lite)
68	SD_DAT4	*n.c.*	microSD (CM5 Lite)
69	SD_DAT2	SD_DAT2	microSD (CM5 Lite)
70	SD_DAT7	*n.c.*	microSD (CM5 Lite)
71	GND	GND	Ground
72	SD_DAT6	*n.c.*	microSD (CM5 Lite)
73	SD_VDD_Override	*n.c.*	microSD (CM5 Lite)
74	GND	GND	Ground
75	SD_PWR_ON	SD_PWR_ON	microSD (CM5 Lite)
76	VBAT	*n.c.*	Power
77	+5v_(Input)	+PS4_SENS	Power
78	GPIO_VREF(1.8v/3.3v_Input)	GPIO_VREF	Power
79	+5v_(Input)	+PS4_SENS	Power
80	SCL0	LED_I2C-0.SCL	I2C buses
81	+5v_(Input)	+PS4_SENS	Power
82	SDA0	LED_I2C-0.SDA	I2C buses
83	+5v_(Input)	+PS4_SENS	Power
84	+3.3v_(Output)	+3v3_CM5	Power
85	+5v_(Input)	+PS4_SENS	Power
86	+3.3v_(Output)	+3v3_CM5	Power
87	+5v_(Input)	+PS4_SENS	Power
88	+1.8v_(Output)	*n.c.*	Power
89	WiFi_nDisable	*n.c.*	System
90	+1.8v_(Output)	*n.c.*	Power
91	BT_nDisable	*n.c.*	System

Pin	CM5 function	Board net	Subsystem
92	PWR_BUT	PWR_BUT	System
93	nRPIBOOT	*n.c.*	System
94	CC1	*n.c.*	System
95	LED_nPWR	nPWR_LED	System
96	CC2	*n.c.*	System
97	CAM_GPIO0	MCU_B00T	Scaffold dock (J2)
98	GND	GND	Ground
99	PMIC_ENABLE	*n.c.*	Power
100	CAM_GPIO1	+PS2_EN_I035	Scaffold dock (J2)

Appendix: J7 — CM5B (pins 101-200)

Pin	CM5 function	Board net	Subsystem
101	USB_OTG_ID	USB_OTG	USB 2.0 OTG
102	PCIE_nCLKREQ	PCIE.nCLKREQ	PCle Gen2 x1
103	USB2_N	DEBUG_USB2_N	USB 2.0 OTG
104	PCIE_nWAKE	PCIE.nWAKE	PCle Gen2 x1
105	USB2_P	DEBUG_USB2_P	USB 2.0 OTG
106	PCIE_PWR_EN	PCIE.PWR_EN	PCle Gen2 x1
107	GND	GND	Ground
108	GND	GND	Ground
109	PCIE_nRST	PCIE.nRST	PCle Gen2 x1
110	PCIE_CLK_P	WIFI_PCIE.CLK_P	PCle Gen2 x1
111	VBUS_EN	3v3_PWR_EN	PCle Gen2 x1
112	PCIE_CLK_N	WIFI_PCIE.CLK_N	PCle Gen2 x1
113	GND	GND	Ground
114	GND	GND	Ground
115	MIPI0_D0_N	*n.c.*	MIPI CSI/DSI (unused)
116	PCie_RX_P	WIFI_PCIE.RX_P	PCle Gen2 x1
117	MIPI0_D0_P	*n.c.*	MIPI CSI/DSI (unused)
118	PCie_RX_N	WIFI_PCIE.RX_N	PCle Gen2 x1
119	GND	GND	Ground
120	GND	GND	Ground
121	MIPI0_D1_N	*n.c.*	MIPI CSI/DSI (unused)
122	PCie_TX_P	WIFI_PCIE.TX_P	PCle Gen2 x1
123	MIPI0_D1_P	*n.c.*	MIPI CSI/DSI (unused)
124	PCie_TX_N	WIFI_PCIE.TX_N	PCle Gen2 x1
125	GND	GND	Ground
126	GND	GND	Ground
127	MIPI0_C_N	*n.c.*	MIPI CSI/DSI (unused)
128	USB3-0-RX_N	USER_USB3-0.RX_N	USB3-0 (USB-C J10)
129	MIPI0_C_P	*n.c.*	MIPI CSI/DSI (unused)
130	USB3-0-RX_P	USER_USB3-0.RX_P	USB3-0 (USB-C J10)
131	GND	GND	Ground
132	GND	GND	Ground

Pin	CM5 function	Board net	Subsystem
133	MIPI0_D2_N	*n.c.*	MIPI CSI/DSI (unused)
134	USB3-0-D_P	USER_USB3-0.D_P	USB3-0 (USB-C J10)
135	MIPI0_D2_P	*n.c.*	MIPI CSI/DSI (unused)
136	USB3-0-D_N	USER_USB3-0.D_N	USB3-0 (USB-C J10)
137	GND	GND	Ground
138	GND	GND	Ground
139	MIPI0_D3_N	*n.c.*	MIPI CSI/DSI (unused)
140	USB3-0-TX_N	USER_USB3-0.TX_N	USB3-0 (USB-C J10)
141	MIPI0_D3_P	*n.c.*	MIPI CSI/DSI (unused)
142	USB3-0-TX_P	USER_USB3-0.TX_P	USB3-0 (USB-C J10)
143	HDMI1_HOTPLUG	*n.c.*	HDMI (unused)
144	GND	GND	Ground
145	HDMI1_SDA	*n.c.*	HDMI (unused)
146	HDMI1_TX2_P	*n.c.*	HDMI (unused)
147	HDMI1_SCL	*n.c.*	HDMI (unused)
148	HDMI1_TX2_N	*n.c.*	HDMI (unused)
149	HDMI1_CEC	*n.c.*	HDMI (unused)
150	GND	GND	Ground
151	HDMI0_CEC	*n.c.*	HDMI (unused)
152	HDMI1_TX1_P	*n.c.*	HDMI (unused)
153	HDMI0_HOTPLUG	*n.c.*	HDMI (unused)
154	HDMI1_TX1_N	*n.c.*	HDMI (unused)
155	GND	GND	Ground
156	GND	GND	Ground
157	USB3-1-RX_N	USER_USB3-1.RX_N	USB3-1 (USB-A J9)
158	HDMI1_TX0_P	*n.c.*	HDMI (unused)
159	USB3-1-RX_P	USER_USB3-1.RX_P	USB3-1 (USB-A J9)
160	HDMI1_TX0_N	*n.c.*	HDMI (unused)
161	GND	GND	Ground
162	GND	GND	Ground
163	USB3-1-D_P	MUX_USB3-1.D_P	USB3-1 (USB-A J9)
164	HDMI1_CLK_P	*n.c.*	HDMI (unused)
165	USB3-1-D_N	MUX_USB3-1.D_N	USB3-1 (USB-A J9)
166	HDMI1_CLK_N	*n.c.*	HDMI (unused)
167	GND	GND	Ground
168	GND	GND	Ground
169	USB3-1-TX_N	USER_USB3-1.TX_N	USB3-1 (USB-A J9)
170	HDMI0_TX2_P	*n.c.*	HDMI (unused)
171	USB3-1-TX_P	USER_USB3-1.TX_P	USB3-1 (USB-A J9)
172	HDMI0_TX2_N	*n.c.*	HDMI (unused)
173	GND	GND	Ground
174	GND	GND	Ground
175	MIPI1_D0_N	*n.c.*	MIPI CSI/DSI (unused)
176	HDMI0_TX1_P	*n.c.*	HDMI (unused)
177	MIPI1_D0_P	*n.c.*	MIPI CSI/DSI (unused)

Pin	CM5 function	Board net	Subsystem
178	HDMI0_TX1_N	*n.c.*	HDMI (unused)
179	GND	GND	Ground
180	GND	GND	Ground
181	MIPI1_D1_N	*n.c.*	MIPI CSI/DSI (unused)
182	HDMI0_TX0_P	*n.c.*	HDMI (unused)
183	MIPI1_D1_P	*n.c.*	MIPI CSI/DSI (unused)
184	HDMI0_TX0_N	*n.c.*	HDMI (unused)
185	GND	GND	Ground
186	GND	GND	Ground
187	MIPI1_C_N	*n.c.*	MIPI CSI/DSI (unused)
188	HDMI0_CLK_P	*n.c.*	HDMI (unused)
189	MIPI1_C_P	*n.c.*	MIPI CSI/DSI (unused)
190	HDMI0_CLK_N	*n.c.*	HDMI (unused)
191	GND	GND	Ground
192	GND	GND	Ground
193	MIPI1_D2_N	*n.c.*	MIPI CSI/DSI (unused)
194	MIPI1_D3_N	*n.c.*	MIPI CSI/DSI (unused)
195	MIPI1_D2_P	*n.c.*	MIPI CSI/DSI (unused)
196	MIPI1_D3_P	*n.c.*	MIPI CSI/DSI (unused)
197	GND	GND	Ground
198	GND	GND	Ground
199	HDMI0_SDA	*n.c.*	HDMI (unused)
200	HDMI0_SCL	*n.c.*	HDMI (unused)